STV7697A

PLASMA DISPLAY PANEL SCAN DRIVER

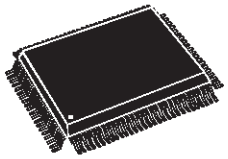
FEATURES

- 64 OUTPUTS PLASMA DISPLAY DRIVER
- 170V ABSOLUTE MAXIMUM SUPPLY
- 5V SUPPLY FOR LOGIC
- 100/400 mA SOURCE / SINK OUTPUT
- 700 mA SOURCE / SINK OUTPUT DIODE
- 64-BIT SHIFT REGISTER (20 MHz)
- BLANK CONTROL
- COMPLEMENTARY OUTPUT CONTROL
- BCD TECHNOLOGY
- 100 PINS PQFP PACKAGE OR DICE.

DESCRIPTION

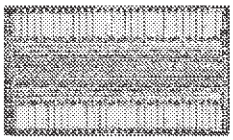
The STV7697A is a scan driver for Plasma Display Panel (PDP) implemented in ST's proprietary BCD technology. Using a 64-bit cascadable 20 MHz shift register, it drives 64 high current & high voltage outputs. By serially connecting several STV7697A, any vertical pixel definition can be performed. The STV7697A is supplied with a separated 160V power output supply and a 5V logic supply.All command inputs are CMOS compatible.

The STV769 7A package is a 100 pins PQFP.



PQFP100 (14 x 20 x 2.80 mm)
(Full Plastic Quad Flat Pack)

ORDER CODE: STV7697A



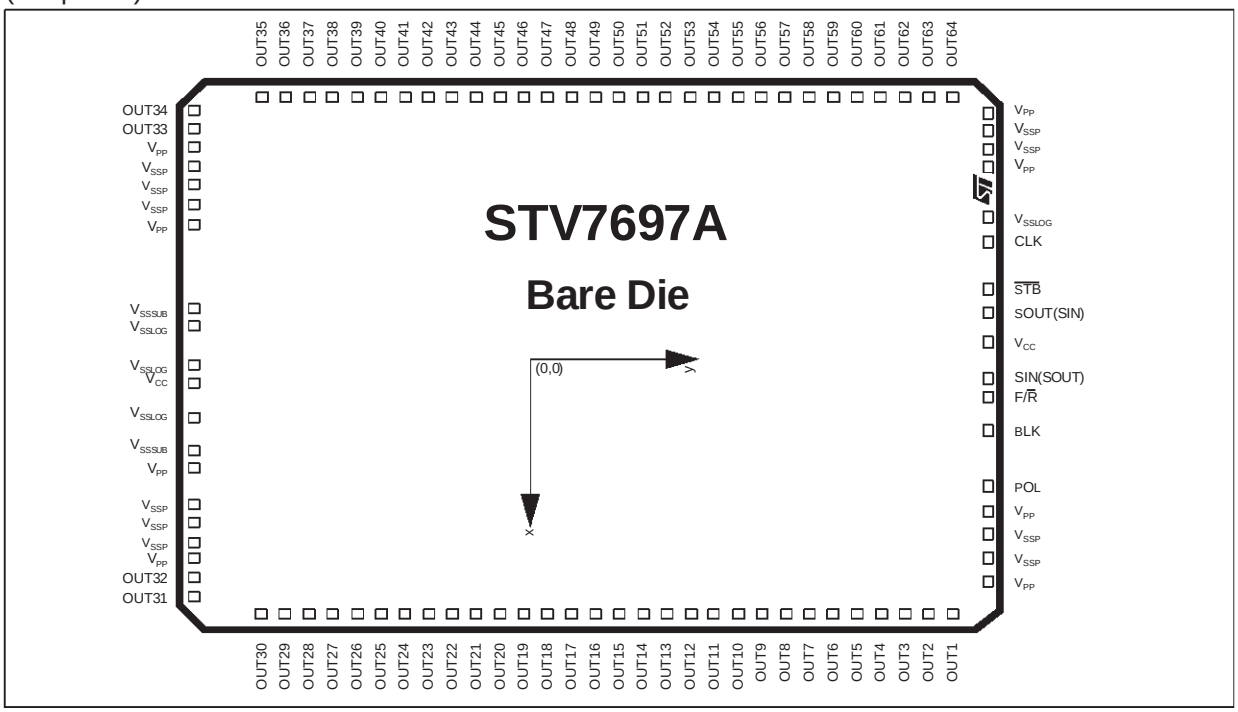
ORDER CODE: STV7697A/WAF (1)
(1): Unsawn Tested Wafer

Version 4.2

TABLE OF CONTENTS

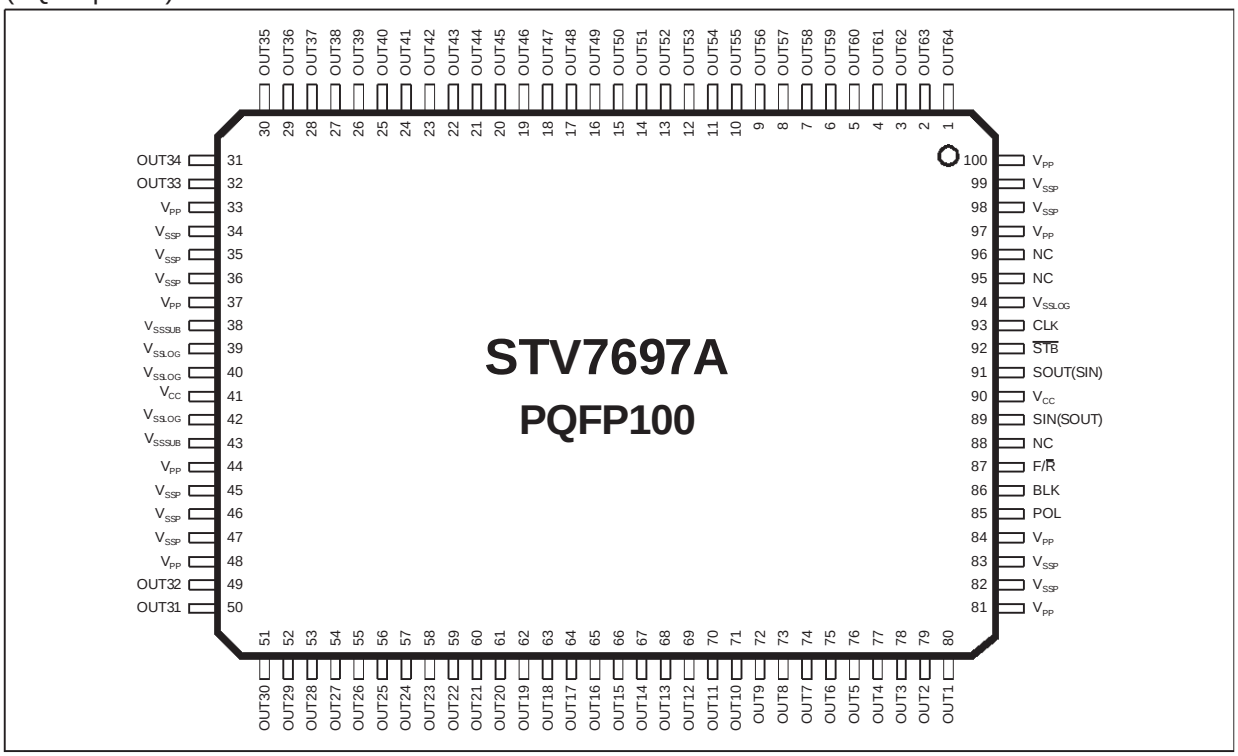
PIN CONNECTIONS

(Die pinout)



PIN CONNECTIONS

(TQFP pinout)



PIN ASSIGNMENT

(TQFP100)

Pin Number	Symbol	Type	Function
33-37-44-48-81-84-97-100	V_{PP}	Supply	High Voltage Supply of power outputs
41 - 90	V_{CC}	Supply	5 V Logic Supply
34-35-36-45-46-47-82-83-98-99	V_{SSP}	Ground	Ground of power outputs
38-43	V_{SSSUB}	Ground	Substrate Ground
39-40-42-94	V_{SSLOG}	Ground	Logic Ground
1 to 32, 49 to 80	OUT 64 to OUT 1	Output	Power Output
91	SOUT (SIN)	Output	Shift Register Data Output (forward)
85	POL	Input	Polarity Selection
86	BLK	Input	Output Blanking Command
87	$F/\overline{R}$	Input	Selection of shift direction
89	SIN (SOUT)	Input	Shift Register Data Input (forward)
92	$\overline{STB}$	Input	Latch of data to outputs
93	CLK	Input	Clock of data shift register
88-95-96	NC	-	

PIN ASSIGNMENT (Power Outputs)

Output N°	Pin N°	Output N°	Pin N°	Output N°	Pin N°	Output N°	Pin N°
1	80	17	64	33	32	49	16
2	79	18	63	34	31	50	15
3	78	19	62	35	30	51	14
4	77	20	61	36	29	52	13
5	76	21	60	37	28	53	12
6	75	22	59	38	27	54	11
7	74	23	58	39	26	55	10
8	73	24	57	40	25	56	9
9	72	25	56	41	24	57	8
10	71	26	55	42	23	58	7
11	70	27	54	43	22	59	6
12	69	28	53	44	21	60	5
13	68	29	52	45	20	61	4
14	67	30	51	46	19	62	3
15	66	31	50	47	18	63	2
16	65	32	49	48	17	64	1

PADS DIMENSIONS (in μm)/ PADS POSITIONS

The reference is the centre of the die (x=0, y=0)

TOP SIDE from left to right

Name	Centre:X	Centre:Y	Size:x	SIze: y
V_{PP}	-2468.5	4135.0	75.0	90.0
V_{SSP}	-2313.5	4135.0	75.0	90.0
V_{SSP}	-2188.5	4135.0	75.0	90.0
V_{PP}	-2063.5	4134.5	75.0	90.0
V_{SSLOG}	-1620.0	4135.0	75.0	90.0
CLK	-1430.0	4135.0	75.0	90.0
$\overline{STB}$	-781.0	4135.0	75.0	90.0
SOUT	-612.5	4135.0	75.0	90.0
V_{CC}	-335.5	4144.5	75.0	90.0
SIN	379.5	4135.0	75.0	90.0
F/$\overline{R}$	548.0	4135.0	75.0	90.0
BLK	1082.0	4135.0	75.0	90.0
POL	1853.0	4135.0	75.0	90.0
V_{PP}	2021.5	4140.0	75.0	90.0
V_{SSP}	2156.5	4140.0	75.0	90.0
V_{SSP}	2291.5	4140.0	75.0	90.0
V_{PP}	2454.5	4129.5	75.0	90.0

BOTTOM SIDE from left to right

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT34	-2468.0	-4087.5	75.0	90.0
OUT33	-2318.0	-4089.5	75.0	90.0
V_{PP}	-2182.0	-4089.5	75.0	90.0
V_{SSP}	-2047.0	-4093.0	75.0	90.0
V_{SSP}	-1912.0	-4093.0	75.0	90.0
V_{SSP}	-1777.0	-4093.0	75.0	90.0
V_{PP}	-1642.0	-4089.5	75.0	90.0
V_{SSSUB}	-683.0	-4088.0	75.0	90.0
V_{SSLOG}	-382.5	-4088.0	75.0	90.0
V_{SSLOG}	419.5	-4087.5	75.0	90.0
V_{CC}	618.5	-4087.5	75.0	90.0
V_{SSLOG}	951.0	-4087.5	75.0	90.0
V_{SSSUB}	1308.0	-4087.5	75.0	90.0

BOTTOM SIDE from left to right (continued)

Name	Centre:X	Centre:Y	Size:x	SIze: y
V_{PP}	1438.5	-4087.5	75.0	90.0
V_{SSP}	1797.5	-4093.5	75.0	90.0
V_{SSP}	1932.5	-4093.5	75.0	90.0
V_{SSP}	2067.5	-4093.5	75.0	90.0
V_{PP}	2193.0	-4093.5	75.0	90.0
OUT32	2318.0	-4093.5	75.0	90.0
OUT31	2468.5	-4093.5	75.0	90.0

RIGHT SIDE from top to bottom

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT1	2647.0	3697.0	90.0	75.0
OUT2	2647.0	3484.0	90.0	75.0
OUT3	2647.0	3238.5	90.0	75.0
OUT4	2647.0	2992.5	90.0	75.0
OUT5	2647.0	2743.0	90.0	75.0
OUT6	2647.0	2506.5	90.0	75.0
OUT7	2647.0	2264.0	90.0	75.0
OUT8	2647.0	2018.0	90.0	75.0
OUT9	2647.0	1774.5	90.0	75.0
OUT10	2647.0	1529.0	90.0	75.0
OUT11	2647.0	1285.5	90.0	75.0
OUT12	2647.0	1040.0	90.0	75.0
OUT13	2647.0	796.5	90.0	75.0
OUT14	2647.0	551.0	90.0	75.0
OUT15	2647.0	307.5	90.0	75.0
OUT16	2647.0	62.0	90.0	75.0
OUT17	2647.0	-181.5	90.0	75.0
OUT18	2647.0	-427.0	90.0	75.0
OUT19	2647.0	-670.5	90.0	75.0
OUT20	2647.0	-916.0	90.0	75.0
OUT21	2647.0	-1159.5	90.0	75.0
OUT22	2647.0	-1405.0	90.0	75.0
OUT23	2647.0	-1648.5	90.0	75.0
OUT24	2647.0	-1894.0	90.0	75.0

RIGHT SIDE from top to bottom (continued)

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT25	2647.0	-2137.5	90.0	75.0
OUT26	2647.0	-2383.5	90.0	75.0
OUT27	2647.0	-2627.0	90.0	75.0
OUT28	2647.0	-2872.5	90.0	75.0
OUT29	2647.0	-3116.0	90.0	75.0
OUT30	2647.0	-3363.0	90.0	75.0

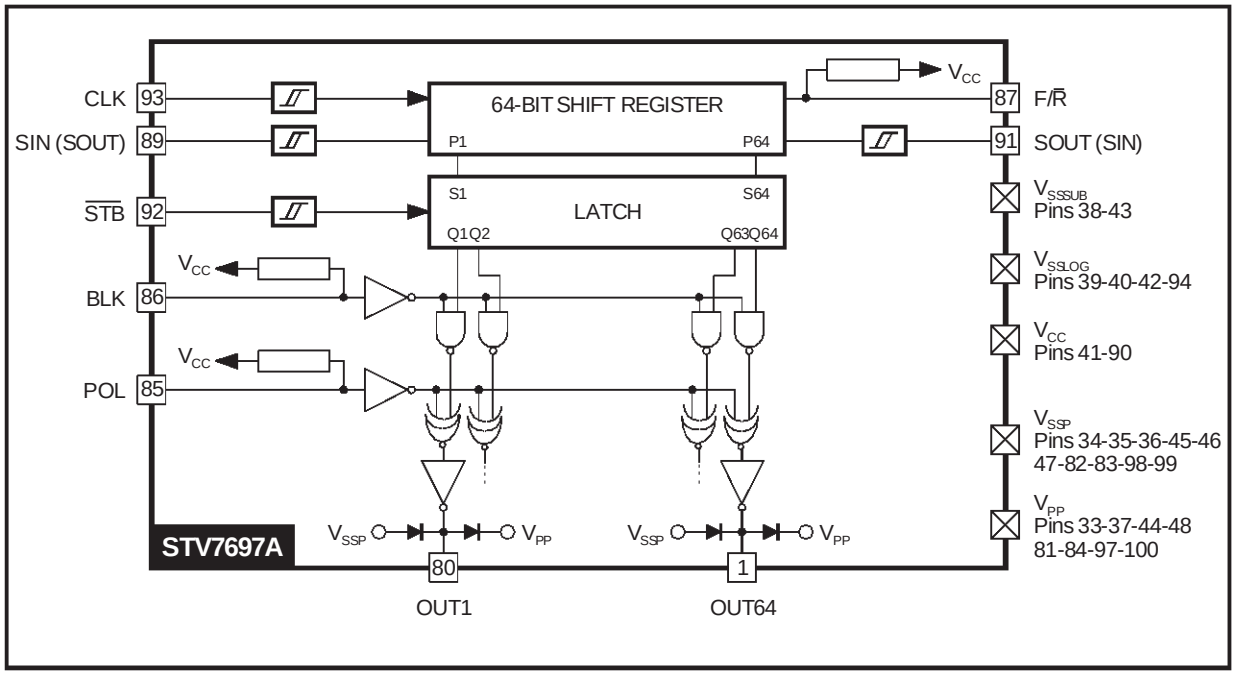
LEFT SIDE from bottom to top

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT35	-2646.5	-3363.0	90.0	75.0
OUT36	-2646.5	-3116.0	90.0	75.0
OUT37	-2646.5	-2872.5	90.0	75.0
OUT38	-2646.5	-2627.0	90.0	75.0
OUT39	-2646.5	-2383.5	90.0	75.0
OUT40	-2646.5	-2137.5	90.0	75.0
OUT41	-2646.5	-1894.0	90.0	75.0
OUT42	-2646.5	-1648.5	90.0	75.0
OUT43	-2646.5	-1405.0	90.0	75.0
OUT44	-2646.5	-1159.5	90.0	75.0
OUT45	-2646.5	-916.0	90.0	75.0
OUT46	-2646.5	-670.5	90.0	75.0
OUT47	-2646.5	-427.0	90.0	75.0
OUT48	-2646.5	-181.5	90.0	75.0
OUT49	-2646.5	62.0	90.0	75.0
OUT50	-2646.5	307.5	90.0	75.0
OUT51	-2646.5	551.0	90.0	75.0
OUT52	-2646.5	796.5	90.0	75.0
OUT53	-2646.5	1040.0	90.0	75.0
OUT54	-2646.5	1285.5	90.0	75.0
OUT55	-2646.5	1529.0	90.0	75.0
OUT56	-2646.5	1774.5	90.0	75.0
OUT57	-2646.5	2018.0	90.0	75.0
OUT58	-2646.5	2264.0	90.0	75.0
OUT59	-2646.5	2506.5	90.0	75.0
OUT60	-2646.5	2743.0	90.0	75.0

LEFT SIDE from bottom to top (continued)

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT61	-2646.5	2949.5	90.0	75.0
OUT62	-2646.5	3228.5	90.0	75.0
OUT63	-2646.5	3487.0	90.0	75.0
OUT64	-2646.5	3763.0	90.0	75.0

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The STV7697A contains all the logic and the power circuits necessary to drive rows of a Plasma Display Panel (P. D. P.). The state of the displayed line is loaded into the shift register. Data are shifted at each low to high transition of the (CLK) shift clock. After 64 shifts the first bit is available at the serial output. This output can be used to cascade several drivers to perform any vertical resolution.

The forward / reverse (F/$\overline{R}$) input is used to select the direction of the shift register, data input/output status is set according to the selected direction. SIN, CLK, $\overline{STB}$ inputs

are Smith trigger inputs . If not used on the application, F/$\overline{R}$, BLK, $\overline{POL}$ logical inputs are internaly pulled to level "1". The maximum frequency of the shift clock is 20 MHz.

All the data are memorized into the latch stage when the strobe input ($\overline{STB}$) is pulled high.

Blanking input ($\overline{BLK}$) forces the power outputs to high level when pulled high with polarity input (POL) at high level and forced to low level with POL at low level.

The level of the power output is inverted when the polarity command (POL) is pulled high.

Sustain current must not be sunk in the power output to V_{PP} when the power supply is applied.

V_{SSLOG} and V_{SSSUB} must be connected as close as possible to the logical reference ground of the application.

Shift Register Truth Table

Input		Input/Output		Shift Register Function
F/$\overline{R}$	CLK	SIN	SOUT	Output Q
H	Rise	IN	OUT	Forward Shift
H	H or L	IN	OUT	Steady
L	Rise	OUT	IN	Reverse Shift
L	H or L	OUT	IN	Steady

Power Output Truth Table

Qn (1)	$\overline{STB}$	BLK	POL	Driver Output	Comments
X	X	H	H	All H	Forced to High
X	X	H	L	All L	Forced to Low
H	L	L	L	H	Copy Data
L	L	L	L	L	Copy Data
H	L	L	H	L	Copy Inverted Data
L	L	L	H	H	Copy Inverted Data
X	H	L	L	Qn	Data Latched
X	H	L	H	$\overline{Qn}$	Inverted Data Latched

Note 1 Qn is the parallel output of the shift register (n = 1 to 64). Qn takes the value of serial input (SIN) after "n" shift clock periods.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Logic Supply Range	-0.3, +7	V
V_{PP}	Driver Supply Range	-0.3, +170	V
V_{IN}	Logic Input Voltage Range	-0.3, V_{CC} +0.3	V
V_{OUT}	Logic Output Voltage Range	-0.3, V_{CC} + 0.3	V
V_{POUT}	Driver Output Voltage Range	-0.3, V_{PP}	V
I_{POUT}	Driver Output Current (3) (5)	+100/-400	mA
I_{DOUT}	Diode Output Current (4) (5)	±700	mA
T_{jmax}	Operating Temperature	-20, +85	°C
T_{oper}	Junction Temperature (2)	+125	°C
T_{stg}	Storage Temperature	-50,+150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance (2)	Max	50	°C/W
P_{oper}	Operating Power Dissipation (T_{amb} = 25°C)	Max	2	W
T_{joper}	Operating Junction Temperature (2)	Max	+125	°C

Note 2 For PQFP100 packaging.

Note 3 Through one power output.

Note 4 Through one power output with $V_{PP} = V_{SSP}$ (see test diagram).

Note 5 These parameters are measured during ST's internal qualification which includes temperature characterisation on standard batches and on corners batches of the process. These parameters are not tested on the parts.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, V_{PP} = 160 V, V_{SSP} = 0 V, V_{SSLOG} = V_{SSSUB} = 0 V, T_{amb} = 25°C, f_{CLK} = 20 MHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Logic Supply Voltage		4.5	5	5.5	V
I_{CCH}	Logic Supply Current (all inputs high)		-	-	100	µA
I_{CCL}	Logic Supply Current	f_{CLK} = 8 MHz, SIN = 1010	-	5.3	-	mA
V_{PP}	Power Output Supply Voltage		15	-	160	V
I_{PPH}	Power Output Supply Current (steady outputs)		-	-	100	µA
OUTPUT						
OUT1-OUT64						
V_{POUTH}	Power Output High Level (voltage drop versus V_{PP})	I_{POUTH} = - 10 mA I_{POUTH} = - 40 mA	10 -	- 5	- -	V V
V_{POUTL}	Power Output Low Level	I_{POUTL} = 200 mA	-	3.1	10	V
V_{DOUTH}	Output Diode High Level	I_{DOUTH} = +400 mA (5)	-	2.3	10	V
V_{DOUTL}	Output Diode Low Level	I_{DOUTL} = - 400 mA (5)	-10	-2.2	-	V
SOUT						
V_{OH}	Logic Output High Level	I_{OH} = 1 mA	4	-	-	V
V_{OL}	Logic Output Low Level	I_{OL} = -1 mA	-	-	0.4	V
INPUT (CLK, F/ R , $\overline{STB}$, POL, BLK, SIN,)						
V_{IH}	Input High Level		0.8 V_{CC}	-	-	V
V_{IL}	Input Low Level		-	-	0.2V_{CC}	V
I_{IH}	High Level Input Current	V_{IH} = V_{CC}	-	-	10	µA
I_{IL}	Low Level Input Current CLK, SIN, $\overline{STB}$, F/ R , BLK, POL	V_{IL} = 0 V	- -	- 70	10 100	µA µA

Note 6 Compatible with power dissipation (see test diagram).

AC TIMINGS REQUIREMENTS

(V_{CC} = 4.5 V to 5.5 V, T_{amb} = -20 to +85°C, input signals max leading edge & trailing edge (t_R, t_F) = 10 ns)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data Clock Period	50	-	-	ns
t_{WHCLK}	Duration of clock (CLK) pulse at high level	15	-	-	ns
t_{WHCLK}	Duration of clock (CLK) pulse at low level	15	-	-	ns
t_{SDAT}	Set-up Time of data input before clock low to high transition	10	-	-	ns
t_{HDAT}	Hold Time of data input after clock low to high transition	10	-	-	ns
t_{SFR}	Forward/$\overline{\text{reverse}}$ (F/$\overline{R}$) Set-up Time before low to high transition	100	-	-	ns
t_{DSTB}	Minimum Delay to latch $\overline{\text{STB}}$ after clock low to high transition	10	-	-	ns
t_{STB}	Strobe $\overline{\text{STB}}$ Pulse Duration	20	-	-	ns
t_{BLK}	Blank (BLK) Pulse Duration	500	-	-	ns
t_{POL}	Polarity (POL) Pulse Duration	500	-	-	ns

AC TIMINGS CHARACTERISTICS

(V_{CC} = 5 V, V_{PP} = 90 V, V_{SSP} = 0 V, V_{SSLOG} = V_{SSSUB} = 0 V, T_{amb} = 25°C, f_{CLK} = 20 MHz, $V_{ILMax.}$ = 0.2 Vcc, $V_{IHMin.}$ = 0.8 V_{CC}, V_{OH} = 4.0 V, V_{OL} = 0.4 V, C_L = 15pF, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data Clock Period	50	-	-	ns
t_{RDAT}	Logical Data Output Rise Time	-	20	-	ns
t_{FDAT}	Logical Data Output Fall Time	-	11	-	ns
t_{PHL1}	Delay of logic data output after clock (CLK) high to low transition	-	45	80	ns
t_{PLH1}	Delay of logic data output after clock (CLK) low to high transition	-	48	80	ns
t_{PHL2}	Delay of power output change after clock (CLK) high to low transition	-	120	180	ns
t_{PLH2}	Delay of power output change after clock (CLK) low to high transition	-	120	180	ns
t_{PHL3}	Delay of power output change after blanking (BLK) high to low transition	-	110	165	ns
t_{PLH3}	Delay of power output change after blanking (BLK) low to high transition	-	110	165	ns
t_{PHL4}	Delay of power output change after polarity (POL) high to low transition	-	-	160	ns
t_{PLH4}	Delay of power output change after polarity (POL) low to high transition	-	-	160	ns
t_{ROUT}	Power Output Rise Time (7)	-	100	200	ns
t_{FOUT}	Power Output Fall Time (7)	-	60	200	ns

Note 7 One output among 64, loading capacitor C_{OUT} = 100pF, other outputs at low level.

Figure 1. AC Characteristics Waveform

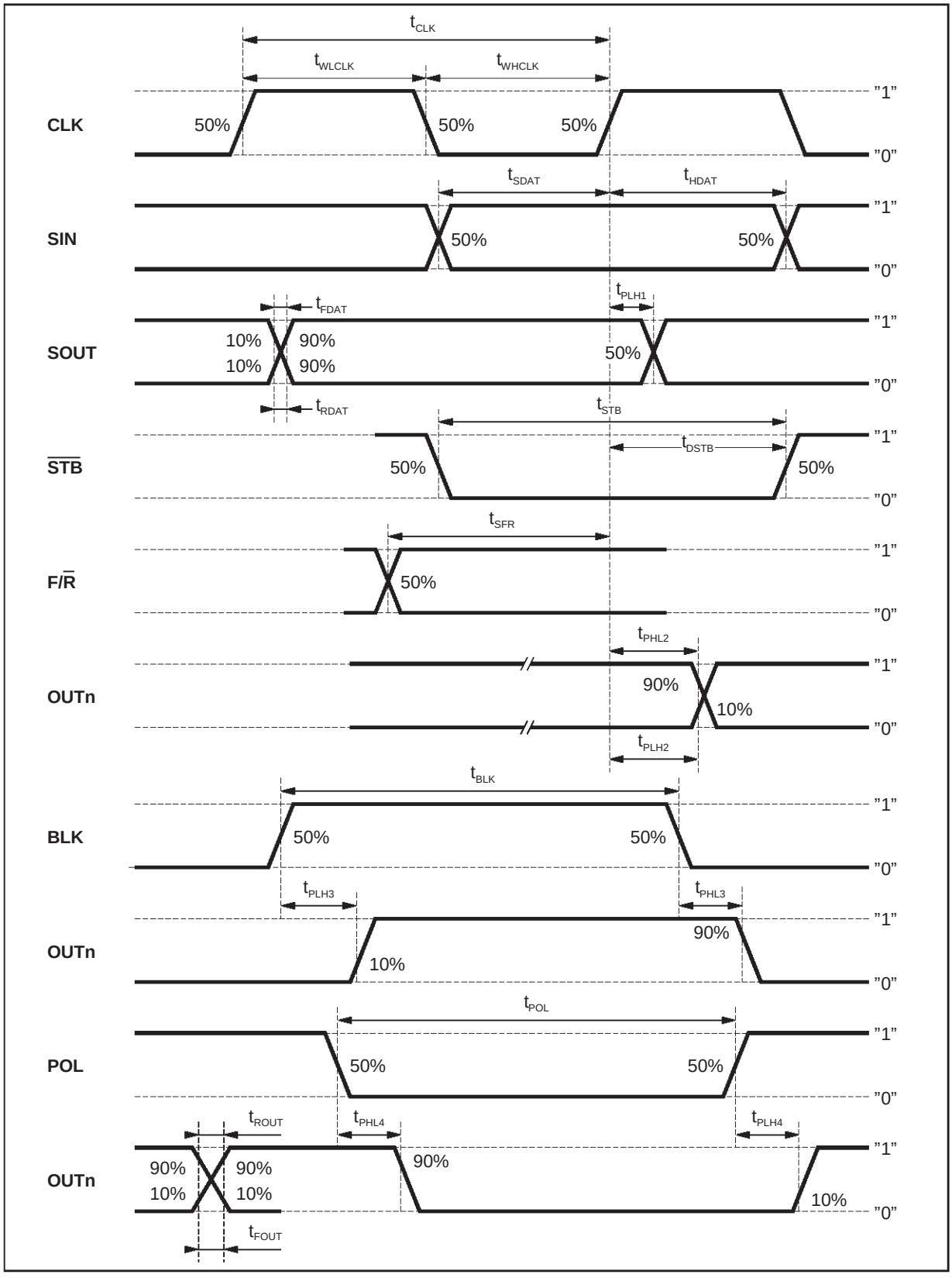
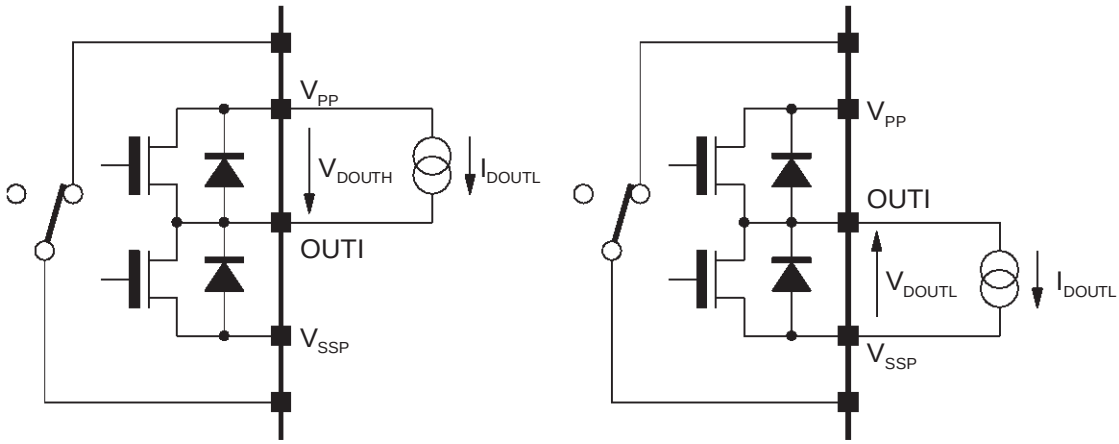


Figure 2. Test Configuration



Output sinking current as positive value, sourcing current as negative value

INPUT/OUTPUT SCHEMATICS

Figure 3. F/$\overline{R}$, BLK, POL, HIZ

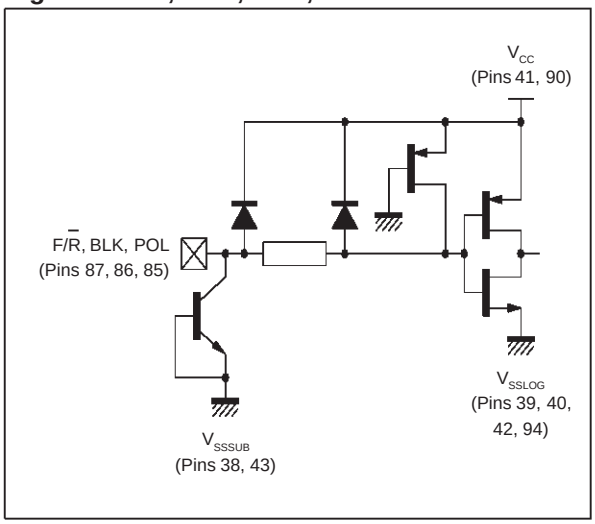


Figure 4. CLK, $\overline{STB}$

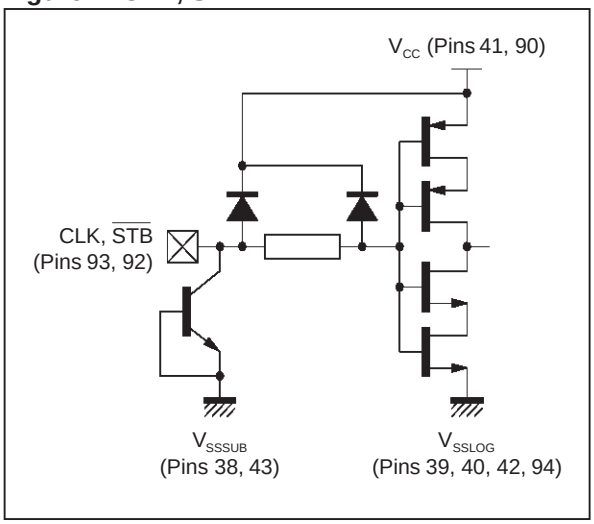


Figure 5. SIN, SOUT Input

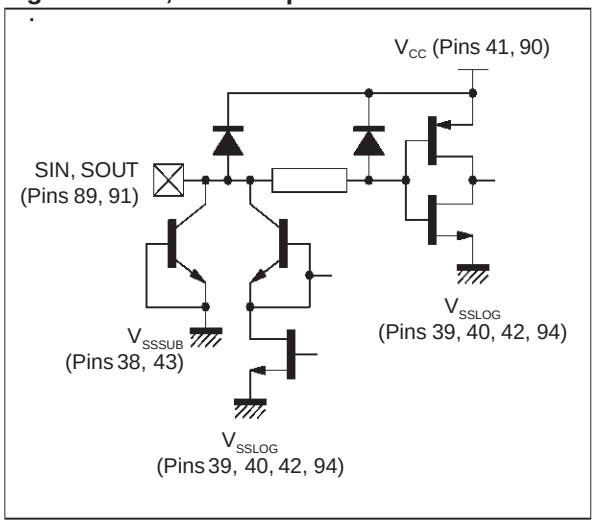
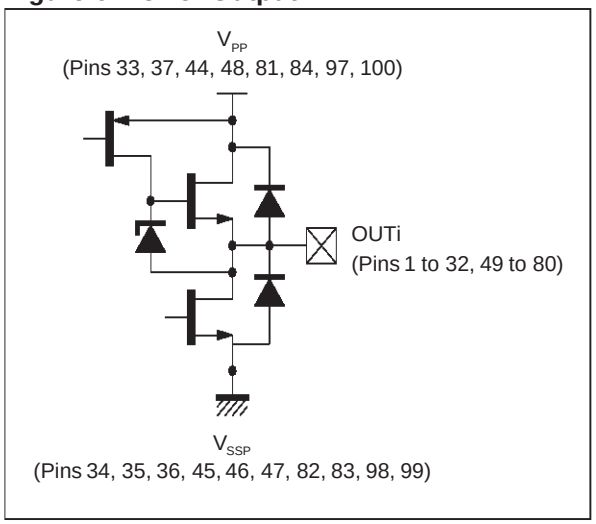
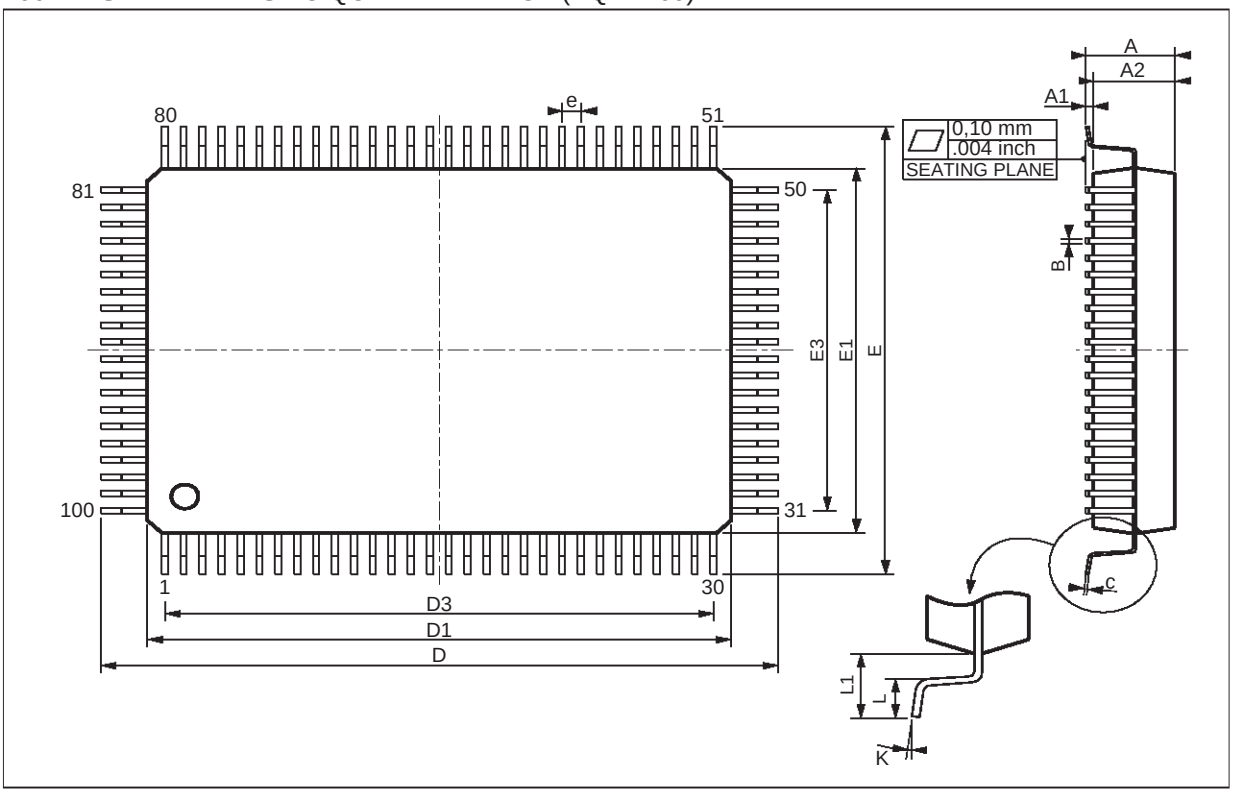


Figure 6. Power Output



PACKAGE MECHANICAL DATA

100 PINS - THIN PLASTIC QUAD FLAT PACK (PQFP100)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.22		0.38	0.0087		0.015
C	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.903	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.85			0.742	
e		0.65			0.026	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.35			0.486	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0° (Min.), 7° (Max.)					