
BB305M

Build in Biasing Circuit MOS FET IC
UHF/VHF RF Amplifier

HITACHI

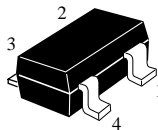
ADE-208-607C (Z)
4th. Edition
May 1998

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Superior cross modulation characteristics.
- High gain; (PG = 28 dB typ. at f = 200 MHz)
- Wide supply voltage range;
Applicable with 5V to 9V supply voltage.
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; MPAK-4(SOT-143mod)

Outline

MPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

- Note: 1. Marking is "EW-".
2. BB305M is individual type number of HITACHI BBFET.

BB305M

Absolute Maximum Ratings (Ta = 25°C)

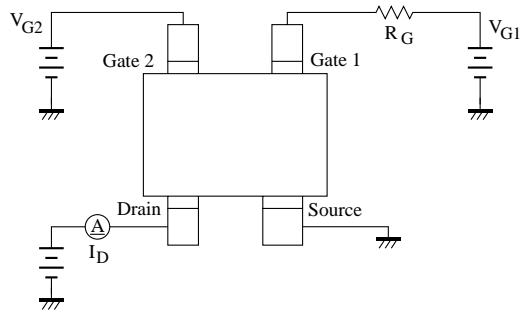
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	12	V
Gate1 to source voltage	V_{G1S}	+10 -0	V
Gate2 to source voltage	V_{G2S}	±10	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Electrical Characteristics (Ta = 25°C)

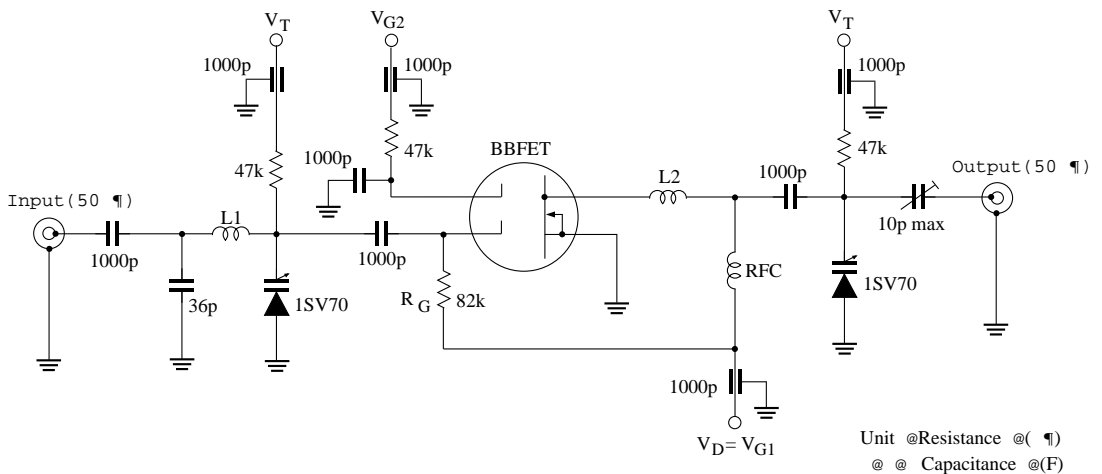
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	12	—	—	V	$I_D = 200\mu A, V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+10	—	—	V	$I_{G1} = +10\mu A, V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	± 10	—	—	V	$I_{G2} = \pm 10\mu A, V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +9V, V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	± 100	nA	$V_{G2S} = \pm 9V, V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.4	—	1.0	V	$V_{DS} = 5V, V_{G2S} = 4V, I_D = 100\mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	—	1.0	V	$V_{DS} = 5V, V_{G1S} = 5V, I_D = 100\mu A$
Input capacitance	C_{iss}	2.3	2.8	3.5	pF	$V_{DS} = 5V, V_{G1} = 5V$
Output capacitance	C_{oss}	1.1	1.5	1.9	pF	$V_{G2S} = 4V, R_G = 82k\Omega$
Reverse transfer capacitance	C_{rss}	—	0.017	0.04	pF	$f = 1MHz$
Drain current	$I_{D(op) 1}$	10	15	20	mA	$V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V$ $R_G = 82k\Omega$
	$I_{D(op) 2}$	—	13	—	mA	$V_{DS} = 9V, V_{G1} = 9V, V_{G2S} = 6V$ $R_G = 220k\Omega$
Forward transfer admittance	$ y_{fs} 1$	23	28	—	mS	$V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V$ $R_G = 82k\Omega, f = 1kHz$
	$ y_{fs} 2$	—	28	—	mS	$V_{DS} = 9V, V_{G1} = 9V, V_{G2S} = 6V$ $R_G = 220k\Omega, f = 1kHz$
Power gain	PG1	24	28	—	dB	$V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V$ $R_G = 82k\Omega, f = 200MHz$
	PG2	—	28	—	dB	$V_{DS} = 9V, V_{G1} = 9V, V_{G2S} = 6V$ $R_G = 220k\Omega, f = 200MHz$
Noise figure	NF1	—	1.4	1.9	dB	$V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V$ $R_G = 82k\Omega, f = 200MHz$
	NF2	—	1.4	—	dB	$V_{DS} = 9V, V_{G1} = 9V, V_{G2S} = 6V$ $R_G = 220k\Omega, f = 200MHz$

Main Characteristics

Test Circuit for Operating Items ($I_{D(op)}$, y_{fs} , C_{iss} , C_{oss} , C_{rss} , NF , PG)

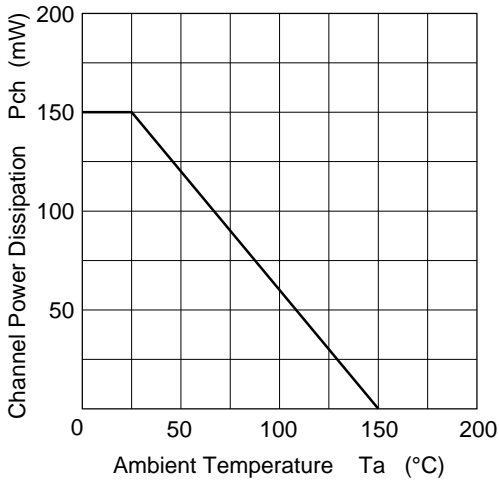


Power Gain, Noise Figure Test Circuit

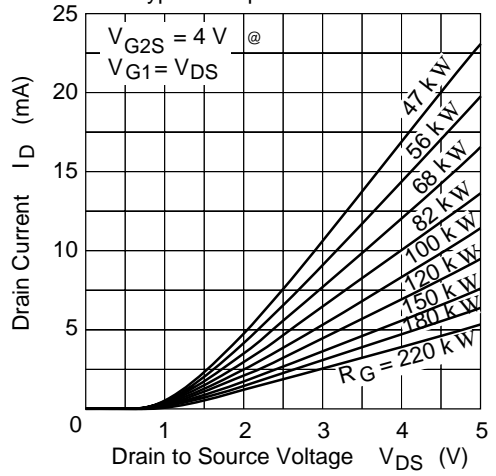


- L1 : 1mm Enameled Copper Wire, Inside dia 10mm, 2Turns
- L2 : 1mm Enameled Copper Wire, Inside dia 10mm, 2Turns
- RFC : 1mm Enameled Copper Wire, Inside dia 5mm, 2Turns

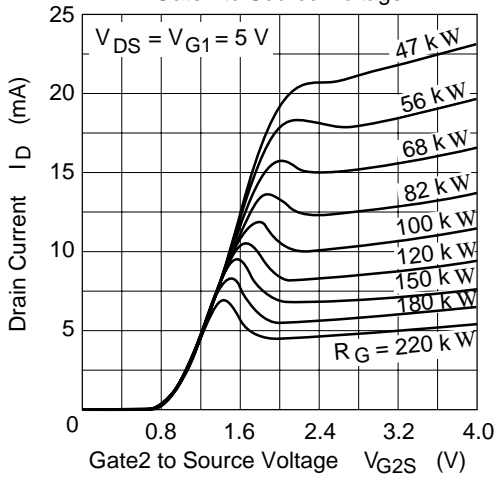
Maximum Channel Power Dissipation Curve



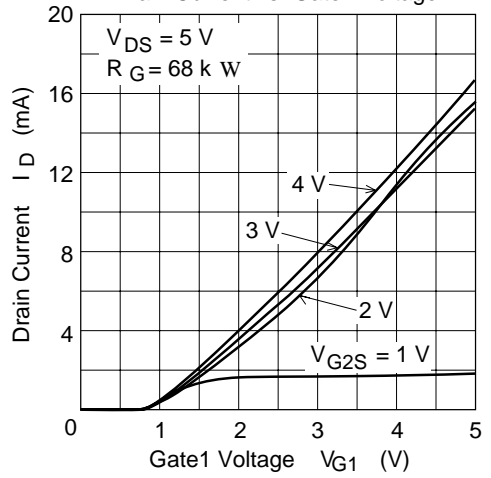
Typical Output Characteristics



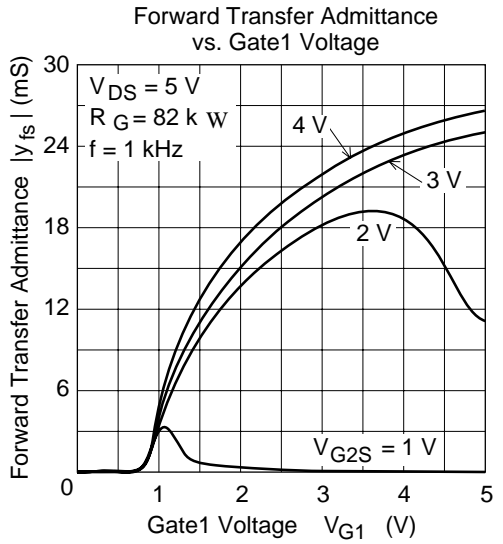
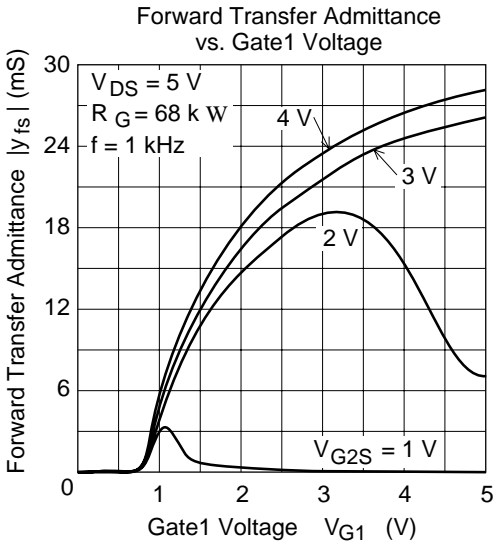
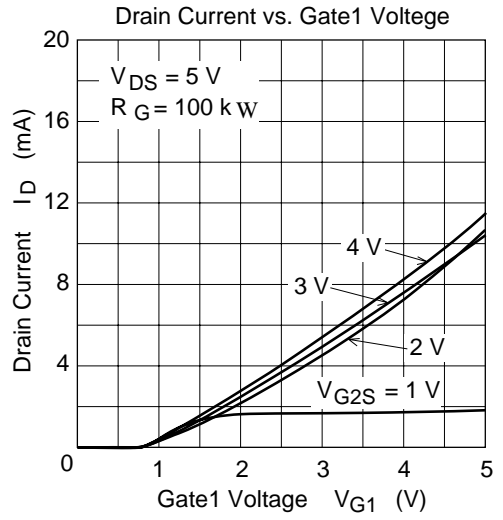
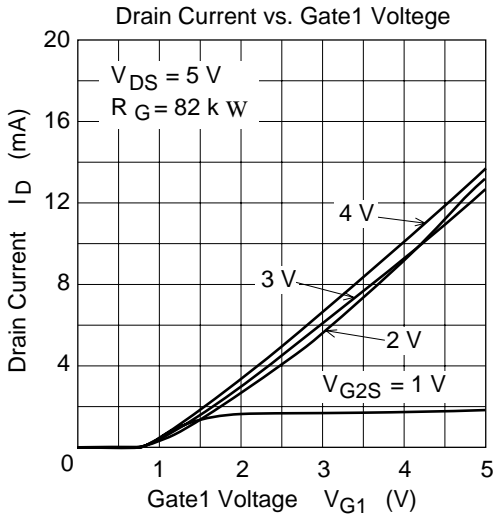
Drain Current vs. Gate2 to Source Voltage



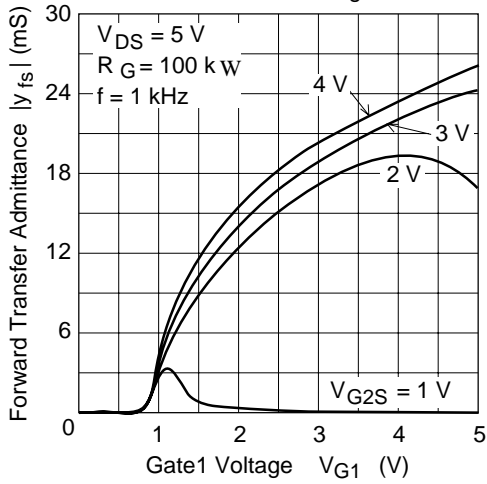
Drain Current vs. Gate1 Voltage



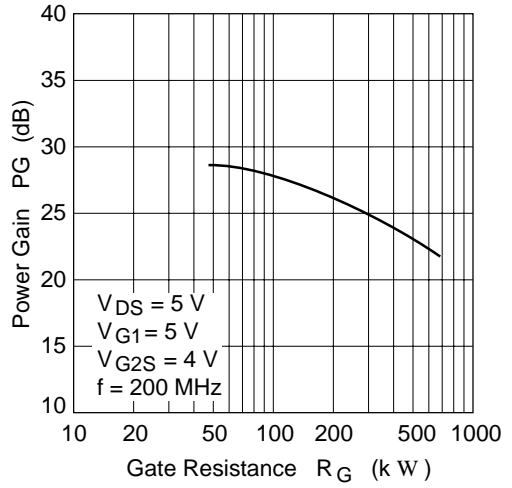
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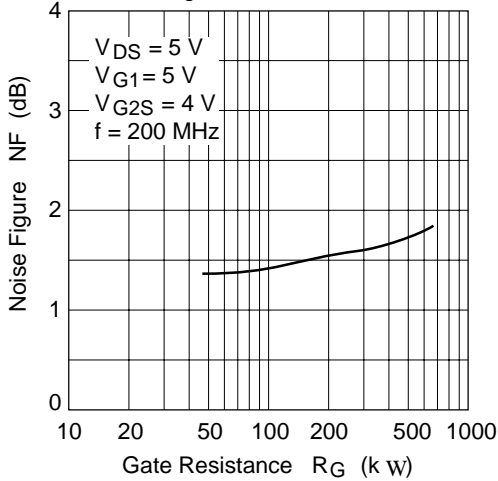
Forward Transfer Admittance vs. Gate1 Voltage



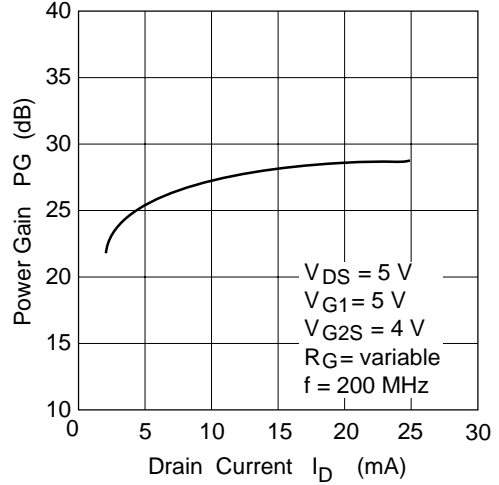
Power Gain vs. Gate Resistance

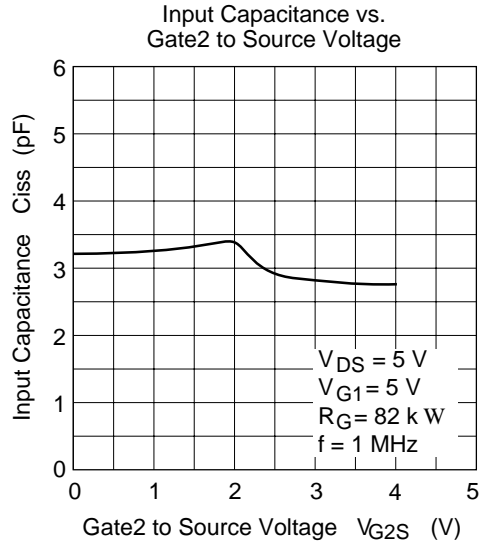
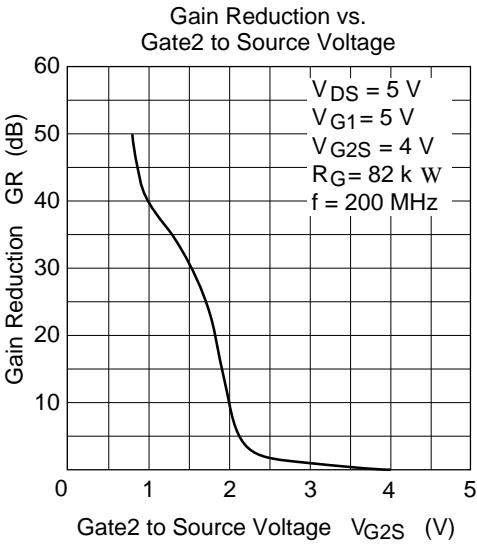
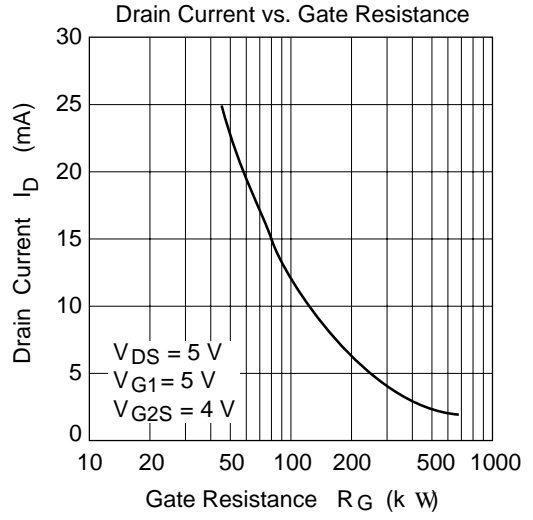
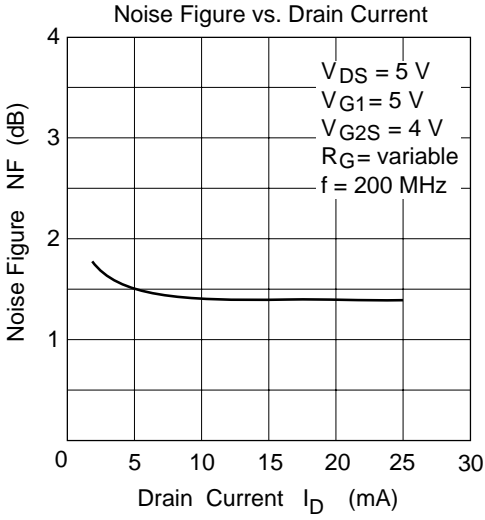


Noise Figure vs. Gate Resistance

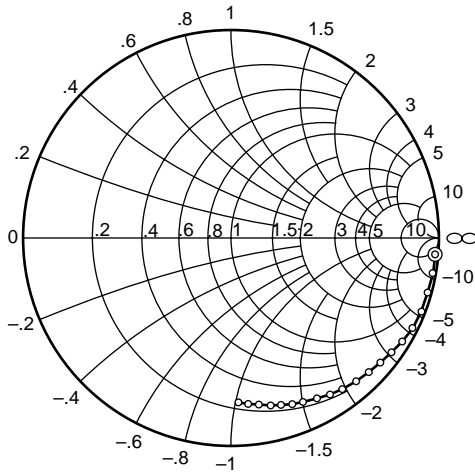


Power Gain vs. Drain Current



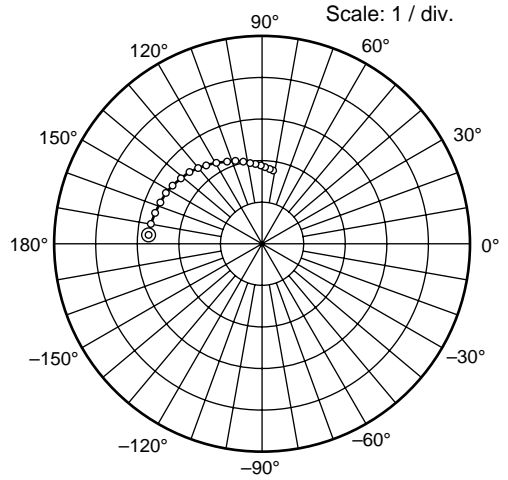


S11 Parameter vs. Frequency



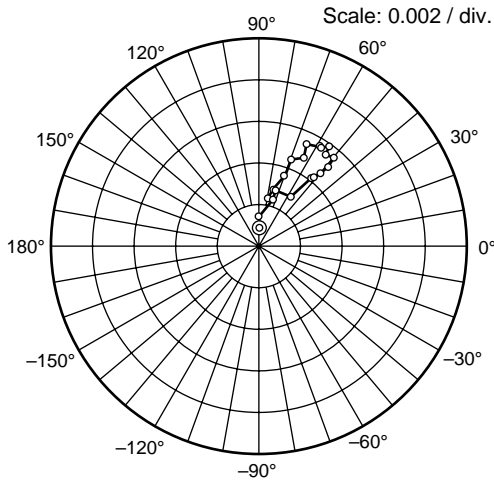
Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 50 ~ 1000 MHz (50 MHz step)

S21 Parameter vs. Frequency



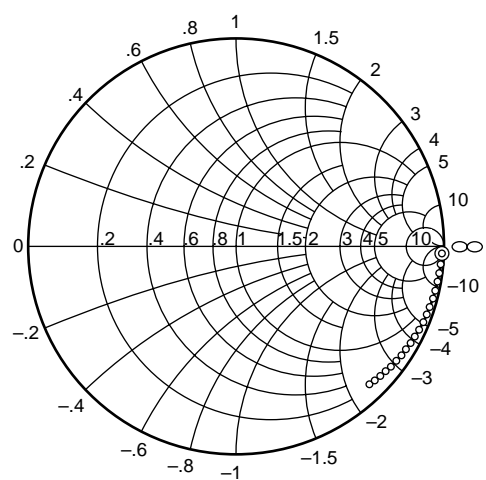
Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 50 ~ 1000 MHz (50 MHz step)

S12 Parameter vs. Frequency



Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 50 ~ 1000 MHz (50 MHz step)

S22 Parameter vs. Frequency



Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 50 ~ 1000 MHz (50 MHz step)

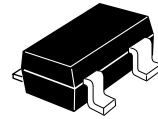
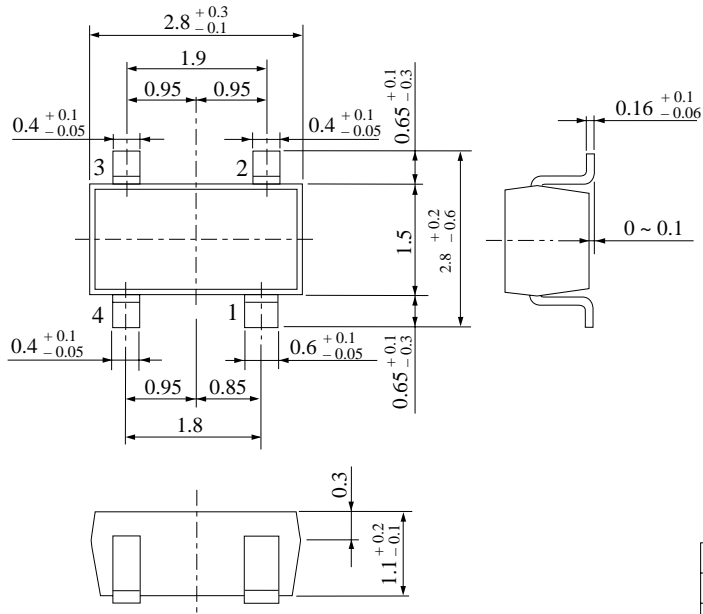
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Sparameter ($V_{DS} = V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 82k\Omega$, $Z_0 = 50\Omega$)

f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.991	-4.8	2.69	174.9	0.00090	91.4	0.991	-2.2
100	0.991	-9.9	2.68	169.3	0.00153	90.5	0.992	-4.8
150	0.982	-15.4	2.66	163.4	0.00243	73.8	0.991	-7.5
200	0.975	-20.7	2.62	157.5	0.00293	74.9	0.989	-9.9
250	0.972	-25.6	2.60	152.0	0.00370	70.1	0.985	-12.6
300	0.956	-30.6	2.54	146.3	0.00444	69.0	0.981	-15.0
350	0.942	-35.5	2.47	140.9	0.00478	63.7	0.977	-17.3
400	0.928	-40.1	2.42	135.7	0.00535	64.8	0.973	-19.7
450	0.920	-44.9	2.38	130.5	0.00551	56.8	0.967	-22.0
500	0.906	-49.2	2.32	125.7	0.00549	58.6	0.962	-24.5
550	0.894	-53.6	2.25	120.8	0.00584	54.4	0.957	-26.9
600	0.880	-57.8	2.18	116.2	0.00542	53.3	0.952	-29.2
650	0.868	-62.1	2.12	111.5	0.00562	49.5	0.944	-31.5
700	0.854	-66.2	2.06	106.8	0.00509	48.6	0.939	-33.8
750	0.842	-70.3	2.00	102.5	0.00465	49.7	0.933	-36.1
800	0.835	-73.9	1.94	98.4	0.00427	51.6	0.927	-38.3
850	0.820	-77.7	1.89	94.0	0.00416	53.3	0.921	-40.5
900	0.802	-81.5	1.83	89.6	0.00289	57.9	0.915	-42.7
950	0.801	-84.7	1.78	85.6	0.00288	72.9	0.909	-44.9
1000	0.789	-87.9	1.73	82.1	0.00241	78.9	0.904	-47.1

Package Dimensions

Unit: mm



Hitachi Code	MPAK-4
EIAJ	SC-61AA
JEDEC	—

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