2, 4 and 8 Multiplex LCD Driver

Features

- V 6118 2 is 2 way multiplex with 2 rows and 38 columns
- V 6118 4 is 4 way multiplex with 4 rows and 36 columns
- V 6118 8 is 8 way multiplex with 8 rows and 32 columns
- Low dynamic current, 150 µA max.
- Low standby current, 1 µA max. at 25 °C
- Voltage bias and mux signal generation on chip
- Display refresh on chip, 40 x 8 RAM for display storage
- Display RAM addressable as 8, 40 bit words
- Column driver only mode to have 40 column outputs
- Crossfree cascadable for large LCD applications
- Separate logic and LCD supply voltage pins
- Wide power supply range, V_{DD}: 2 to 6 V, V_{LCD}: 2 to 8 V
- BLANK function for LCD blanking on power up etc.
- Voltage bias inputs for applications with large pixel sizes
- Bit mapped
- Serial input / output
- Very low external component count
- -40 °C to +85 °C temperature range
- No busy states
- LCD updating synchronized to the LCD refresh signal
- QFP52 and TAB packages

Description

The V 6118 is a universal low multiplex LCD driver. The Version V 6118 2 drives two ways multiplex (two blackplanes) LCD, the version V 6118 4, four way multiplex LCD, and the V 6118 8, eight way multiplex LCD. The display refresh is handled on chip via a 40 x 8 bit RAM which holds the LCD content driven by the driver. LCD pixels (or segments) are addressed on a one to one basis with the 40 x 8 bit RAM (a set bit corresponds to an activated LCD pixel). The V 6118 has very low dynamic current consumption, 150 µA max., making it particularly attractive for portable and battery powered applications. The wide operating range on both the logic (V_{DD}) and the LCD (V_{LCD}) supply voltages offers much application flexibility. The LCD bias generation is internal. The voltage bias levels can also be provided externnally for applications having large pixels sizes. The V 6118 can be used as a column only driver for cascading in large display applications. In the column only mode, 40 column Outputs available to address the display. A BLANK function is provided to blank the LCD, useful at power up to hold the display blank until the microprocessor has updated the display RAM.

Applications

- Balances and scales
- Automotive displays
- Utility meters
- Large displays (public information panels etc.)
- Pagers
- Portable, battery operated products
- Telephones

Typical Operating Configuration

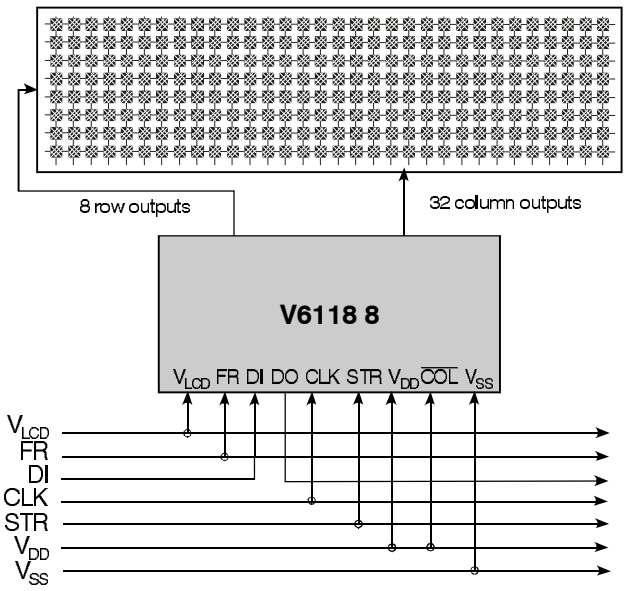
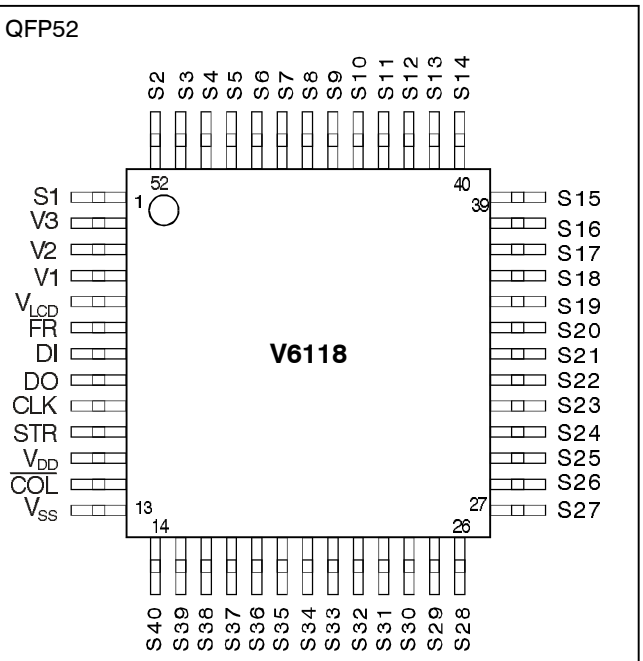


Fig. 1

Pin Assignment



See Fig.15 for the TAB pinout

Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	V_{DD}	-0.3V to +8V
LCD supply voltage range	V_{LCD}	-0.3V to +9V
Voltage at DI, CLK,DO, STR, FR, $\overline{COL}$	V_{LOGIC}	-0.3V to V_{DD}+0.3V
Voltage at V1 to V3, S1 to S40	V_{DISP}	-0.3V to V_{LCD}+0.3V
Storage temperature range	T_{STO}	- 65 to +150 °C
Power dissipation	P_{MAX}	100 mW
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{SMAX}	1000V
Max. soldering conditions	T_S	250 °C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	-40		+85	°C
Logic supply voltage	V_{DD}	2	5.0	6	V
LCD supply voltage	V_{LCD}	2	5.0	8	V

Table 2

Electrical Characteristics

V_{DD} = 5V $\pm$ 10%, V_{LCD} = 2 to 7 V and T_A = -40 to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Dynamic supply current	I_{LCD}	See note [1]		100	150	µA
Dynamic supply current	I_{DD}	See note [1] at T_A = + 25 °C		0.1	1	µA
Dynamic supply current	I_{DD}	See note [1]		3	12	µA
Dynamic supply current	I_{DD}	See note [2]		200	250	µA
Standby supply current	I_{SS}	See note [3] at T_A = + 25 °C		0.1	1	µA
Control Signals DI, CLK, STR, FR and $\overline{COL}$						
Input leakage	I_{IN}	$0 < V_{IN} < V_{DD}$		1	100	nA
Input capacitance	C_{IN}	at T_A = + 25 °C		8		pF
Low level input voltage	V_{IL}		0		0.8	V
High level input voltage for DI, STR, FR and $\overline{COL}$	V_{IH}		2.0		V_{DD}	V
High level input voltage for CLK	V_{IH}		3.0		V_{DD}	V
Data Output DO						
High level output voltage	V_{OH}	I_H = 4 mA	2.4			V
Low level output voltage	V_{OL}	I_L = 4 mA			0.4	V
Driver Outputs S1…S40						
Driver impedance [4]	R_{OUT}	I_{OUT} = 10 µA, V_{LCD} = 7 V		0.5	1.5	k Ω
Driver impedance [4]	R_{OUT}	I_{OUT} = 10 µA, V_{LCD} = 3 V		1.2	2.5	k Ω
Driver impedance [4]	R_{OUT}	I_{OUT} = 10 µA, V_{LCD} = 2 V		9		k Ω
Bias impedance V1, V2, V3 [5]	R_{BIAS}	I_{OUT} = 10 µA, V_{LCD} = 7 V		16	20	k Ω
Bias impedance V1, V2, V3 [5]	R_{BIAS}	I_{OUT} = 10 µA, V_{LCD} = 3 V		18	25	k Ω
Bias impedance V1, V2, V3 [5]	R_{BIAS}	I_{OUT} = 10 µA, V_{LCD} = 2 V		30		k Ω
DC output component	$\pm V_{DC}$	See tables 4a and 4b, V_{LCD} = 5 V		30	50	mV

Table 3

[1] All outputs open, STR at V_{SS}, FR = 400 Hz, all other inputs at V_{DD}.

[2] All outputs open, STR at V_{SS}, FR = 400 Hz, f_{CLK} = 1 MHz, all other inputs at V_{DD}.

[3] All outputs open, all inputs at V_{DD}.

[4] This is the impedance between the voltage bias level pins (V1, V2, or V3) and the output pins S1 to S40 when a given voltage bias level is driving the outputs (S1 to S40).

[5] This is the impedance seen at the segment pin. Outputs measured one at a time.

Column Drivers

Outputs	FR polarity	$\overline{COL}$	Column data	Measured	Guaranteed
S1 to S40	logic 1	logic 0	logic 1	$\lvert Sx^* - V_{SS} \rvert$	
S1 to S40	logic 0	logic 0	logic 1	$\lvert V_{LCD} - Sx^* \rvert$	$\lvert V_{LCD} - Sx^* \rvert = \lvert Sx^* - V_{SS} \rvert \pm 25mV$
S1 to S40	logic 1	logic 0	logic 0	$\lvert V_{LCD} - Sx^* \rvert$	
S1 to S40	logic 0	logic 0	logic 0	$\lvert Sx^* - V_{SS} \rvert$	$\lvert V_{LCD} - Sx^* \rvert = \lvert Sx^* - V_{SS} \rvert \pm 25$ mV

* Sx = the output no. (i.e. S1 to S40)

Table 4a

Row Drivers

Outputs	FR polarity	$\overline{COL}$	Row data	Measured	Guaranteed
S1 to Sn*	logic 1	logic 1	logic 1	$\lvert V_{LCD} - Sx \rvert$	
S1 to Sn*	logic 0	logic 1	logic 1	$\lvert Sx - V_{SS} \rvert$	$\lvert V_{LCD} - Sx \rvert = \lvert Sx - V_{SS} \rvert \pm 25mV$
S1 to Sn*	logic 1	logic 1	logic 0	$\lvert Sx - V_{SS} \rvert$	
S1 to Sn*	logic 0	logic 1	logic 0	$\lvert V_{LCD} - Sx \rvert$	$\lvert V_{LCD} - Sx \rvert = \lvert Sx - V_{SS} \rvert \pm 25$ mV

* n = the V 6118 version no. (i.e. 2, 4 or 8)

Table 4b

Timing Characteristics

V_{DD} = 5.0 V ± 10%, V_{LCD} = 2 to 8 V, and T_A = -40 to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		120			ns
Clock low pulse width	t_{CL}		120			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		20[1)]			ns
Data input hold time	t_{DH}		30[1)]			ns
Data output propagation	t_{PD}	C_{LOAD} = 50 pF			100	ns
STR pulse width	t_{STR}		100			ns
CLK falling to STR rising	t_P		10			ns
STR falling to CLK falling	t_D		200			ns
FR frequency (Vers. 2/4/8)	F_{FR}[2)]			128/256/512		Hz

[1)] $t_{DS} + t_{DH}$ minimum must be ≥ 100 ns. If t_{DS} = 20 ns then $t_{DH} \geq 80$ ns.

Table 5a

[2)] V 6118n. FR = n times the desired LCD refresh rate where n is the V 6118 version number.

V_{DD} = 2 to 6 V, V_{LCD} = 2 to 8 V, and T_A = -40 to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		500			ns
Clock low pulse width	t_{CL}		500			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		100[1)]			ns
Data input hold time	t_{DH}		150[1)]			ns
Data output propagation	t_{PD}	C_{LOAD} = 50 pF			400	ns
STR pulse width	t_{STR}		500			ns
CLK falling to STR rising	t_P		10			ns
STR falling to CLK falling	t_D		1			µs
FR frequency (Vers. 2/4/8)	F_{FR}[2)]			128/256/512		Hz

[1)] $t_{DS} + t_{DH}$ minimum must be ≥ 500 ns. If t_{DS} = 100 ns then $t_{DH} \geq 400$ ns.

Table 5b

[2)] V 6118n, FR = n times the desired LCD refresh rate where n is the V 6118 version number.

Timing Waveforms

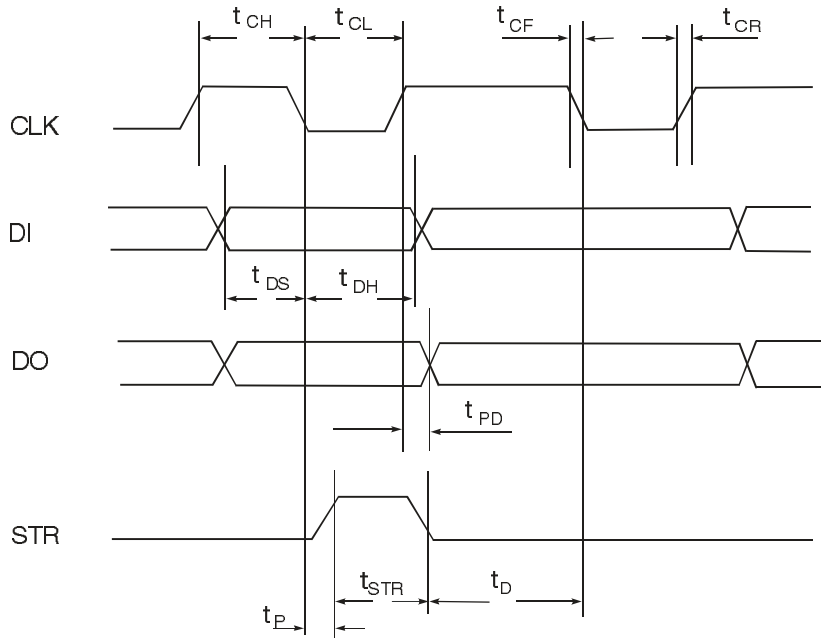
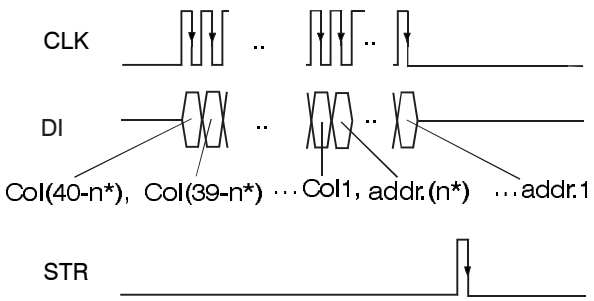


Fig. 3

V6118 Data Transfer Cycle, $\overline{COL}$ Inactive

V 6118 as a row and column driver ($\overline{COL}$ inactive)
40 bit load cycle, RAM address provided by address bit 1 to (n*)



* n = the V6118 version number (i.e. 2,4, or 8)

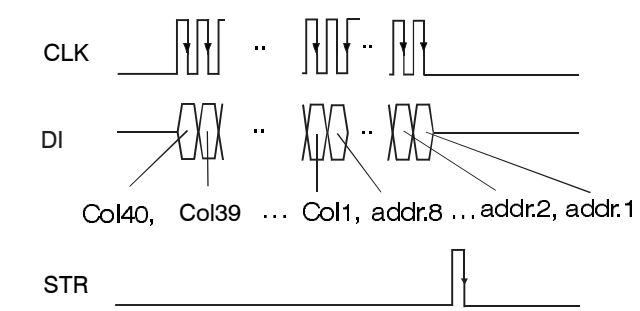
Address Bits			Display RAM	
V6118 2	V6118 4	V6118 8	Addr.	LCD row[1)]
Addr.1 to Addr.n*				
10	1000	10000000	10000000	Row1
01	0100	01000000	01000000	Row2
	0010	00100000	00100000	Row3
	0001	00010000	00010000	Row4
		00001000	00001000	Row5
		00000100	00000100	Row6
		00000010	00000010	Row7
		00000001	00000001	Row8

[1)] A set address bit corresponds to a write enabled RAM Address, the same data can be written to more than one RAM address by setting the required address bits.

Fig. 4

V6118 Data Transfer Cycle, $\overline{COL}$ Active

V 6118 as a column driver only ($\overline{COL}$ active)
48 bit load cycle, RAM address provided by address bits 1 to 8

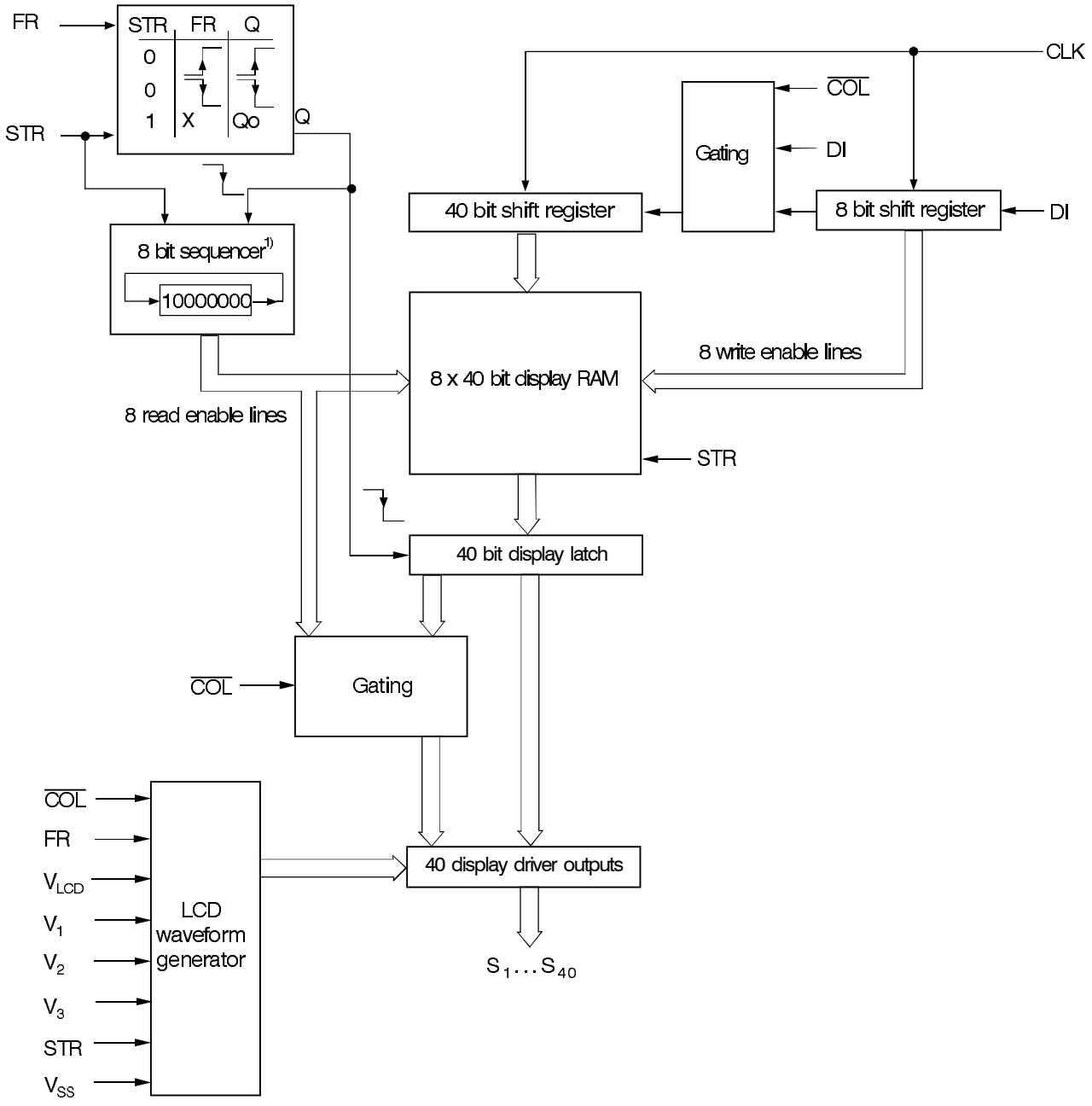


Address Bits			Display RAM	
V6118 2	V6118 4	V6118 8	Addr.	LCD row[1)]
Addr. 1 to Addr.8				
10000000	10000000	10000000	10000000	Row1
01000000	01000000	01000000	01000000	Row2
	00100000	00100000	00100000	Row3
	00010000	00010000	00010000	Row4
		00001000	00001000	Row5
		00000100	00000100	Row6
		00000010	00000010	Row7
		00000001	00000001	Row8

[1)] A set address bit corresponds to a write enabled RAM address,the same data can be written to more than one RAM address by setting the required address bits.

Fig. 5

Block Diagram



1) When logic "1" the STR input forces the display RAM addr. 10000000 (which corresponds to row 1) to be selected by the 8 bit sequences. Cascaded V6118s are synchronized in this way. The LCD picture is rebuilt starting from row 1 each time data is written to the display RAM.

Fig. 6

Pin Description

Name	Function
S1...S40	LCD outputs, see table 7
V3	LCD voltage bias level 3[1)2)]
V2	LCD voltage bias level 2[1)]
V1	LCD voltage bias level 1[1)]
V_{LCD}	Power supply for the LCD
FR	AC input signal for LCD driver outputs
DI	Serial data input
DO	Serial data output
CLK	Data clock input
STR	Data strobe, blank, synchronize input
V_{DD}	Power supply for logic
$\overline{COL}$	Column only driver mode
V_{SS}	Supply GND

Table 6

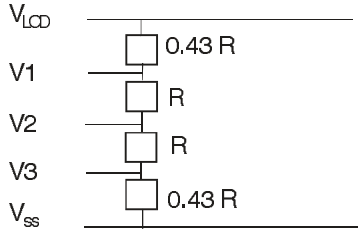
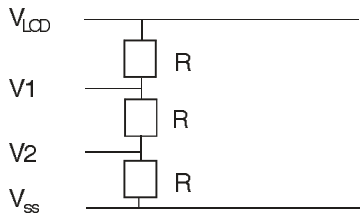
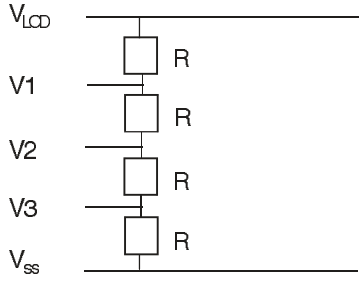
[1)] The V6118 has internal voltage bias level generation. When driving large pixels, an external resistor divider chain can be connected to the voltage bias level inputs to obtain enhanced display contrast (see Fig. 12, 13 and 14). The external resistor divider ratio should be in accordance with the internal resistor ratio (see table 8).

[2)] V3 is connected internally on the V6118 4.

Name	$\overline{COL}$ Inactive			$\overline{COL}$ Active
	V6118 2	V6118 4	V6118 8	
S1	Row1	Row1	Row1	Col1
S2	Row2	Row2	Row2	Col2
S3	Col1	Row3	Row3	Col3
S4	Col2	Row4	Row4	Col4
S5	Col3	Col1	Row5	Col5
S6	Col4	Col2	Row6	Col6
S7	Col5	Col3	Row7	Col7
S8	Col6	Col4	Row8	Col8
S9...S40	Col7....38	Col5....36	Col1....32	Col 9....40

Table 7

LCD Voltage Bias Levels

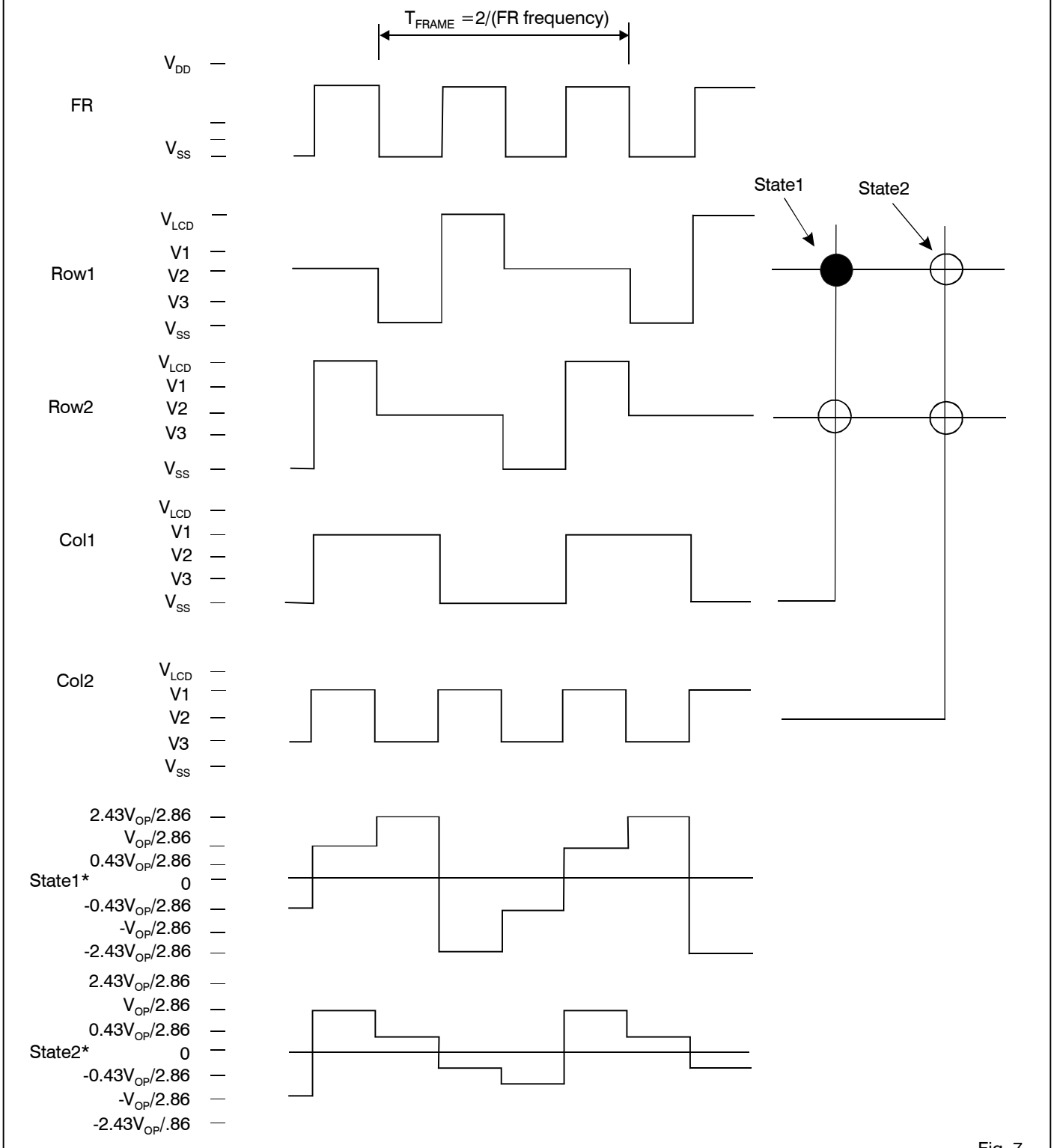
	LCD Drive Type	LCD Bias Configuration	$\frac{V_{OP}\ (*)}{V_{OFF}\ (rms)}$	$\frac{V_{ON}\ (rms)}{V_{OFF}\ (rms)}$
	V6118 2 n = 2 1:2MUX	Alt + Pleshko 5 levels	$\sqrt{\frac{2n}{1-\sqrt{\frac{1}{n}}}} = 3.69$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 2.41$
	V6118 4 n = 4 1:4 MUX	1/3 Bias 4 levels	3	$\sqrt{1+\frac{8}{n}} = 1.73$
	V6118 8 n = 8 1:8 MUX	1/4Bias 5 levels	$\frac{4}{\sqrt{1+\frac{3}{n}}} = 3.4$	$\sqrt{\frac{n+15}{n+3}} = 1.446$

(*) $V_{OP} = V_{LCD} - V_{SS}$

Table 8

Row and Column Multiplexing Waveform V6118 2

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

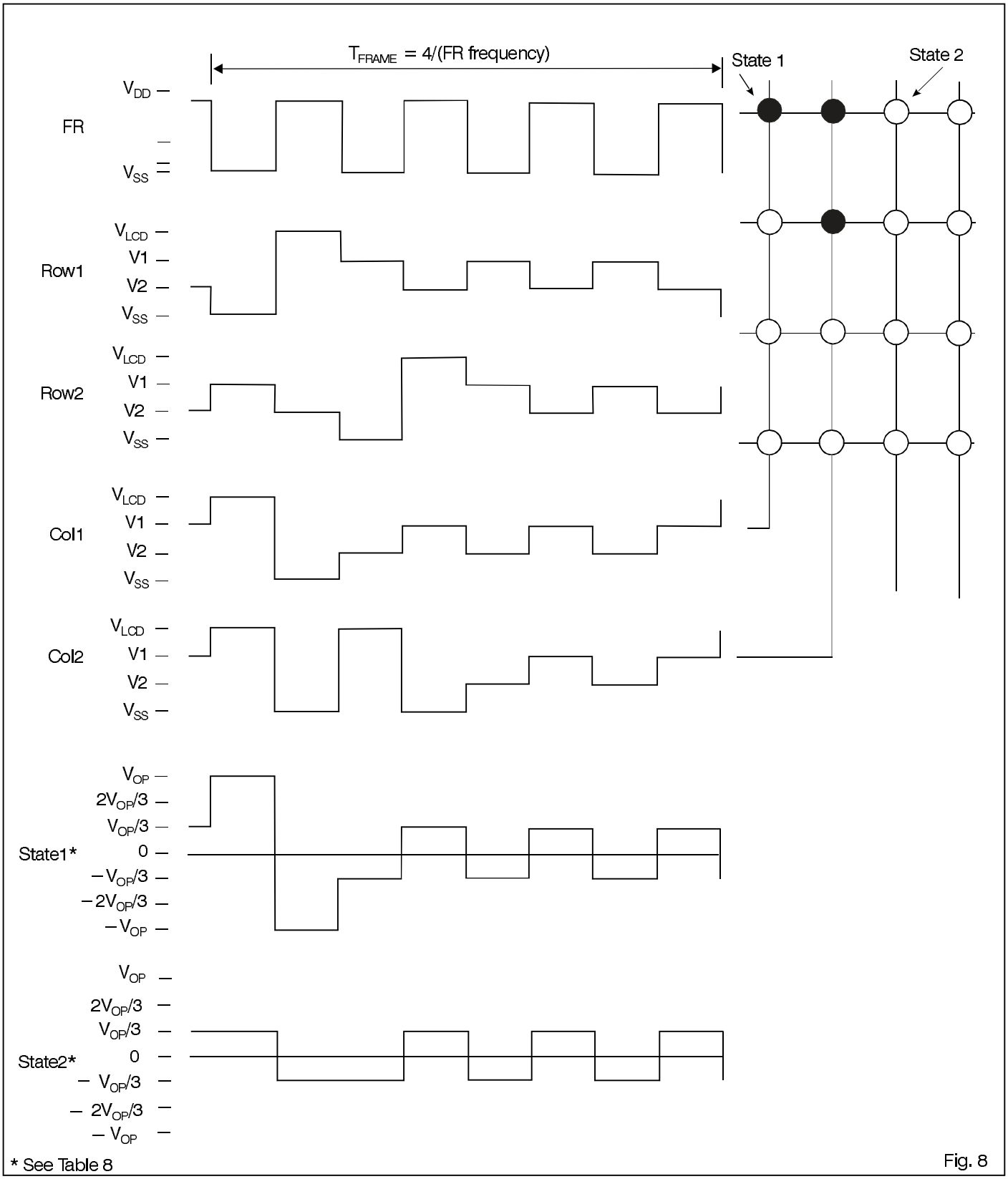


*See Table 8

Fig. 7

Row and Column Multiplexing Waveform V6118 4

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

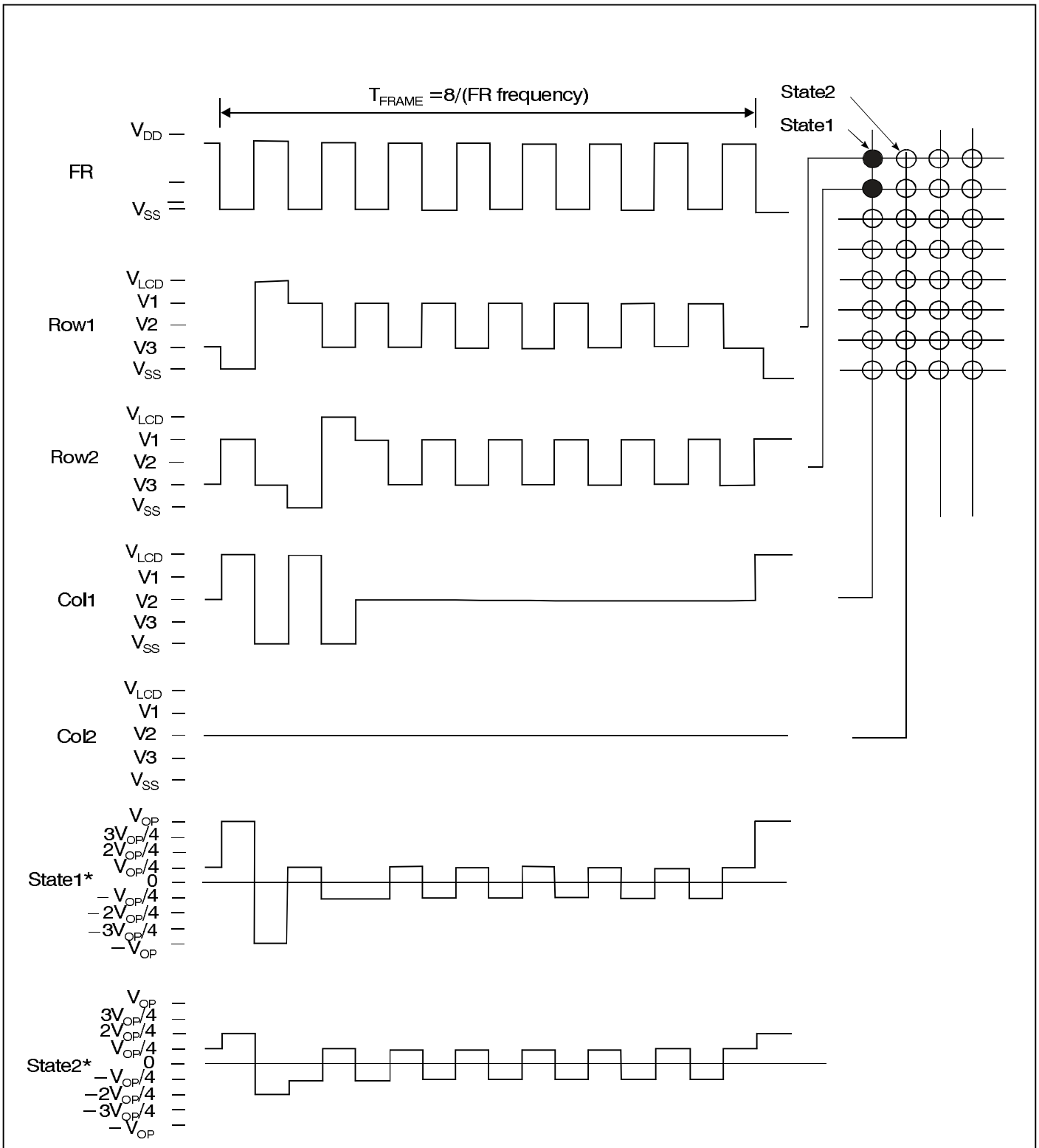


* See Table 8

Fig. 8

Row and Column Multiplexing Waveform V6118 8

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$



* See Table 8

Fig. 9

Functional Description

Supply Voltage V_{LCD}, V_{DD}, V_{SS}

The voltage between V_{DD} and V_{SS} is the supply voltage for the logic and the interface. The voltage between V_{LCD} and V_{SS} is the supply voltage for the LCD and is used for the generation of the internal LCD bias levels. The internal LCD bias levels have a maximum impedance of 25 kΩ for a V_{LCD} voltage from 3 to 8 V. Without external connections to the V1, V2, and V3 bias level inputs, the V 6118 can drive mostmedium sized LCD (pixel area up to 4'000 mm^2).

For displays with a wide variation in pixel sizes the configuration shown in Fig. 13 can give enhanced contrast by giving faster pixel switching times. On changing the row polarity (see Fig. 7, 8 and 9) the parallel capacitors lower the impedance of the bias level generation to the peak current, giving faster pixel charge times and thus a higher RMS "on" value. A higher RMS "on" value can give better contrast. If for a given LCD size and operating voltage, the "off" pixels appear "on", or there is poor contrast, then an external bias level generation circuit can be used with the V 6118. An external bias level generation circuit can lower the bias level impedance and hence improve the LCD contrast (see Fig. 12). The optimum values of R, Rx, and C, vary according to the LCD size used and V_{LCD}. They are best determined through actual experimentation with the LCD.

For LCD with every large average pixel size up to 10'000 mm^2, the bias level configuration shown in Fig. 14 should be used.

When V 6118s are cascaded connect the V1, V2, and V3 bias inputs are shown in Fig. 10. The pixel load is averaged across all the cascaded drivers. This will give enhanced display contrast as the effective bias level source impedance is the parallel combination of the total number of drivers. For example, if two V 6118 are cascaded as shown in Fig. 10, then the maximum bias level impedance becomes 12.5 KΩ for a V_{LCD} voltage from 3 to 8 V. Table 8 shows the relationship between V1, V2, and V3 for multiplex rates 2, 4 and 8. Note that $V_{LCD}>V1>V2>V3$ for the V 6118 2 and V 6118 8, and for the V 6118 4, $V_{LCD}>V1>V2$.

Data Input/ Output

The data input pin, DI, is used to load serial data into the V 6118. The serial data word length is 40 bits when $\overline{COL}$ is inactive, and 48 bits when it is active. Data is loaded in inverse numerical order, the data for bit 40 (bit 48 when $\overline{COL}$ is active) is loaded first with the data for bit 1 last. The column data bits are loaded first and then the address bits (see Fig. 4 and 5).

The data output pin, DO, is used in cascaded applications (see Fig. 10). DO transfers the data to the next cascaded chip. The data at DO is equal to the data at DI delayed by 40 clock periods, when $\overline{COL}$ is inactive and 48 clock periods when $\overline{COL}$ is active. In order to cascade V 6118s, DOofonechipmustbeconnected to DI of the following chip (see Fig. 10). In cascaded applications the data of the last V 6118 (the one that does not have DO connected) must be loaded first and the data for the first V6118 (its DI is connected to the processor) loaded last (see Fig. 10).

The display RAM word length is 40 bits (see Fig. 6). Each LCD row has a corresponding display RAM address which provides the column data (on or off) when the row is selected (on). When down loading data to the V 6118 any display RAM address can be chosen, there is no display RAM addressing sequence (see Fig. 4 and 5).

The same data can be written to more than one display RAM address. If more than one address bit is set, then more than one display RAM address is write enabled, and so the same data is written to more than one address. This feature can be useful to flash the LCD on and off under software control. If the address bits are all zero then no display RAM is write enabled and no data is written to the display RAM on the falling edge of STR. Use address 0 to synchronize cascaded V 6118s without updating the display RAM.

CLK Input

The CLK is used to clock the DI serial data into the shift register and to clock the DO serial data out. Loading and shifting of data occurs at the falling edge of this clock, outputting of the data at the rising edge (see Fig. 3). When cascading devices, all CLK lines should be tied together (see Fig. 10).

STR Input

The STR input is used to write to the display RAM, blank the LCD, and synchronize cascaded V 6118s. The STR input writes the data loaded into the shift register, on the DI input, to the display RAM on the falling edge of the STR signal. The display RAM address is given by the address bits (see Fig. 4 and 5).

The STR input when high blanks the LCD by disconnecting the internal voltage bias generation from the V_{SS} potential. Segment outputs S1 to S40 (rows and columns) are pulled up to V_{LCD}. The delay to driving the LCD with V_{LCD} on S1 to S40, is dependent on the capacitive load of the LCD and is typically 1 μs. An LCD pixel responds to RMS voltage and takes approximately 100 ms to turn on or off. The delay from putting STR high to the LCD being blank is dependent on the LCD off time and is typically 100 ms. In applications, which have a long STR pulse width (10 μs), the LCD is driven by V_{LCD} on both the rows and columns during this time. As the time is short (1 μA), it will have zero measurable effect on the RMS "on" value (over 100 ms) of an LCD pixel and also zero measurable effect on the pixel DC component. Such STR pulses will not be visible to the human eye on an LCD.

Note if an external voltage bias generation circuit is used as shown in Fig. 12 and 14, the LCD blank function (STR high) will not blank the LCD. When STR is high the LCD will be driven by the parallel combination of the external voltage bias generation circuit and part of the internal voltage bias generation circuit.

The STR input, when high, synchronizes cascaded V 6118s by forcing a new time frame to begin at the next falling edge of the FR input signal (see Fig.6). A time frame begins with row 1 and so the LCD picture is rebuilt from row 1 each time

cascaded V 6118s are synchronized. When cascading devices, all STR lines must be tied together (see Fig. 10).

FR input

The FR signal controls the segment output frequency generation (see Fig. 7,8 and 9). To avoid having DC on the display, the FR signal must have a 50% duty cycle. The frequency of the FR signal must be n times the desired display refresh rate, where n is the V 6118 version no. (2,4 or 8). For example, if the desired refresh rate is 40 Hz, the FR signal frequency must be 320 Hz for the V6118 8. A selected row (on) is in phase with the FR signal (see Fig. 7, 8 and 9).

It is recommended that data transfer to the V 6118 should be synchronized to the FR signal to avoid a falling or rising edge on the FR signal while writing data to the V 6118. The LCD pixels change polarity with the FR signal. On the edges of the FR signal current spikes will appear on the V_{SS} and V_{LCD} supply lines. If the supply lines have high impedance then voltage spikes will appear. These voltage spikes could interfere with data loading on the DI and CLK pins.

Driver output S1 to S40

There are 40 LCD driver outputs on the V 6118. When $\overline{COL}$ is inactive the outputs S1 to Sn function as row drivers and the outputs S(n + 1) to S40 function as column drivers, where n is the V 6118 version no. (2,4 or 8). When $\overline{COL}$ is active, all 40 outputs function as column drivers (see table 6). There is a one to one relationship between the display RAM and the LCD driver outputs. Each pixel (segment) driven by the V 6118 on the LCD has a display RAM bit which corresponds to it. Setting the bit turns the segment "on" and clearing it turns it "off".

$\overline{COL}$ Input

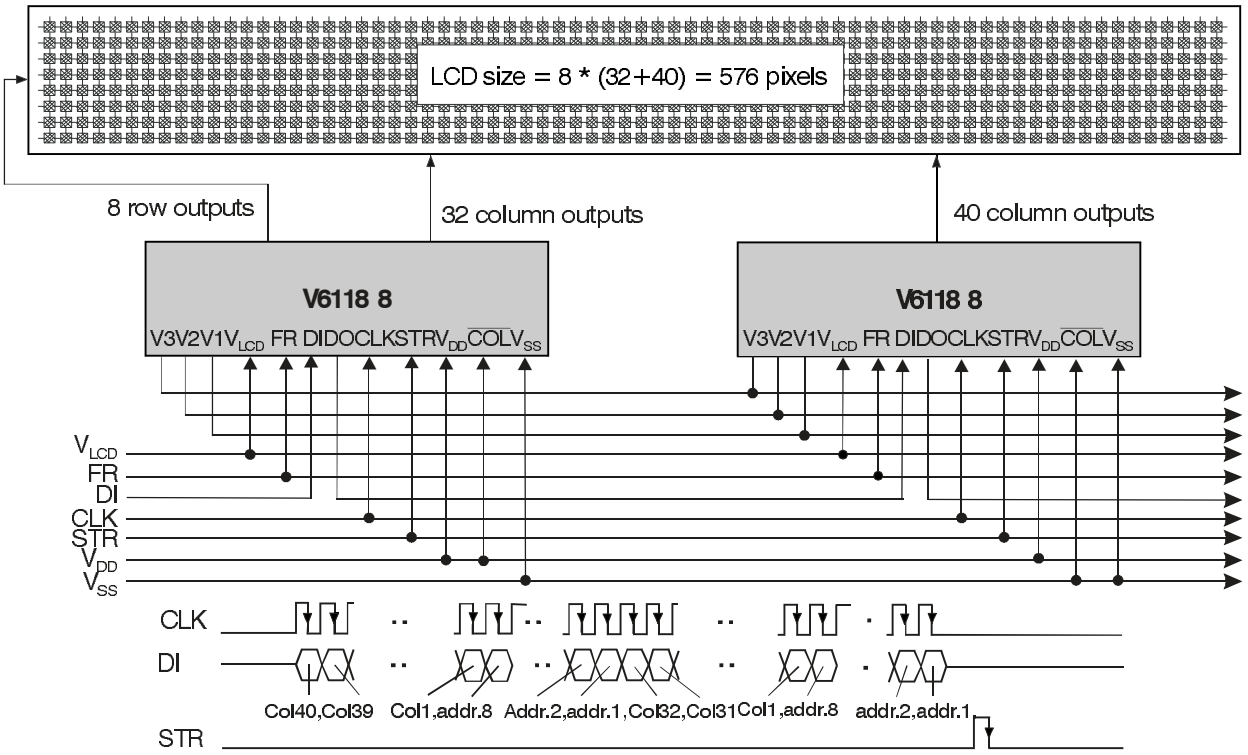
The V 6118 functions as a row and column driver while the $\overline{COL}$ is inactive. When active the $\overline{COL}$ input configures the V 6118 to function as a column driver only. The former row outputs function as column outputs. In cascaded applications one V6118 should be used in the row column configuration ($\overline{COL}$ inactive) and the rest as pure column drivers ($\overline{COL}$ active) (see Fig. 10). Note when cascading V 6118s never cascades one version with another. If a V6118 8 is used to drive the rows then only V 6118 8s can be cascaded with it. When $\overline{COL}$ is active the V 6118 needs 48 bits of data in a load cycle. 40 bits are used for the column data and 8 bits to address the display RAM regardless of V 6118 version (2, 4 or 8) (see Fig. 4, 5 and 10).

Power Up

On power up the data is shift registers, the display RAM and the 40-bit display latch are undefined. The STR input should be taken high on power up to blank the display, and then the display data written to the display RAM (see Fig. 11). When finished the initial write to the display RAM, take the STR input low to display the display RAM contents (see also section “STR Input").

Applications

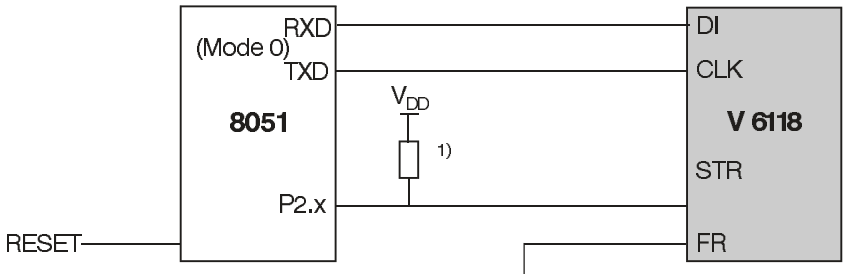
Two V6118 8s Cascaded



By connecting the V1, V2 and V3 bias inputs as shown, the pixel load is averaged across all the drivers. The sffective bias level source impedance is the parallel combination of the total number of drivers. For example, if two V 6118 are cascaded as above, then the maximum bias level impedance becomes 12. 5 kΩ .

Fig. 10

Microprocessor Interface and LCD Blanking



[1)]When themicroprocessor is reset, the port pin will be configured as an input and so the STR line would float. The pullup resistor will ensure that the LCD is blank while the system reset line is active and after until the port pin is setup by software.

Oscillator
50% duty cycle.

Writing Data to the Display RAM while Keeping the LCD Blank

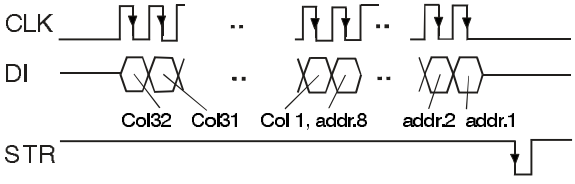
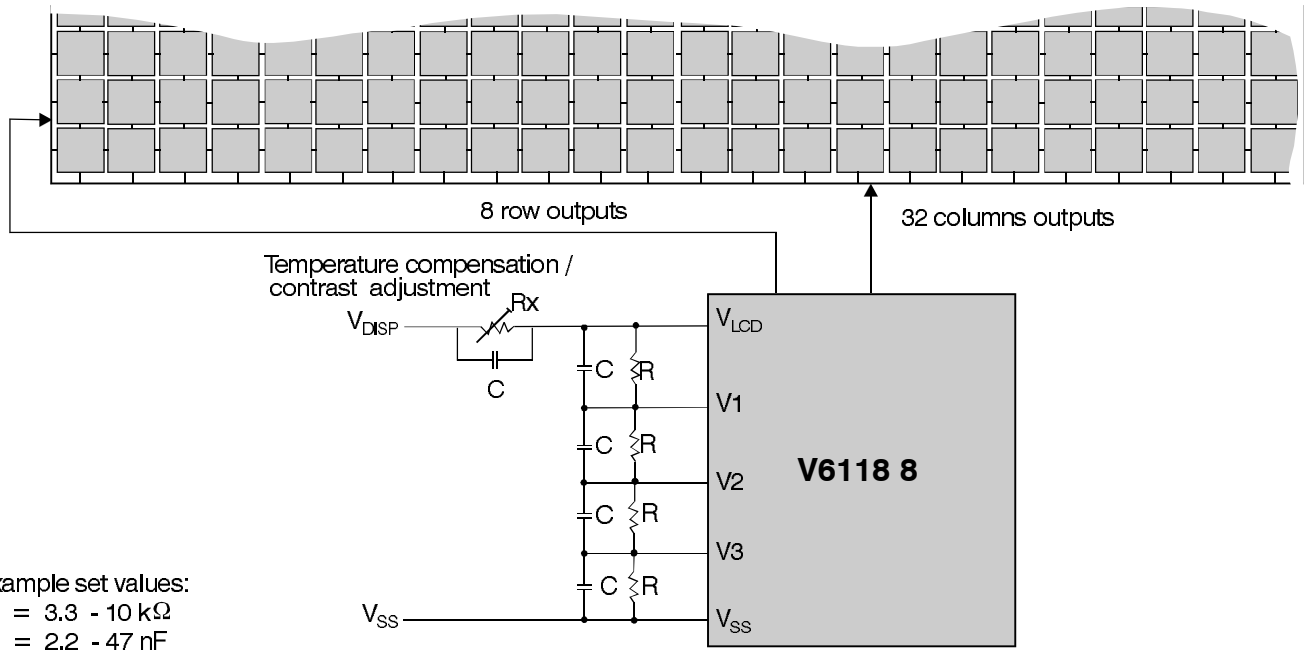


Fig. 11

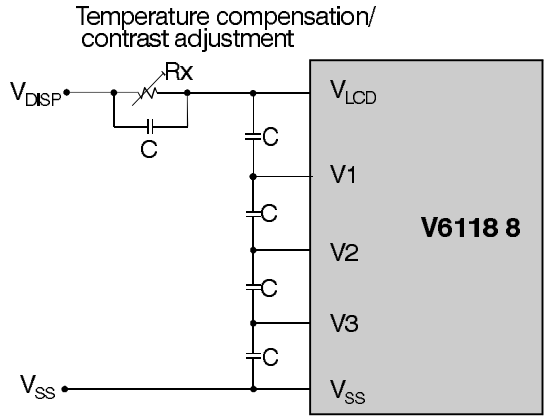
V 6118 with External Resistor Divider Bias Generation



Example set values:
R = 3.3 - 10 kΩ
C = 2.2 - 47 nF
Rx is given by the formula:
$Rx = 4R((V_{DISP}/V_{LCD})-1) = 10 - 30\ k\Omega$

Fig. 12

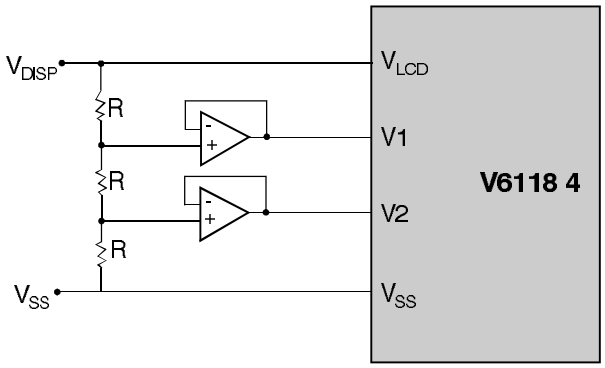
Enhanced Switching from the V 6118



C= 1 µF
Rx is given by the formula:
$Rx = 4\ (20\ k\Omega)\ ((V_{DISP}/V_{LCD}) - 1)$

Fig. 13

Bias Configuration for a Large LCD



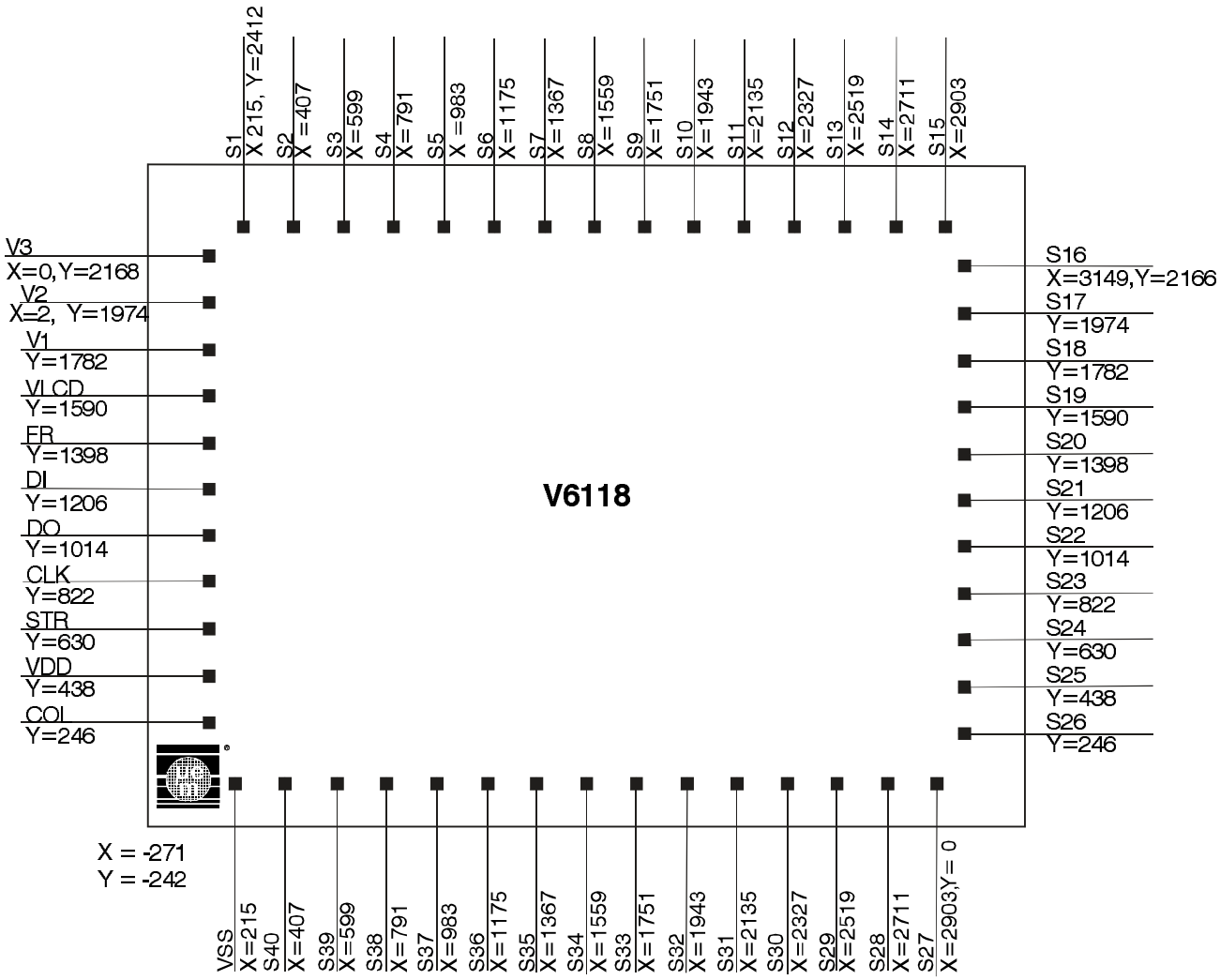
Large LCD example:
V_{OP}= 5 V, average pixel active area up to 10'000 mm^2
Display refresh = 64 Hz

For single V 6118 4 driving such an LCD the voltage follower buffer (opamp) requirements is:
peak current 1.8 mA,
steady state current typically 100 µA

Fig.14

Package and Ordering Informatiion

Dimensions of Chip Form



Thickness (typ.) = 11 mils. Chip size is X = 3657 by Y = 2895 microns or X = 144 by Y = 114 mils.
Note: The origin (0,0) is the lower left coordinate of center pads. The lower left corner of the chip shows distances to origin.

Dimensioms in microns

Fig. 15

Ordering Information

The V 6118 is available in the following packages:

QFP52, pin plastic package	V 6118 2 52F	Chip form	V 6118 2Chip*
	V 6118 4 52F		V 6118 4 Chip*
	V 6118 8 52F		V 6118 8 Chip'
TAB, tape automated bonding	V 6118 2 TAB	* on request	
	V 6118 4 TAB	When ordering, please specify the complete part number and package.	
	V 6118 8 TAB		