

## Features

- 256 x 256 or 512 x 256 switching configurations
- 8-bit or 4-bit channel switching capability
- Guarantees frame integrity for wideband channels
- Automatic identification of ST-BUS/GCI interfaces
- Accepts serial streams with data rates up to 8.192 Mb/s
- Rate conversion from 2.048 Mb/s to 4.096 or 8.192 Mb/s and vice-versa
- Programmable frame offset on inputs
- Per-channel three-state control
- Per-channel message mode
- Control interface compatible to Intel/Motorola CPUs
- Low power consumption

## Applications

- Medium size digital switch matrices
- Hyperchannel switching (e.g., ISDN H0)
- MVIP™ interface functions
- Serial bus control and monitoring
- Centralized voice processing systems
- Voice/Data multiplexer
- 32 kbit/s channel switching

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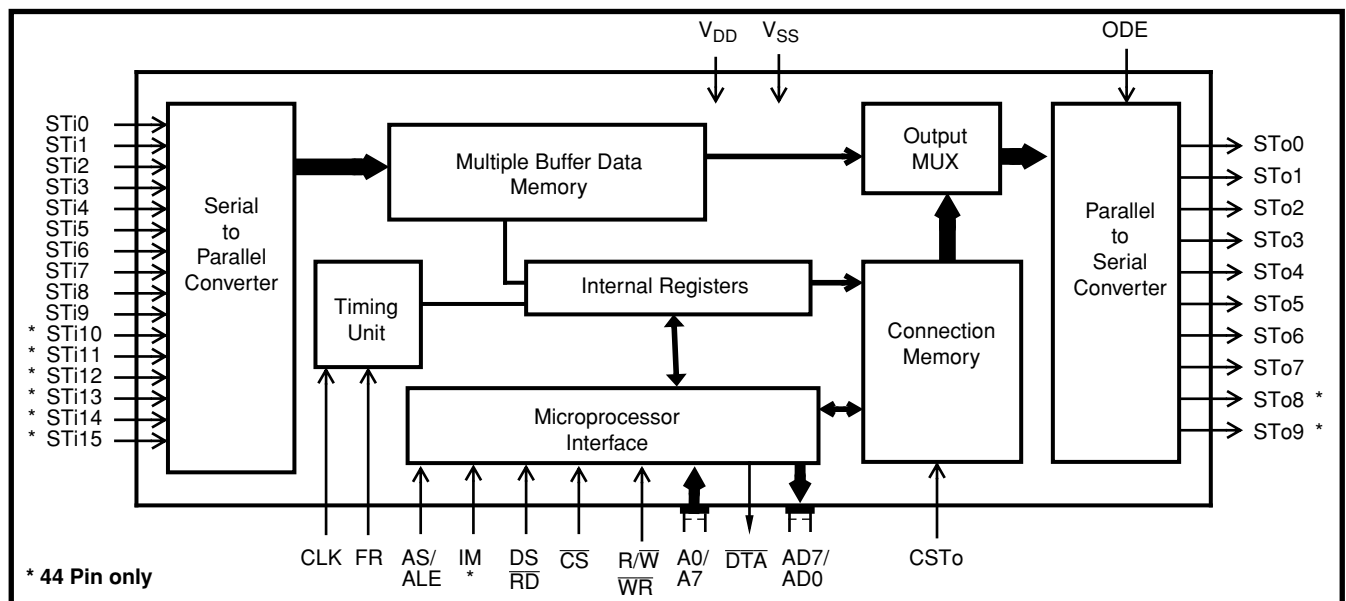
### Ordering Information

MT8986AE	40 Pin Plastic DIP
MT8986AP	44 Pin PLCC
MT8986AL	44 Pin QFP
<b>-40°C to +85°C</b>	

## Description

The Multiple Rate Digital Switch (MRDX) is an upgraded version of Zarlink's MT8980D Digital Switch (DX). It is pin compatible with the MT8980D and retains all of its functionality. This device is designed to provide simultaneous connections (non-blocking) for up to 256 64kb/s channels or blocking connections for up to 512 64kb/s channels. The serial inputs and outputs connected to MT8986 may have 32 to 128 64kb/s channels per frame with data rates ranging from 2048 up to 8192 kb/s. The MT8986 provides per-channel selection between variable and constant throughput delays allowing voice and grouped data channels to be switched without corrupting the data sequence integrity.

In addition, the MT8986 can be used for switching of 32 kb/s channels in ADPCM applications. The MT8986 is ideal for medium size mixed voice and data switching/processing applications.



**Figure 1 - Functional Block Diagram**

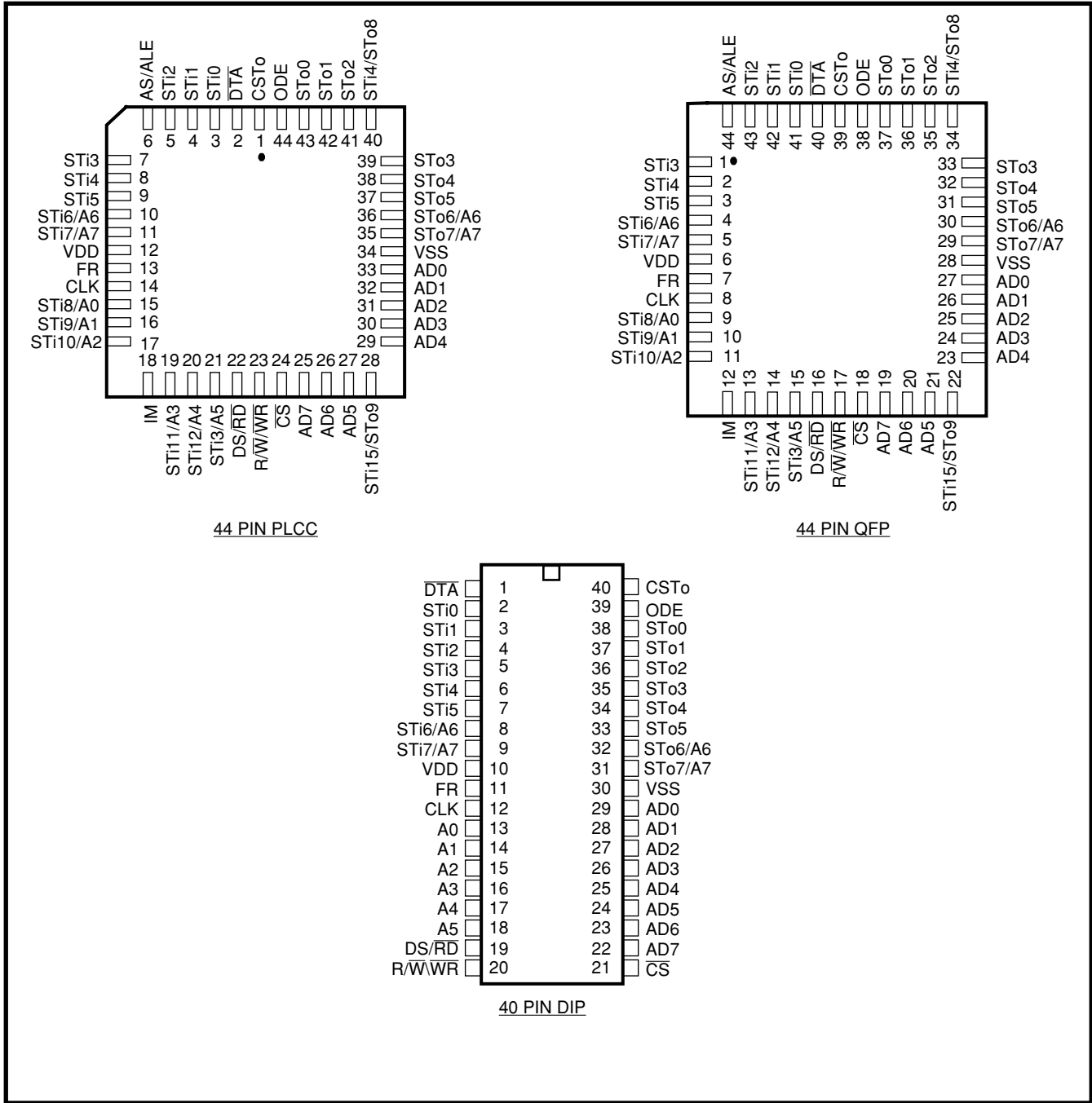


Figure 2 - Pin Connections

Pin Description

Pin #			Name	Description
40 DIP	44 PLCC	44 QFP		
1	2	40	DTA	<b>Data Acknowledgement</b> (Open Drain Output). This active low output indicates that a data bus transfer is complete. A 10kΩ pull-up resistor is required at this output.
2-7	3-5 7-9	41-43 1-3	STi0-5	<b>ST-BUS Inputs 0 to 5</b> (Inputs). Serial data input streams. These streams may have data rates of 2.048, 4.096 or 8.192 Mbit/s with 32, 64 or 128 channels, respectively.

## Pin Description (continued)

Pin #			Name	Description
40 DIP	44 PLCC	44 QFP		
8	10	4	STi6/A6	<b>ST-BUS Input 6/Addr.6 input</b> (Input). The function of this pin is determined by the switching configuration enabled. If non-multiplexed CPU bus is used along with a higher input rate of 8.192 or 4.096 Mb/s, this pin provides A6 address input function. For 2.048 and 4.096 Mb/s (8x4) applications or when multiplexed CPU bus (44 pin only) is selected, this pin assumes STi6 function. See Control Register bits description and Tables 1, 2, 6 & 7 for more details. Note that for applications where both A6 and STi6 inputs are required simultaneously (e.g., 8 x 4 switching configuration at 4.096 Mb/s or rate conversion between 2.048Mb/s to 4.196 or 8.192 Mb/s) the A6 input should be connected to pin STo6/A6.
9	11	5	STi7/A7	<b>ST-BUS Input 7/Addr.7 input</b> (Input): The function of this pin is determined by the switching configuration enabled. If non-multiplexed CPU bus is used along with a higher input rate of 8.192 Mb/s, this pin provides A7 address input function. For 2.048 and 4.096 Mb/s (8x4) applications or when multiplexed CPU bus (44 pin only) is selected, this pin assumes STi7 function. See Control Register bits description and Tables 1, 2, 6 & 7 for more details. Note that for applications where both A7 and STi7 inputs are required simultaneously (e.g., 2.048 to 8.192 Mb/s rate conversion) the A7 input should be connected to pin STo7/A7.
10	12	6	V <sub>DD</sub>	+5 Volt Power Supply.
11	13	7	FR	<b>Frame Pulse</b> (Input). This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS and GCI interface specifications.
12	14	8	CLK	<b>Clock</b> (Input). Serial clock for shifting data in/out on the serial streams. Depending on the serial interface speed selected by IMS (Interface Mode Select) register, the clock at this pin can be 4.096 or 8.192 MHz.
13-15	15-17	9-11	A0-2/ STi8-10	<b>Address 0-2 / Input Streams 8-10</b> (Input). When non-multiplexed CPU bus is selected, these lines provide the A0-A2 address lines to MT8986 internal registers. When 16x8 switching configuration is selected (in 44 pin only), then these pins are ST-BUS serial inputs 8 to 10 receiving data at 2.048 Mb/s.
16-18	19-21	13-15	A3-5/ STi11-13	<b>Address 3-5 / Input Streams 11-13</b> (Input). When non-multiplexed CPU bus is selected, these lines provide the A3-A5 address lines to MT8986 internal registers. When 16x8 switching configuration is selected (in 44 pin only), then these pins are ST-BUS serial inputs 11 to 13 receiving data at 2.048 Mb/s.
19	22	16	DS/ $\overline{\text{RD}}$	<b>Data Strobe/Read</b> (Input). When non-multiplexed CPU bus or Motorola multiplexed bus (44 pin only) are selected, this input is DS. This active high input works in conjunction with $\overline{\text{CS}}$ to enable read and write operation. For Intel/National multiplexed bus (44 pin only), this input is $\overline{\text{RD}}$ . This active low input configures the data bus lines (AD0-AD7) as outputs.
20	23	17	R/ $\overline{\text{W}}$ / $\overline{\text{WR}}$	<b>Read/Write \ Write</b> (Input). In case of non-multiplexed and Motorola multiplexed buses (44 pin only), this input is R/ $\overline{\text{W}}$ . This input controls the direction of the data bus lines (AD0-AD7) during a microprocessor access. With Intel/National multiplexed timing (44 pin only), this input is $\overline{\text{WR}}$ . This active low signal configures the data bus lines (AD0-AD7) as inputs.
21	24	18	$\overline{\text{CS}}$	<b>Chip Select</b> (Input). Active low input enabling a microprocessor read or write of the control register or internal memories.
22-29	25-27 29-33	19-21 23-27	AD7- AD0	<b>Data Bus</b> (Bidirectional): These pins provide microprocessor access to the internal control registers, connection memories high and low and data memories. In multiplexed bus mode (44 pin) these pins also provide the input address to the internal Address Latch circuit.
30	34	28	V <sub>SS</sub>	Ground.

## Pin Description (continued)

Pin #			Name	Description
40 DIP	44 PLCC	44 QFP		
31	35	29	STo7/A7	<p><b>ST-BUS Output 7/Address 7 input</b> (Three-state output/input). The function of this pin is determined by the switching configuration enabled. If non-multiplexed CPU bus is used along with data rates employing 8.192 Mb/s rates, this pin provides A7 address input function. For 2.048 Mb/s applications or when multiplexed CPU bus (44 pin only) is selected, this pin assumes STo7 function. See Tables 1, 2, 6 &amp; 7 for more details.</p> <p>Note that for applications where A7 input and STo7 output are required simultaneously (e.g., 8.192 to 2.048 Mb/s rate conversion), the A7 input should be connected to pin STi7/A7.</p>
32	36	30	STo6/A6	<p><b>ST-BUS Output 6/Address 6 input</b> (Three-state output/input). The function of this pin is determined by the switching configuration enabled. If non-multiplexed CPU bus is used along with a higher data rate employing 8.192 or 4.096 Mb/s, this pin provides the A6 address input function. For 2.048 Mb/s applications or when multiplexed CPU bus (44 pin only) is selected, this pin assumes STo6 function. See Tables 1, 2, 6 &amp; 7 for more details.</p> <p>Note that for applications where both A6 input and STo6 output are required simultaneously (e.g., 4.096 to 2.048 Mb/s or 8.192 to 2.048 Mb/s rate conversion applications), the A6 input should be connected to pin STi6/A6.</p>
33-38	37-39 41-43	31-33 35-37	STo5-0	<p><b>ST-BUS Outputs 5 to 0</b> (Three-state Outputs). Serial data output streams. These serial streams may be composed of 32, 64 and 128 channels at data rates of 2.048, 4.096 or 8.192 Mbit/s, respectively.</p>
39	44	38	ODE	<p><b>Output Drive Enable</b> (Input). This is the output enable input for the STo0 to STo9 serial outputs. If this input is low STo0-9 are high impedance. If this input is high each channel may still be put into high impedance by using per-channel control bits in Connect Memory High.</p>
40	1	39	CSTo	<p><b>Control ST-BUS Output</b> (Output). This is a 2.048 Mb/s output containing 256 bits per frame. The level of each bit is determined by the CSTo bit in the Connect Memory high locations.</p>
-	6	44	AS/ALE	<p><b>Address Strobe or Latch Enable</b> (Input). This input is only used if multiplexed bus is selected via the IM input pin (44 pin only). The falling edge of this signal is used to sample the address into the address latch circuit. In case of non-multiplexed bus, this input is not required and should be left open.</p>
-	18	12	IM	<p><b>CPU Interface Mode</b> (Input). If HIGH, this input configures MT8986 in multiplexed microprocessor bus mode. If this input pin is not connected or grounded, the MT8986 assumes non-multiplexed CPU interface.</p>
-	28	22	STi15/ STo9	<p><b>ST-BUS Input 15 / ST-BUS Output 9</b> (Input/three-state output). This pin is only used if multiplexed CPU bus is selected. If 16-input x 8-output switching configuration is enabled in the SCB bits (IMS register), this pin is an input receiving serial ST-BUS stream 15 at a data rate of 2.048 Mbit/s. If Stream Pair Selection capability is enabled (see switching configuration section), this pin is the ST-BUS stream 9 output. When non-multiplexed bus structure is used, this pin should be left open.</p>
-	40	34	STi14/ STo8	<p><b>ST-BUS Input 14 / ST-BUS Output 8</b> (Input/three-state output). This pin is only used if multiplexed CPU bus is selected. If 16-input x 8-output switching configuration is enabled in the SCB bits (IMS register), this pin is an input that receives serial ST-BUS stream 14 at a data rate of 2.048 Mbit/s. If Stream Pair Selection capability is enabled (see switching configuration section), this pin is the ST-BUS stream 8 output. When non-multiplexed bus structure is used, this pin should be left open.</p>

## DEVICE OVERVIEW

With the integration of voice, video and data services in the same network, there has been an increasing demand for systems which ensure that data at  $N \times 64$  kbit/s rates maintain sequence integrity while being transported through time-slot interchange circuits. This requirement demands time-slot interchange devices which perform switching with constant throughput delay for wideband data applications while guaranteeing minimum delay for voice channels.

The MT8986 device meets the above requirement and allows existing systems based on the MT8980D to be easily upgraded to maintain the data integrity when wideband data is transported. The device is designed to switch 32, 64 or  $N \times 64$  kbit/s data. The MT8986 can provide frame integrity for data applications and minimum throughput switching delay for voice applications on a per channel basis.

The serial streams of the MT8986 device can operate at 2.048, 4.096 or 8.192 Mbit/s and are arranged in 125  $\mu$ s wide frames which contain 32, 64 and 128 channels, respectively. In addition, a built-in rate conversion circuit allows the user to interconnect various backplane speeds like 2.048 or 4.096 or 8.192 Mb/s while maintaining the control of throughput delay function on a per-channel basis.

By using Zarlink Message mode capability, the microprocessor can access input and output time-slots on a per channel basis to control external circuits or other ST-BUS devices. The MT8986 automatically identifies the polarity of the frame synchronization input signal and configures its serial port to be compatible to both ST-BUS and GCI formats.

In the 44 pin packages, two different microprocessor bus interfaces can be selected through an input mode pin (IM): Non-Multiplexed or Multiplexed. These interfaces provide compatibility with Intel/National multiplexed and Motorola Multiplexed/Non-Multiplexed buses. In 44 pin, the MT8986 provides a  $16 \times 8$  switching configuration to form a  $512 \times 256$  channel blocking matrix. Also, a flexible Stream Pair Selection operation allows the software selection of which pair of input and output streams can be connected to an internal  $128 \times 128$  matrix. See Switching Configurations section for details.

## Functional Description

A functional Block Diagram of the MT8986 device is shown in Figure 1. Depending on the application, the

MT8986 device receives TDM serial data at different rates and from different number of serial streams.

### Data and Connect Memories

For all data rates, the received serial data is converted to parallel format by the serial to parallel converters and stored sequentially in a Data Memory. Depending on the selected operation programmed in the IMS (Interface Mode Select) register, the Data Memory may have up to 512 bytes in use. The sequential addressing of the Data Memory is performed by an internal counter which is reset by the input 8 kHz frame pulse (FR) marking the frame boundaries of the incoming serial data streams.

Data to be output on the serial streams may come from two sources: Data Memory or Connect Memory. Locations in the Connect Memory, which is split into HIGH and LOW parts, are associated with particular ST-BUS output streams. When a channel is due to be transmitted on an ST-BUS output, the data for the channel can either be switched from an ST-BUS input as in connection mode or it can be from the Connect Memory Low as in message mode. Data destined for a particular channel on the serial output stream is read from the Data Memory or Connect Memory Low during the previous channel time-slot. This allows enough time for memory access and parallel to serial conversion.

### Connection and Message Modes

In connection mode, the addresses of the input source data for all output channels are stored in the Connect memories High (CMH) and Low (CML). The CML and CMH are mapped so that each location corresponds to an output channel on the output streams. The number of source address bits in CMH and CML to be utilized varies according to the switching configuration selected in the IMS register. For details on the use of the source address data (CAB and SAB bits), see CMH and CML bit description (Figures 5 & 6). Once the source address bits are programmed by the CPU, the contents of the Data Memory at the selected address are transferred to the parallel-to-serial converters. By having the output channel specify the source channel through the connect memory, the user can route the same input channel to several output channels, allowing broadcast facility within the switch.

In message mode the CPU writes data to the Connect Memory Low locations corresponding to the output link and channel number. The contents of the Connect Memory Low are transferred directly to the parallel-to-serial converter one channel before it is to

be output. The Connect Memory Low data is transmitted on to the output every frame until it is changed by the CPU with a new data.

The features of each output channel in the MT8986 are controlled by the Connect Memory High bits. These bits determine individual output channels to be in message or connection mode, select throughput delay types and enable/disable output drivers. The Connect Memory High also provides additional stream and channel address bits for some configurations. In addition, the Connect Memory High provides one bit to allow the user to control the CSto output in 2.048 Mb/s applications.

If an output channel is set to high-impedance, the TDM serial stream output will be placed in high impedance during that channel time. In addition to the per-channel control, all channels on the TDM outputs can be placed in high impedance by pulling the ODE input pin LOW. This overrides the individual per-channel programming by the Connect Memory High bits.

The Connect Memory data is received via the Microprocessor Interface through the data I/O lines. The addressing of the MT8986 internal registers, Data and Connect memories is performed through address input pins and some bits of the device's Control register. The higher order address bits come from the Control register, which may be written or read through the microprocessor interface. The lower order address bits come directly from address input pins. For details on the device addressing, see Software Control and Control register bits description (Figure 3 & Tables 5, 6 and 7).

## Serial Data Interface

The master clock (CLK) can be either at 4.096 or 8.192 MHz allowing serial data link operations at 2.048, 4.096 and 8.192 Mb/s. These data rates can be independently selected on input and output streams allowing the MT8986 device to be used in various speed backplanes and in rate conversion applications. The selected data rates apply to the inputs or the output streams. Different bit rates among input streams or among output streams are not allowed. Due to the I/O data rate selection flexibility, two major operations can be selected: Identical or Different I/O data rates.

The DMO bit (Device Main Operation) in the IMS register is used for selecting between Identical I/O rates or Different I/O rates. On system power-up, the CPU should set up the DMO, the IDR (Input Data Rate) and ODR (Output Data Rate) bits located in the IMS register. When Identical I/O data rates are selected by the DMO bit, the switching configuration

and the number of the device's input and output streams can be selected through the SCB bits (Switching Configuration Bits) in the IMS register. See Switching Configurations section for details.

Depending on the application, the interface clock can be selected to be twice the data rate or equal to the data rate. This selection is performed through bit CLKM in the IMS register. For applications where both serial inputs and outputs are at 2.048 Mb/s (ST-BUS or GCI format), the CLKM bit should be set LOW enabling the interface clock to be twice the bit rate. In applications where both inputs and outputs are at 4.096 or 8.192 Mb/s, CLKM should be set HIGH enabling the interface clock to be equal to the bit rate. In applications where inputs and outputs are at different rates, the CLKM bit has no effect.

In applications with serial links at 2.048 Mb/s (see Figures 16 to 19), the input 8 kHz frame pulse can be in either ST-BUS or GCI format. The MT8986 device automatically detects the presence of an input frame pulse and identifies what type of backplane is present on the serial interface. Upon determining the interface connected to the serial port, the internal timing unit establishes the appropriate transmit and sampling edges. In ST-BUS format, every second falling edge of the 4.096 MHz clock marks a bit boundary and the input data is clocked in by the rising edge, three quarters of the way into the bit cell. In GCI format, every second rising edge of the 4.096 MHz clock marks the bit boundary while data sampling is performed during the falling edge, at three quarters of the bit boundaries.

For identical I/O rates at 4.096 and 8.192 Mb/s (see Figure 20), the clock and interface data rates are equal. The bit transmit and sampling edges vary according to the applied frame pulse polarity. For example, if the FR pulse polarity is positive, the bit transmit operation is done on every rising edge of CLK and the bit sampling on every falling edge. If the FR pulse polarity is negative, these edges are inverted. For different I/O rates, the MT8986 side operating at 2.048 Mb/s data rate will comply with ST-BUS or GCI interfaces for transmit and sampling procedures. The MT8986 side operating at 4.096 or 8.192 Mb/s behaves according to the frame pulse polarity applied. See Figures 22 to 25.

## Switching Configurations

Switching configurations are determined basically by the interface rates selected at the serial inputs and outputs. To specify the switching configuration required, the IMS register has to be initialized on system power-up. In case of Identical I/O rates (DMO bit LOW) at both inputs and outputs, the switching configuration is selected by the two SCB bits as

shown in table 8 (see IMS register). In case of different I/O rates (DMO bit HIGH), the switching configuration is always non-blocking with different number of I/O streams which is defined by the IDR and ODR bits (see IMS register).

### Identical Input/Output Data Rates

When identical input/output data rate is selected by the DMO bit, the I/O rate is determined by the IDR0-1 bits, and the ODR0-1 bits are ignored. For each data rate specified by the IDR bits, different switching configurations can be selected in the SCB1-0 bits.

#### Serial Links with Data Rates at 2.048 Mb/s

When 2.048 Mb/s data rate is selected at the IDR bits, four different I/O configurations can be selected by the SCB1-0 bits (see Table 8); 8 x 8, 16 x 8, 4 x 4 with stream pair selection and nibble switching.

If 8 x 8 switching configuration is selected, a 256 x 256 channel non-blocking switching matrix is available. In this configuration, the MT8986 device is configured with 8 input and 8 output data streams with 32 64 Kbit/s channels each. The interface clock for this operation is 4.096 MHz with both ST-BUS and GCI compatibilities and the per-channel selection between variable and constant throughput delay functions is provided. This configuration is available in both the 40 and 44 pin packages.

In 16 x 8 switching configuration, a 512 x 256 channel blocking switch matrix is available. This configuration is only provided in the 44 pin package and when the CPU interface is configured in multiplexed bus mode. The device clock in this application is 4.096 MHz, ST-BUS or GCI compatible. This configuration only provides variable throughput delay.

If the stream pair selection switching configuration is selected, only four input and four outputs (4 pairs of serial streams) can be selected by the CPU to be internally connected to the switch matrix, totalling a 128 x 128 channel non-blocking switch. From the 10 serial link pairs available, two pairs are permanently connected to the internal matrix (STi0/STo0 and STi1/STo1). An internal stream pair selection capability allows two additional pairs of serial links to be selected from the remaining 8 pairs (from STi/STo2 to STi9/STo9) and be connected to the internal matrix along with the permanently connected STi0/STo0 and STi1/STo1 streams. The two additional pair of streams called stream pair A and stream pair B, should be selected in the Stream Pair Selection register (SPS). The device clock for this operation is

4.096 MHz compatible to ST-BUS and GCI interfaces. In addition, the per-channel selection between variable or constant throughput delay is available. This configuration is only provided in the 44 pin packages.

In case of nibble switching, 4-bit wide 32 kb/s data channels can be switched within the device. In this case, every serial stream is run at 2.048 Mb/s and transports 64 nibbles per frame. When Nibble Switching is selected at SCB bits, the MT8986 automatically assumes a 8 input x 4 output stream configuration, providing a blocking switch matrix of 512 x 256 nibbles. If a non-blocking switch matrix is required for nibble switching, the switch capacity is reduced to 256 x 256 channel with a 4 input x 4 output configuration; the non-blocking matrix can be arranged by the user by selecting any four of the 8 input streams. In nibble switching the interface clock is 4.096 MHz.

#### Serial Links with Data Rates at 4.096 Mb/s

Two I/O configurations can be enabled by the SCB bits when input and output data rates are 4.096 Mb/s on each serial stream: 8 x 4 and 4 x 4. When 8 x 4 switching configuration is selected, a 512 x 256 channel blocking switch is available with serial streams carrying 64, 64 Kb/s channels each. For this operation, a 4.096 MHz interface clock equal to the bit rate should be provided to MT8986. Only variable throughput delay mode is provided.

In case of 4 x 4 switching configuration, a 256 x 256 channel non-blocking switch is available with serial streams carrying 64, 64 Kb/s channels each. In this configuration, the interface clock is 4.096 MHz and the per-channel selection between variable and constant throughput delay operation is provided. Figure 20 shows the timing for 4.096 Mb/s operation.

#### Serial Links with Data Rates at 8.192 Mb/s

Only 2 input x 2 output stream configuration is available for 8.192 Mb/s, allowing a 256 x 256 channel non-blocking switch matrix to be implemented. To enable this operation, the IDR bits should be programmed to select 8.192 Mb/s rates and the SCB bits have no effect. At 8.192 Mb/s, every input and output stream provides 128 time-slots per frame. The interface clock for this operation should be 8.192 MHz. Figure 20 shows the timing for 8.192 Mb/s operation.

Table 1 summarizes the MT8986 switching configurations for identical I/O data rates.

Serial Interface Data Rate	Interface Clock required at CLK Pin (MHz)	Number of Input x Output Streams	Matrix Channel Capacity	Input/Output Streams Used	Variable/ Constant throughput Delay Selection
2 Mb/s	4.096	8x8	256x256 Non-Blocking	STi0-7/STo0-7	Yes
2 Mb/s *	4.096	16x8 *	512x256 Blocking	STi0-15/STo0-7	No
2 Mb/s *	4.096	10x10 *	128x128 Non-Blocking (only 4 input x 4-output can be selected)	STi0-9/STo0-9	Yes
Nibble Switching (2 Mb/s)	4.096	8x4	512x256 Nibbles	STi0-7/STo0-3	No
4 Mb/s	4.096	8x4	512x256 Blocking	STi0-7/STo0-3	No
4 Mb/s	4.096	4x4	256x256 Non-Blocking	STi0-3/STo0-3	Yes
8 Mb/s	8.192	2x2	256x256 Non-Blocking	STi0-1/STo0-1	Yes

**Table 1. Switching Configurations for Identical Input and Output Data Rates**

\* - only in the 44 pin packages

## Different Input/Output Data Rates

When Different I/O rate is selected by the DMO bit, the input and output data rates should be selected at the IDR and ODR bits, respectively. The Switching Configuration Bits (SCB) are ignored with this operation. This selection allows the user to multiplex conventional 2.048 Mb/s serial streams into two higher rates and vice-versa. In addition to the rate conversion itself, the MT8986 allows for a complete 256 x 256 channel non-blocking switch at different rates. In this operation, the per-channel variable/constant throughput delay selection is provided.

Depending on which data rates are programmed for input and output streams, the number of data streams used on the input and output as well as the serial interface clock (CLK input pin) is different. Once the CPU defines the data rates at the IDR and ODR bits, the MT8986 automatically configures itself with the appropriate number of input and output streams for the desired operation. Table 2 summarizes the four options available when MT8986 is used with different I/O rates. Figures 22 to 25 show the timing for each of the four modes shown in Table 2.

## Input Frame Offset Selection

When 4.096 or 8.192 Mb/s serial interfaces are selected, the MT8986 device provides a feature called Input Frame Offset allowing the user to compensate for the varying delays at the incoming serial inputs while building large switch matrices. Usually, different delays occur on the digital backplanes causing the data and frame synchronization signals to be skewed at the input of the switch device. This may result in the system frame synchronization pulse to be active at the MT8986 FR input before the first bit of the frame is received at the serial inputs.

When the input frame offset is enabled, an "internal delay" of up to four clock periods is added to the actual data input sampling, providing the MT8986 serial timing unit a new input frame reference. An internal virtual frame is created which is aligned with the framing of the actual serial data coming in at the serial inputs and not with the FR frame pulse input. In this operation, the transmission of the output frame on the serial links is still aligned to the frame pulse input signal (FR).

The selection of the data input sampling delay is defined by the CPU in the Frame Input Offset

Input and Output Data Rates	Interface Clock required at CLK Pin (MHz)	Number of Input x Output Streams	Matrix Channel Capacity	Input/Output Streams Used	Variable/ Constant throughput Delay Selection
2 Mb/s to 4 Mb/s	4.096	8x4	256x256 Non-Blocking	STi0-7/STo0-3	Yes
2 Mb/s to 8 Mb/s	8.192	8x2	256x256 Non-Blocking	STi0-7/STo0-1	Yes
4 Mb/s to 2 Mb/s	4.096	4x8	256x256 Non-Blocking	STi0-3/STo0-7	Yes
8 Mb/s to 2 Mb/s	8.192	2x8	256x256 Non-Blocking	STi0-1/STo0-7	Yes

**Table 2. Switching Configurations for Different I/O Data Rates**



Register (FIO). If this function is not required in the user's applications, the FIO register should be set up during system initialization to a state where offset functions are disabled.

## Delay Through the MT8986

The switching of information from the input serial streams to the output serial streams results in a delay. Depending on the type of information to be switched, the MT8986 device can be programmed to perform time-slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, variable throughput delay can be selected ensuring minimum delay between input and output data. In wideband data applications, constant throughput delay can be selected maintaining the frame integrity of the information through the switch.

The delay through the MT8986 device varies according to the type of throughput delay selected in the  $\bar{V}/C$  bit of the connect memory high.

### Variable Throughput Delay Mode ( $\bar{V}/C$ bit = 0)

#### Identical I/O Data Rates

The delay in this mode is dependent on the combination of source and destination channels and

it is independent of the input and output streams. The minimum delay achievable in the MT8986 depends on the data rate selected for the serial streams. For instance, for 2.048 Mb/s the minimum delay achieved corresponds to three time-slots. For 4.096 Mb/s it corresponds to five time-slots while for 8.192 Mb/s it is nine time-slots. Switching configurations with input and output channels that provides more than its corresponding minimum throughput delay, will have a throughput delay equal to the difference between the output and input channels; i.e., the throughput delay will be less than one frame period. Table 3a shows the MT8986 throughput delay for each data rate operation.

#### Different I/O Data Rates

Except for 2 Mb/s to 4 Mb/s and 2 Mb/s to 8 Mb/s rate conversion operations, the throughput delay in the MT8986 may vary according to the output stream used for switching.

Table 3b explains the worst case conditions for the throughput delay when different I/O data rate switching configurations are used.

### Constant Throughput Delay mode ( $\bar{V}/C$ bit = 1)

In this mode frame sequence integrity is maintained in both Identical and Different I/O Data Rate

Input Rate	Output Channel (# m)				
	m < n	m=n, n+1, n+2	m= n+3, n+4	m=n+5, .. n+8	m > n+8
2.048 Mb/s	32-(n-m) t.s.	m-n + 32 t.s.	m-n t.s.	m-n t.s.	m-n t.s.
4.096 Mb/s	64-(n-m) t.s.	m-n + 64 t.s.	m-n+64 t.s.	m-n t.s.	m-n t.s.
8.192 Mb/s	128-(n-m) t.s.	m-n + 128 t.s.	m-n+128 t.s.	m-n+128 t.s.	m-n t.s.

**Table 3a. Variable Throughput Delay Values for Identical I/O Rate Applications**

n= input channel, t.s. = time-slot

I/O Data Rate Configuration	Output Stream Used			
	0, 1	2, 3	4, 5	6, 7
2 Mb/s to 4 Mb/s	dmin=5x 4Mb/s t.s. dmax=1 fr.+(4x 4Mb/s t.s.)			
2 Mb/s to 8 Mb/s	dmin=9x 8Mb/s t.s. dmax=1 fr.+(8x 8Mb/s t.s.)			
4 Mb/s to 2 Mb/s	dmin=3x 2Mb/s t.s. dmax=1 fr.+(2x 2Mb/s t.s.)		dmin=(2x 2Mb/s t.s.)+(1x 4Mb/s t.s.) dmax=1 fr.+(1x 2Mb/s t.s.)+(1x 4Mb/s t.s.)	
8 Mb/s to 2 Mb/s	dmin=3x 2Mb/s t.s. dmax=1 fr.+(2x 2Mb/s t.s.)	dmin=(2x 2Mb/s t.s.)+(3x 8Mb/s t.s.) dmax=1 fr.+(1x 2Mb/s t.s.)+(3x 8Mb/s t.s.)	dmin=(2x 2Mb/s t.s.)+(2x 8Mb/s t.s.) dmax=1 fr.+(1x 2Mb/s t.s.)+(2x 8Mb/s t.s.)	dmin=(2x 2Mb/s t.s.)+(1x 8Mb/s t.s.) dmax=1 fr.+(1x 2Mb/s t.s.)+(1x 8Mb/s t.s.)

**Table 3b. Min/Max Throughput Delay Values for Different I/O Rate Applications**

**Notes:** dmin and dmax are measured in time-slots and at the point in time when the output channel is completely shifted out.

t.s. = time-slot

fr. = 125  $\mu$ s frame

2 Mb/s t.s. = 3.9  $\mu$ s

4 Mb/s t.s. = 1.95  $\mu$ s

8 Mb/s t.s. = 0.975  $\mu$ s

Data Rate	Throughput Delay (d)
2.048 Mb/s	$d = [32 + (32 - \text{IN}) + (\text{OUT} - 1)]$ ; (expressed in # time-slots) 2.048 Mb/s time-slot: 3.9 $\mu$ s IN: input time-slot (from 1 to 32) OUT: output time-slot (from 1 to 32)
4.096 Mb/s	$d = [64 + (64 - \text{IN}) + (\text{OUT} - 1)]$ ; (expressed in # time-slots) 4.096 Mb/s time-slot: 1.95 $\mu$ s IN: input time-slot (from 1 to 64) OUT: output time-slot (from 1 to 64)
8.192 Mb/s	$d = [128 + (128 - \text{IN}) + (\text{OUT} - 1)]$ ; (expressed in # time-slots) 8.192 Mb/s time-slot: 0.975 $\mu$ s IN: input time-slot (from 1 to 128) OUT: output time-slot (from 1 to 128)

**Table 4. Constant Throughput Delay values**

operations by making use of a multiple Data-Memory buffer technique. The input channels written in any of the buffers during frame N will be read out during frame N+2. In applications at 2.048 Mb/s for instance, the minimum throughput delay achievable in constant delay mode will be 32 time-slots; for example, when input time-slot 32 (channel 31) is switched to output time-slot 1 (channel 0). Likewise, the maximum delay is achieved when the first time slot in a frame (channel 0) is switched to the last time-slot in the frame (channel 31), resulting in 94 time-slots of delay.

To summarize, any input time-slot from input frame N will always be switched to the destination time-slot on output frame N+2. Table 4 describes the MT8986 constant throughput delay values for different data rates.

## Microprocessor Port

The non-multiplexed bus interface provided by the MT8986 device is identical to that provided in MT8980 Digital Switch device. In addition to the non-multiplexed bus, the MT8986 device provides an enhanced microprocessor interface with multiplexed bus structure compatible to both Motorola and Intel buses. The multiplexed bus structure is available only in the 44 pin packages and it is selected by the CPU Interface Mode (IM) input pin.

If IM input pin is not connected (left open) or grounded, the MT8986 parallel port assumes its default Motorola non-multiplexed bus mode identical to that of MT8980. If IM input is connected HIGH, the internal parallel microport provides compatibility to MOTEL interface allowing direct connection to Intel, National and Motorola CPUs.

The MOTEL circuit (**MO**trola and **IN**TEL compatible bus) automatically identifies the type of CPU Bus connected to the MT8986 device. This circuit uses

the level of the DS/ $\overline{\text{RD}}$  input pin at the rising edge of the AS/ALE to identify the appropriate bus timing connected to the MT8986. If DS/ $\overline{\text{RD}}$  is LOW at the rising edge of AS/ALE then Motorola bus timing is selected. If DS/ $\overline{\text{RD}}$  is HIGH at the rising edge of AS/ALE, then Intel bus timing is selected.

When MT8986 parallel port is operating in Motorola, National or Intel multiplexed bus interfaces, the signals available for controlling the device are: AD0-AD7 (Data and Address), ALE/AS (Address Latch Enable/Address Strobe), DS/ $\overline{\text{RD}}$  (Data Strobe/Read), R/ $\overline{\text{W}}$ WR (Read/Write/Write),  $\overline{\text{CS}}$  (Chip Select) and  $\overline{\text{DTA}}$  (Data Acknowledgement). In Motorola non-multiplexed bus, the interface control signals are: data bus (AD0-AD7), six address input lines (A0-A5) and four control lines ( $\overline{\text{CS}}$ , DS, R/ $\overline{\text{W}}$  and  $\overline{\text{DTA}}$ ). See Figures 26 to 28 for each CPU interface timing.

The MT8986 parallel microport provides the access to the IMS, Control registers, the Connection Memory High, the Connection Memory Low and the Data Memory. All locations can be read or written except for the data memory which can be read only.

## Software Control

The address bus on the microprocessor interface selects the internal registers and memories of the MT8986. If the A5 address input is LOW, then the MT8986 Internal Control, Interface Mode, Stream Pair Selection and Frame Input Offset registers are addressed by the A4 to A0 bits according to Table 5. If A5 input is HIGH, then the remaining address input lines are used to select memory subsections of up to 128 locations corresponding to the maximum number of channels per input or output stream. The address input lines and the Stream Address bits (STA) of the Control register give the user the capability of accessing all sections of the MT8986 Data and Connect memories.

The Control and Interface Mode Selection registers together control all the major functions of the device. The Interface Mode Select register should be set up during system power-up to establish the desired switching configuration as explained in the Serial Interface and Switching Configurations sections.

The Control register is dynamically used by the CPU to control switching operations in the MT8986. The Control register selects the device's internal memories and its subsections to specify the input and output channels selected for switching procedures.

The data in the Control register consists of Split memory and Message mode bits, Memory select and Stream Address bits. The memory select bits allow the Connect Memory HIGH or LOW or the Data Memory to be chosen, and the Stream Address bits define an internal memory subsections corresponding to input or output ST-BUS streams.

Bit 7 (Slip Memory) of the Control register allows split memory operation whereby reads are from the Data memory and writes are to the Connect Memory LOW.

The Message Enable bit (bit 6) places every output channel on every output stream in message mode; i.e., the contents of the Connect Memory LOW (CML) are output on the ST-BUS output streams once every frame unless the ODE input pin is LOW. If ME bit is HIGH, then the MT8986 behaves as if bits 2 (Message Channel) and 0 (Output Enable) of every

Connect Memory HIGH (CMH) locations were set to HIGH, regardless of the actual value. If ME bit is LOW, then bit 2 and 0 of each Connect Memory HIGH location function normally. In this case, if bit 2 of the CMH is HIGH, the associated ST-BUS output channel is in Message mode. If bit 2 of the CMH is LOW, then the contents of the SAB and CAB bits of the CMH and CML define the source information (stream and channel) of the time-slot that is to be switched to an output.

If the ODE input pin is LOW, then all serial outputs are high-impedance. If ODE is HIGH, then bit 0 (Output Enable) of the CMH location enables (if HIGH) or disables (if LOW) the output drivers for the corresponding individual ST-BUS output stream and channel.

The contents of bit 1 (CSTo) of each Connection Memory High location is output on CSTo pin once every frame. The CSTo pin is a 2048 Mbit/s output which carries 256 bits. If CSTo bit is set HIGH, the corresponding bit on CSTo output is transmitted HIGH. If CSTo bit is LOW, the corresponding bit on the CSTo output is transmitted LOW. The contents of the 256 CSTo bits of the CMH are transmitted sequentially on to the CSTo output pin and are synchronous to the 2.048 Mb/s ST-BUS streams. To allow for delay in any external control circuitry the contents of the CSTo bit is output one channel before the corresponding channel on the ST-BUS streams. For example, the contents of CSTo bit in position 0 (ST0, CH0) of the CMH, is transmitted synchronously with ST-BUS channel 31, bit 7. The contents of CSTo bit in position 32 (ST1, CH0) of the

A7	A6	A5	A4	A3	A2	A1	A0	Location
X	X	0	0	0	0	0	0	Control Register
X	X	0	0	0	0	0	1	Interface Mode Select Register
X	X	0	0	0	0	1	0	Stream Pair Select Register
X	X	0	0	0	0	1	1	Frame Input Offset Register
0	0	1	0	0	0	0	0	Channel 0*
0	0	1	0	0	0	0	1	Channel 1*
•	•	1	•	•	•	•	•	•
•	•	1	•	•	•	•	•	•
0	0	1	1	1	1	1	1	Channel 31*
0	1	1	0	0	0	0	0	Channel 32**
0	1	1	0	0	0	0	1	Channel 33**
•	•	1	•	•	•	•	•	•
•	•	1	•	•	•	•	•	•
0	1	1	1	1	1	1	1	Channel 63**
1	0	1	0	0	0	0	0	Channel 64***
•	•	1	•	•	•	•	•	•
•	•	1	•	•	•	•	•	•
1	1	1	1	1	1	1	1	Channel 127***

**Table 5. Address Memory Map**

- \*. channels 0 to 31 are used in 2.048 Mb/s (8 x 8, 16 x 8 and 10 x 10)  
 \*\*. channels 0 to 63 are used in 4.096 Mb/s (Nibble Switching, 4 x 4, 8 x 4 or Different I/O rates)  
 \*\*\*. channels 0 to 127 are used in 8.192 Mb/s (2 x 2 or Different I/O rates)

CMH is transmitted during ST-BUS channel 31 bit 6. For more detailed description of the CSto operation, see section 6 of Application Note MSAN-123.

The Bit  $\bar{V}/C$  (Variable/Constant Delay) of each Connect Memory High location allows the per-channel selection between Variable and Constant throughput delay modes.

## Initialization of the MT8986

On initialization or power up, the contents of the Connection Memory High can be in any state. This is a potentially hazardous condition when multiple MT8986 ST-BUS outputs are tied together to form matrices, as these outputs may conflict. The ODE pin should be held low on power up to keep all outputs in the high impedance condition.

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the matrices, and put all other channels into the high impedance state. Care should be taken that no two ST-BUS outputs drive the bus simultaneously. When this process is complete, the microprocessor controlling the matrices can bring the ODE signal high to relinquish high impedance state control to the CMH<sub>b</sub>0s.

## Control Register - Read/Write

<div><div>76543210</div><div><div>SM</div><div>ME</div><div>STA3</div><div>MS1</div><div>MS0</div><div>STA2</div><div>STA1</div><div>STA0</div></div></div>							
BIT	NAME	DESCRIPTION					
7	SM	<b>Split Memory.</b> When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory Low, except when the Control Register is accessed again. When 0, the Memory Select bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.					
6	ME	<b>Message Enable.</b> When 1, the contents of the Connection Memory Low are output on the Serial Output streams except when in High Impedance as set by the ODE input. When 0, the Connection Memory bits for each channel determine what is output.					
5	STA3	<b>Stream Address Bit 3.</b> This bit is used in the 44 pin packages when 16 x 8 switching configuration is selected. It is used with STA2-0 to select one of the 16 input data streams whenever the Data Memory is to be read. The programming of this bit has no effect in other switching configurations.					
4-3	MS1-0	<b>Memory Select Bits.</b> The memory select bits operate as follows: 0-0 - Not to be used 0-1 - Data Memory (read only from the CPU) 1-0 - Connection Memory Low 1-1 - Connection Memory High					
2-0	STA2-0	The number expressed in binary notation on these bits refers to the input or output ST-BUS stream which corresponds to the subsection of memory made accessible for subsequent operations.  The use of these bits depends on the switching configuration as well as the device's main operation defined by the DMO bit of the Interface Mode Selection register. Tables 6 and 7 show the utilization of these bits according to the device's main operation.					

Figure 3 - Control Register Description

Identical I/O Rate	# of Input x Output Streams	STA bits used to select subsections of the Data Memory	STA bits used to select subsections of the Connection Memory	Input Address pins used to select individual Connection and Data Memory positions within the selected subsection
2 Mb/s	8x8	STA2, STA1, STA0	STA2, STA1, STA0	A4, A3, A2, A1, A0
2 Mb/s *	4x4 *	STA1, STA0	STA1, STA0	A4, A3, A2, A1, A0
2 Mb/s *	16x8 *	STA3, STA2, STA1, STA0	STA2, STA1, STA0	A4, A3, A2, A1, A0
4 Mb/s	4x4	STA1, STA0	STA1, STA0	A6, A4, A3, A2, A1, A0
4 Mb/s	8x4	STA2, STA1, STA0	STA1, STA0	A6, A4, A3, A2, A1, A0
8 Mb/s	2x2	STA0	STA0	A7, A6, A4, A3, A2, A1, A0
Nibble Switch (2 Mb/s)	8x4	STA2, STA1, STA0	STA1, STA0	A6, A4, A3, A2, A1, A0 **

**Table 6. Use of STA Bits for Identical I/O Data Rate Operation**

\* - only in the 44 pin packages.

\*\* - for Data Memory Read operations A0 is not required since two nibbles are provided per read access.

Different I/O Rate	Input x Output Streams Config.	STA bits used to select Data Memory subsections	STA bits used to select Connection Memory subsections	Input Address pins used to access individual Data Memory positions within the selected subsection	Input Address pins used to access individual Connection Memory positions within the selected subsection
2 Mb/s to 4 Mb/s	8x4	STA2, STA1, STA0	STA1, STA0	A4, A3, A2, A1, A0	A6, A4, A3, A2, A1, A0
2 Mb/s to 8 Mb/s	8x2	STA2, STA1, STA0	STA0	A4, A3, A2, A1, A0	A7, A6, A4, A3, A2, A1, A0
4 Mb/s to 2 Mb/s	4x8	STA1, STA0	STA2, STA1, STA0	A6, A4, A3, A2, A1, A0	A4, A3, A2, A1, A0
8 Mb/s to 2 Mb/s	2x8	STA0	STA2, STA1, STA0	A7, A6, A4, A3, A2, A1, A0	A4, A3, A2, A1, A0

**Table 7. Use of STA Bits for Different I/O Data Rate Operation**

Note: In rate conversion applications, Data Memory subsections have different sizes than Connection Memory subsections. This implies that different address inputs are used to select individual positions within the subsections for each type of memory.

## Interface Mode Selection Register - Read/Write

<div><div>76543210</div><div><div>DMO</div><div>IDR1</div><div>IDR0</div><div>ODR1</div><div>ODR0</div><div>SCB1</div><div>SCB0</div><div>CLKM</div></div></div>																	
BIT	NAME	DESCRIPTION															
7	DMO	<p><b>Device Main Operation.</b> This bit is used by the CPU to define one of the two main operations of the MT8986 device. If this bit is LOW, the MT8986 is configured for identical I/O data rates. For this operation, the user should also specify the switching configuration through the SCB bits.</p> <p>If this bit is HIGH, the MT8986 device is configured in Different I/O data rate. This allows combinations of input and output data rates as shown in Table 2. The SCB bits have no effect in this application and the device is in Non-Blocking switch configuration with a 256 x 256 channel capacity.</p>															
6-5	IDR1-0	<p><b>Input Data Rate Selection.</b> These two bits select three different data rates for the inputs of the MT8986. In the case of identical I/O rates (DMO bit = 0), these bits also determine the serial output data rate.</p> <table><tr><th>IDR1</th><th>IDR0</th><th>Input Rate</th></tr><tr><td>0</td><td>0</td><td>2.048 Mb/s</td></tr><tr><td>0</td><td>1</td><td>4.096 Mb/s</td></tr><tr><td>1</td><td>0</td><td>8.192 Mb/s</td></tr><tr><td>1</td><td>1</td><td>reserved</td></tr></table>	IDR1	IDR0	Input Rate	0	0	2.048 Mb/s	0	1	4.096 Mb/s	1	0	8.192 Mb/s	1	1	reserved
IDR1	IDR0	Input Rate															
0	0	2.048 Mb/s															
0	1	4.096 Mb/s															
1	0	8.192 Mb/s															
1	1	reserved															
4-3	ODR1-0	<p><b>Output Data Rate Selection.</b> These bits are only used when Different I/O rates are selected (DMO bit=1). These two bits select three different data rates for the serial outputs of the MT8986. These bits are ignored if DMO bit = 0.</p> <table><tr><th>ODR1</th><th>ODR0</th><th>Output Rate</th></tr><tr><td>0</td><td>0</td><td>2.048 Mb/s</td></tr><tr><td>0</td><td>1</td><td>4.096 Mb/s</td></tr><tr><td>1</td><td>0</td><td>8.192 Mb/s</td></tr><tr><td>1</td><td>1</td><td>reserved</td></tr></table>	ODR1	ODR0	Output Rate	0	0	2.048 Mb/s	0	1	4.096 Mb/s	1	0	8.192 Mb/s	1	1	reserved
ODR1	ODR0	Output Rate															
0	0	2.048 Mb/s															
0	1	4.096 Mb/s															
1	0	8.192 Mb/s															
1	1	reserved															
2-1	SCB1-0	<p><b>Switching Configuration Bits 1-0.</b> These bits should only be used when DMO is set LOW. The use of these bits to select the switching configuration of the MT8986 device is described in Table 8.</p>															
0	CLKM	<p><b>Clock Mode.</b> This bit is only used when the MT8986 device is set to operate in identical I/O data rates. When set High, this bit selects the interface clock to be equal to the bit rate. If Low, this bit selects the interface clock to be twice the bit rate. For Different I/O data rate applications, this bit is ignored.</p>															

Figure 4 - IMS Register Description

DMO Bit	Data Rate Selected at IDR bits (Mb/s)	SCB1	SCB0	Configuration
LOW Identical I/O Rates	2.048	0	0	8 inputs x 8 outputs - Non Blocking
		0	1	16 inputs x 8 outputs - Blocking**
		1	0	Stream pair selection capability (internal channel capacity = 128 x 128) - Non Blocking**
		1	1	Nibble Switching - 8 inputs x 4 outputs - Blocking
	4.096	0	0	8 inputs x 4 outputs - Blocking
		0	1	4 inputs x 4 outputs - Non-Blocking
		1	0	Reserved
		1	1	Reserved
	8.192	no effect	no effect	2 inputs x 2 outputs - Non-Blocking
	Input/Output Rate selected in IDR/ODR bits	no effect	no effect	Reserved
HIGH Different I/O Rates				

**Table 8. Switching Configurations for Identical I/O Rates**

\*\* 44 pin packages only



## Connection Memory High - Read/Write

<div><div>76543210</div><div><div>X</div><div><math>\bar{V}/C</math></div><div>SAB3</div><div>CAB6</div><div>CAB5</div><div>MC</div><div>CSTo</div><div>OE</div></div></div> <div>(CM high bits)</div>							
BIT	NAME	DESCRIPTION					
6	$\bar{V}/C$	<b>Variable/Constant Throughput Delay Mode.</b> This bit is used to select between Variable (LOW) and Constant Delay (HIGH) modes in a per-channel basis. Tables 1 and 2 describe the switching configurations that have this function. In the modes where this function is not available, this bit has not effect.					
5	SAB3	<b>Source Stream Address bit 3.</b> This bit is used along with bits SAB0-2 in CML to select up to 16 different source streams for the connection. Depending on the state of DMO bit and the switching configuration enabled, not all SAB3-0 bits have to be used. See Tables 9 and 10 for details on the utilization of the SAB bits.					
4-3	CAB6-5	<b>Source Channel Address bits 5 and 6.</b> These two bits are used together with bits CAB0-4 in Connect Memory Low to select up 128 different source channels for the connection. Depending on the data rate used in the input/output streams, 5, 6 or all 7 CAB bits can be used respectively, to select 32, 64 or 128 different channels. See Tables 9 and 10 for details on the utilization of the CAB bits.					
2	MC	<b>Message Channel.</b> When 1, the contents of the corresponding location in Connection Memory Low are output on the corresponding channel and stream. When 0, the contents of the programmed location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location’s channel and stream.					
1	CSTo	<b>CSTo Bit.</b> This bit is only available in 2.048 Mb/s applications. It drives a bit time on the CSTo output pin.					
0	OE	<b>Output Enable.</b> This bit enables the output drivers on a per-channel basis. This allows individual channels on individual streams to be made high-impedance, allowing switch matrices to be constructed. A HIGH enables the driver and a LOW disables it.					

Figure 5 - Connection Memory High (CMH) Bits

x=Don't care

## Connection Memory Low - Read/Write

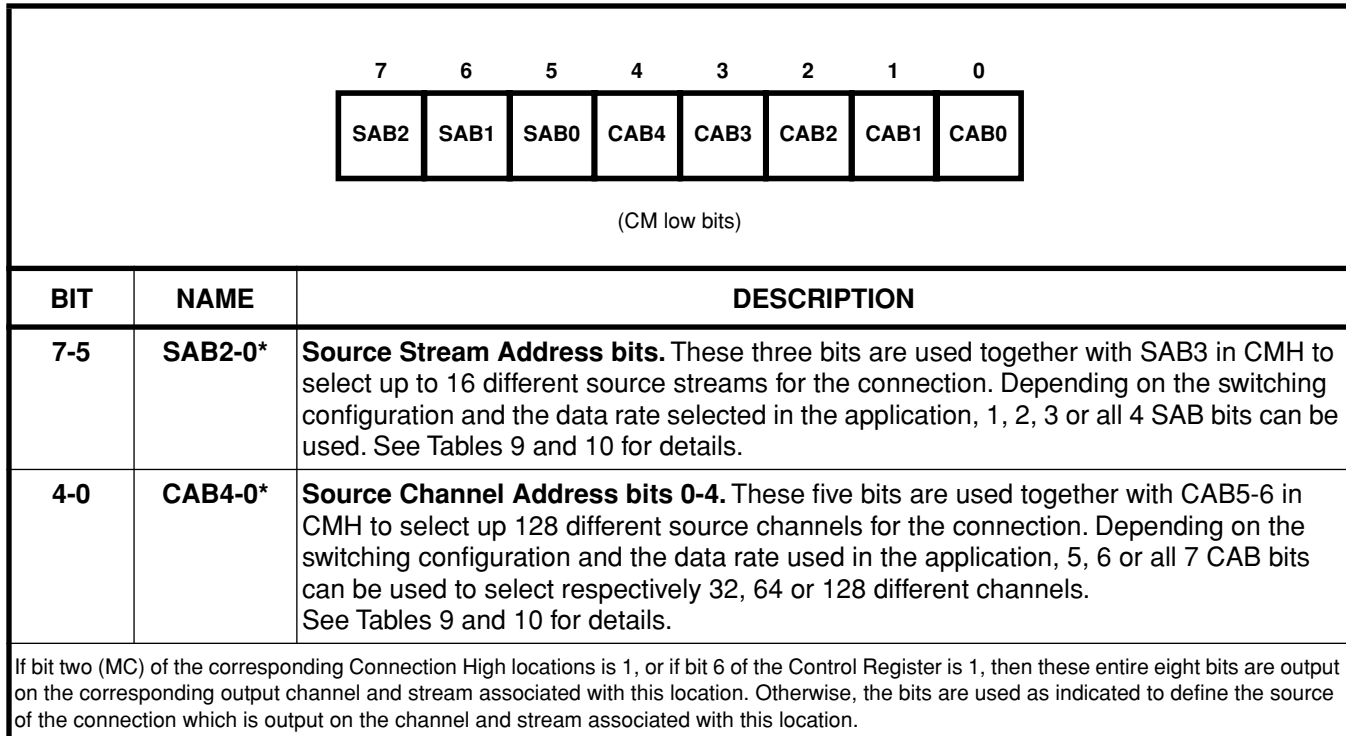


Figure 6 - Connection Memory Low (CML) Bits

Identical I/O Rate	# of Input x Output Streams	CAB bits used to determine the source channel for the connection	SAB bits used to determine the source stream for the connection
2 Mb/s	8x8	CAB4 to CAB0 (32 channel/inp. stream)	SAB2, SAB1, SAB0
2 Mb/s *	4x4 *	CAB4 to CAB0 (32 channel/inp. stream)	SAB2, SAB1
2 Mb/s *	16x8 *	CAB4 to CAB0 (32 channel/inp. stream)	SAB3, SAB2, SAB1, SAB0
4 Mb/s	4x4	CAB5 to CAB0 (64 channel/inp. stream)	SAB2, SAB1
4 Mb/s	8x4	CAB5 to CAB0 (64 channel/inp. stream)	SAB2, SAB1, SAB0
8 Mb/s	2x2	CAB6 to CAB0 (128 channel/inp. stream)	SAB2
Nibble Switch (2 Mb/s)	8x4	CAB5 to CAB0 (64 nibble/inp. stream)	SAB2, SAB1, SAB0

Table 9. CAB and SAB Bits Programming for Identical I/O Rate Applications

\* - only in 44 pin package

Different I/O Rate	# of Input x Output Streams	CAB bits used to determine the source channel for the connection	SAB bits used to determine the source stream for the connection
2 Mb/s to 4 Mb/s	8x4	CAB4 to CAB0 (32 channel/inp. stream)	SAB2, SAB1, SAB0
2 Mb/s to 8 Mb/s	8x2	CAB4 to CAB0 (32 channel/inp. stream)	SAB2, SAB1, SAB0
4 Mb/s to 2 Mb/s	4x8	CAB5 to CAB0 (64 channel/inp. stream)	SAB2, SAB1
8 Mb/s to 2 Mb/s	2x8	CAB6 to CAB0 (128 channel/inp. stream)	SAB2

Table 10. CAB and SAB Bits Programming for Different I/O Rate Applications

## Stream Pair Selection Register - Read/Write (ONLY PROVIDED IN THE 44 PIN PACKAGES)

<div>76543210</div> <div><div>X</div><div>X</div><div>SPA2</div><div>SPA1</div><div>SPA0</div><div>SPB2</div><div>SPB1</div><div>SPB0</div></div>							
BIT	NAME	DESCRIPTION					
5-3	SPA2-0	<b>Stream Pair A selection.</b> These three bits define which pair of streams are going to be connected to the switch matrix, together with the permanently connected streams STi0-1 / STo0-1.					
		<u>SPA2</u>	<u>SPA1</u>	<u>SPA0</u>	<u>Stream Pair A Connected</u>		
		0	0	0	STi2 / STo2		
		0	0	1	STi3 / STo3		
		0	1	0	STi4 / STo4		
		0	1	1	STi5 / STo5		
		1	0	0	STi6 / STo6		
		1	0	1	STi7 / STo7		
		1	1	0	STi8 / STo8		
		1	1	1	STi9 / STo9		
2-0	SPB2-0	<b>Stream Pair B selection.</b> These three bits define which pair of streams are going to be connected to the switch matrix, together with the permanently connected streams STi0-1 / STo0-1.					
		<u>SPB2</u>	<u>SPB1</u>	<u>SPB0</u>	<u>Stream Pair B Connected</u>		
		0	0	0	STi2 / STo2		
		0	0	1	STi3 / STo3		
		0	1	0	STi4 / STo4		
		0	1	1	STi5 / STo5		
		1	0	0	STi6 / STo6		
		1	0	1	STi7 / STo7		
		1	1	0	STi8 / STo8		
		1	1	1	STi9 / STo9		
These bits are only used when the Switching Configuration bits enable stream pair selection capability (SCB 1-0 =10) and the Input Data Rate Selection bits enable 2 Mb/s operation (IDR-0 = 00). In all other modes, the contents of this register are ignored.							

Figure 7 - Stream Pair Selection (SPS) Register

x=Don't care

## Frame Input Offset Register - Read/Write

<div><div>76543210</div><div>OFB2OFB1OFB0XXXXXX</div></div>							
BIT	NAME	DESCRIPTION					
7-5	OFB2-0	Offset Bits 2-0. These three bits define the time it takes the Serial Interface receiver to recognize and store the first bit of the serial input streams; i.e., to start assuming a new internal frame. The input frame offset can be selected to be up to 4 CK clock periods from the time when frame pulse input signal is applied to the FR input.					
		OFB2	OFB1	OFB0	Number of Clock Periods		
		0	0	0	Normal Operation. No bit offsetting.		
		0	0	1	1		
		0	1	0	2		
		0	1	1	3		
		1	0	0	4		
		1	0	1	Reserved		
		1	1	0	Reserved		
		1	1	1	Reserved		
If frame input offset operation is not required, this register should be cleared by the CPU during system initialization.							

Figure 8 - Frame Input Offset (FIO) Register

x=Don't care

Applications

Switch Matrix Architectures

The MT8986 is an ideal device for designs of medium size switch matrix. For applications where voice and grouped data channels are transported within the same frame, the voice samples have to be time interchanged with a minimum delay while maintaining the integrity of grouped data. To guarantee the integrity of grouped data during switching and to provide a minimum delay for voice connections, the MT8986 provides the per-channel selection between variable and constant throughput

delay. This can be selected by the  $\nabla/C$  bit of the Connection Memory High locations.

Different connectivities at different data rates can be built to accommodate Non-Blocking matrices of up to 512 channels while maintaining the per channel selection of the device's throughput delay. Some examples of such Non-Blocking configurations are given in Figures 9 to 11.

For applications where voice and data samples are encoded into individual 64 kb/s time-slots on an 8kHz frame basis, the switch matrix can operate with time interchange procedures where only variable

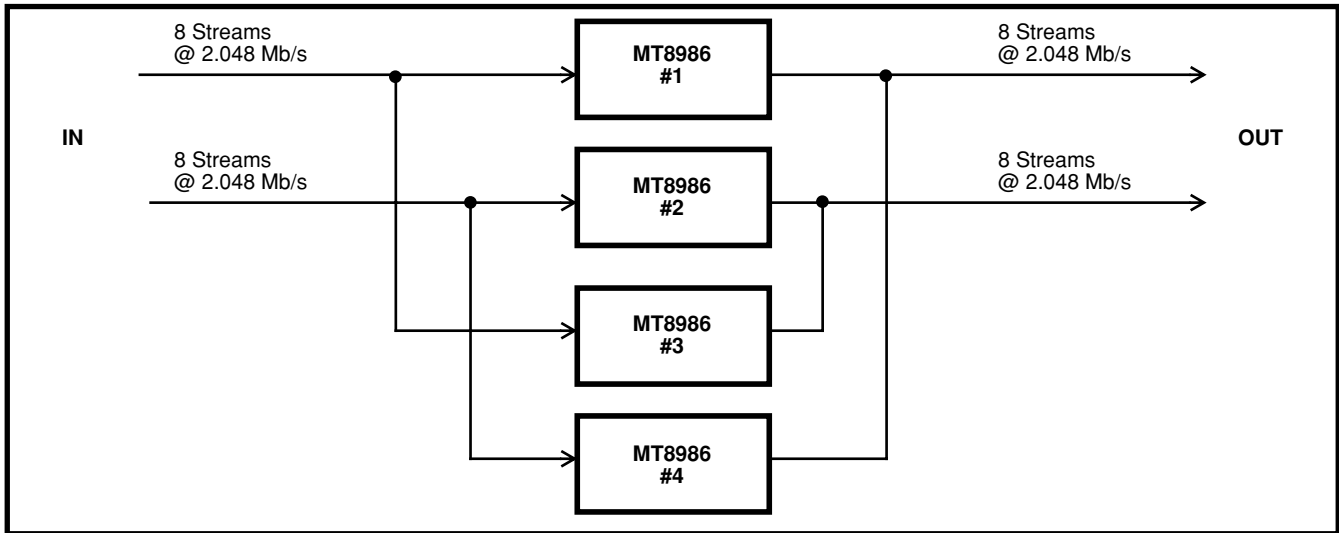


Figure 9 - 512-Channel Switch with Serial Streams at 2.048 Mb/s

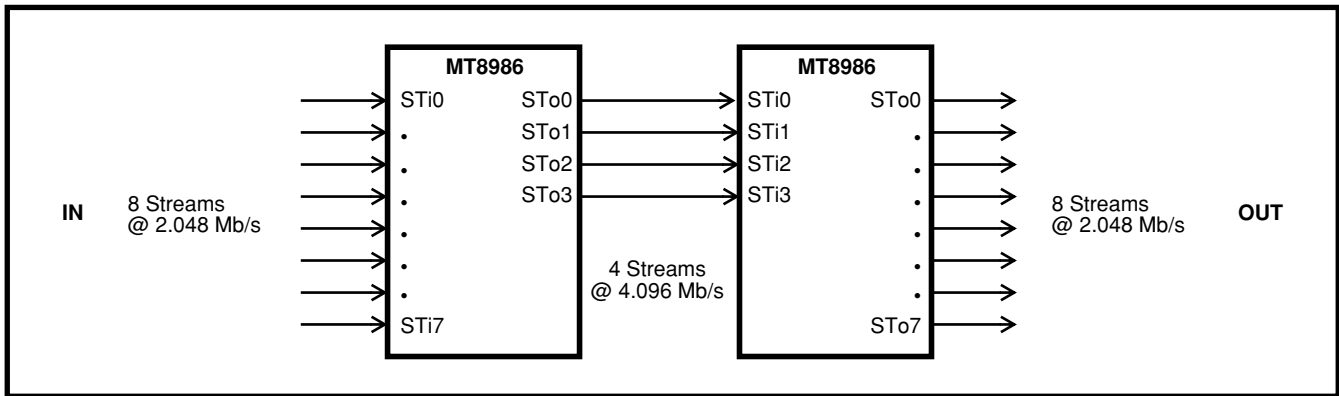


Figure 10 - 256-Channel Switch with Rate Conversion between 2.048 and 4.096 Mb/s

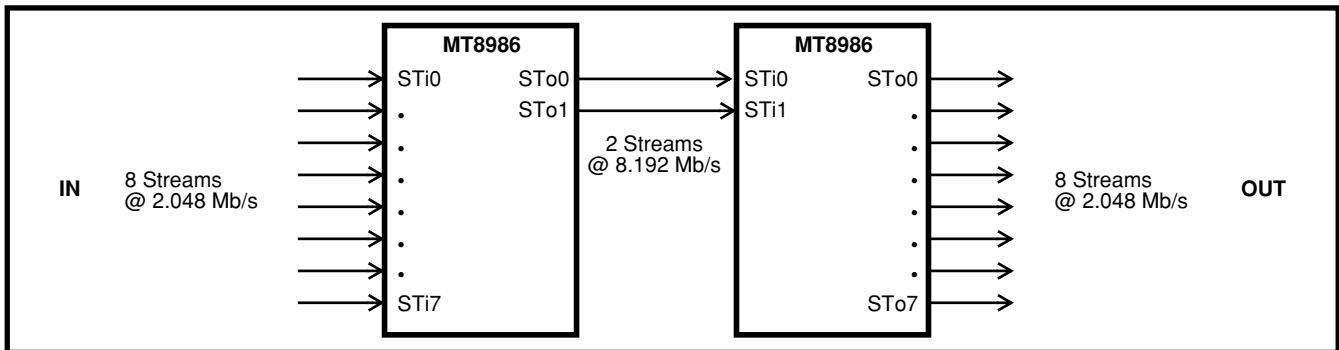


Figure 11 - 256-Channel Switch with Rate Conversion between 2.048 and 8.192 Mb/s

throughput delay is guaranteed. For such applications, the MT8986 device allows cost effective implementations of Non-Blocking matrices ranging up to 1024 channels. Figures 12 and 13 show the block diagram of implementations with Non-Blocking capacities of 512 and 1024-channel, respectively.

## Interfacing MT8986 with 8051

The Intel 8051 is a very cost effective solution for many applications that do not require a large CPU interaction and processing overhead. However, in applications where 8051 is connected to peripherals operating on a synchronous 8 kHz time-base like the MT8986, some connectivity issues have to be addressed. The MT8986 may hold the CPU read/write cycle due to internal contention between the MT8986 microport and the internal serial to parallel and parallel to serial converters. Since the 8051

family of CPUs do not provide Data Ready type of inputs, some external logic and software intervention have to be provided between the MT8986 and the 8051 microcontrollers to allow read/write operation. The external logic described in Figure 14 is a block diagram of a logical connection between MT8986 and 8051. Its main function is to store the 8051 data during a write and the MT8986 data during a read.

For a write, MT8986 address is latched by the internal address latch on the falling edge of the ALE input. Whenever a read or write operation is done to the MT8986 device, the address decoded signal ( $\overline{MTA}$ ) is used to latch or "freeze" the state of  $\overline{RD}$ ,  $\overline{WR}$ , and the ALE signals, until the data acknowledge output signal is provided by the MT8986 device, releasing the latches for a new read/write cycle. Latch U5 is used to hold the 8051 data for a write until the CPU is ready to accept it (when  $\overline{DTA}$  goes low). Latch U4 stores the MT8986 output data

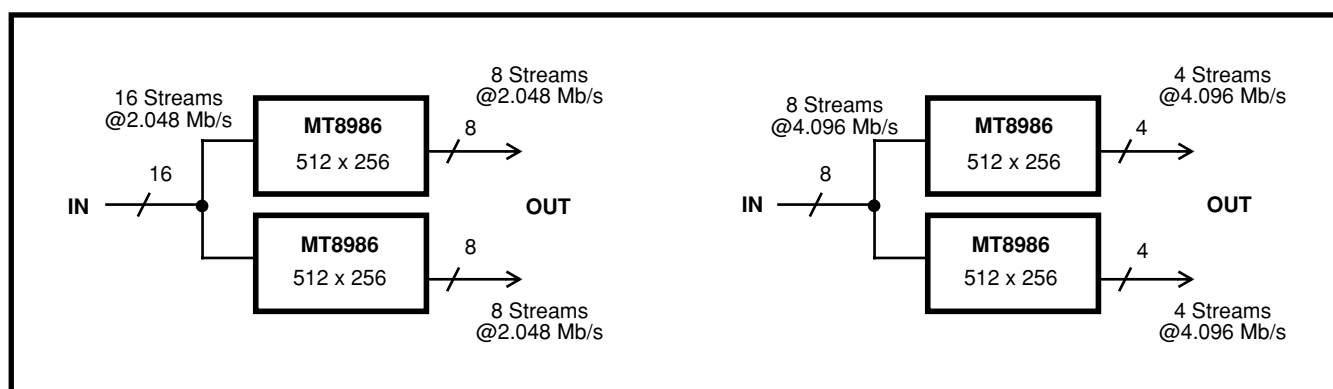


Figure 12 - 512-Channel Non-Blocking Switch Matrix with Serial Streams at 2.048 or 4.096 Mb/s

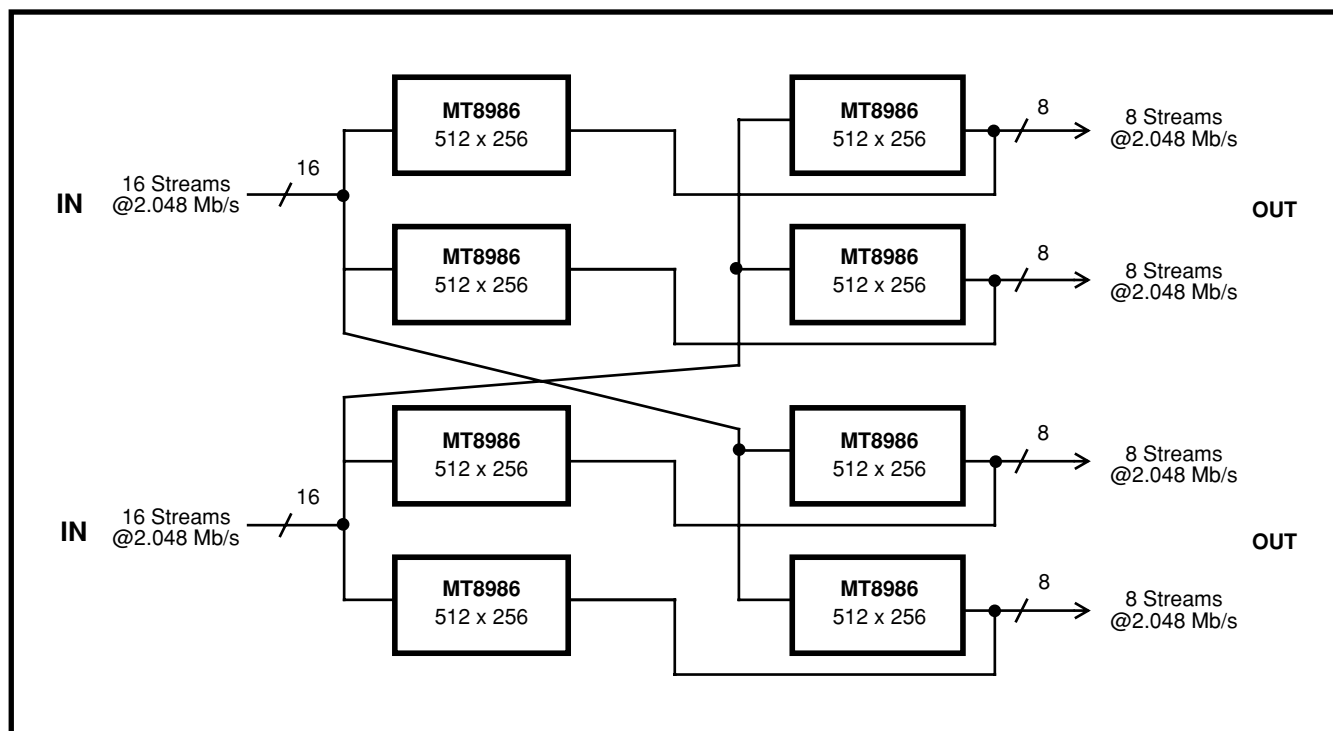
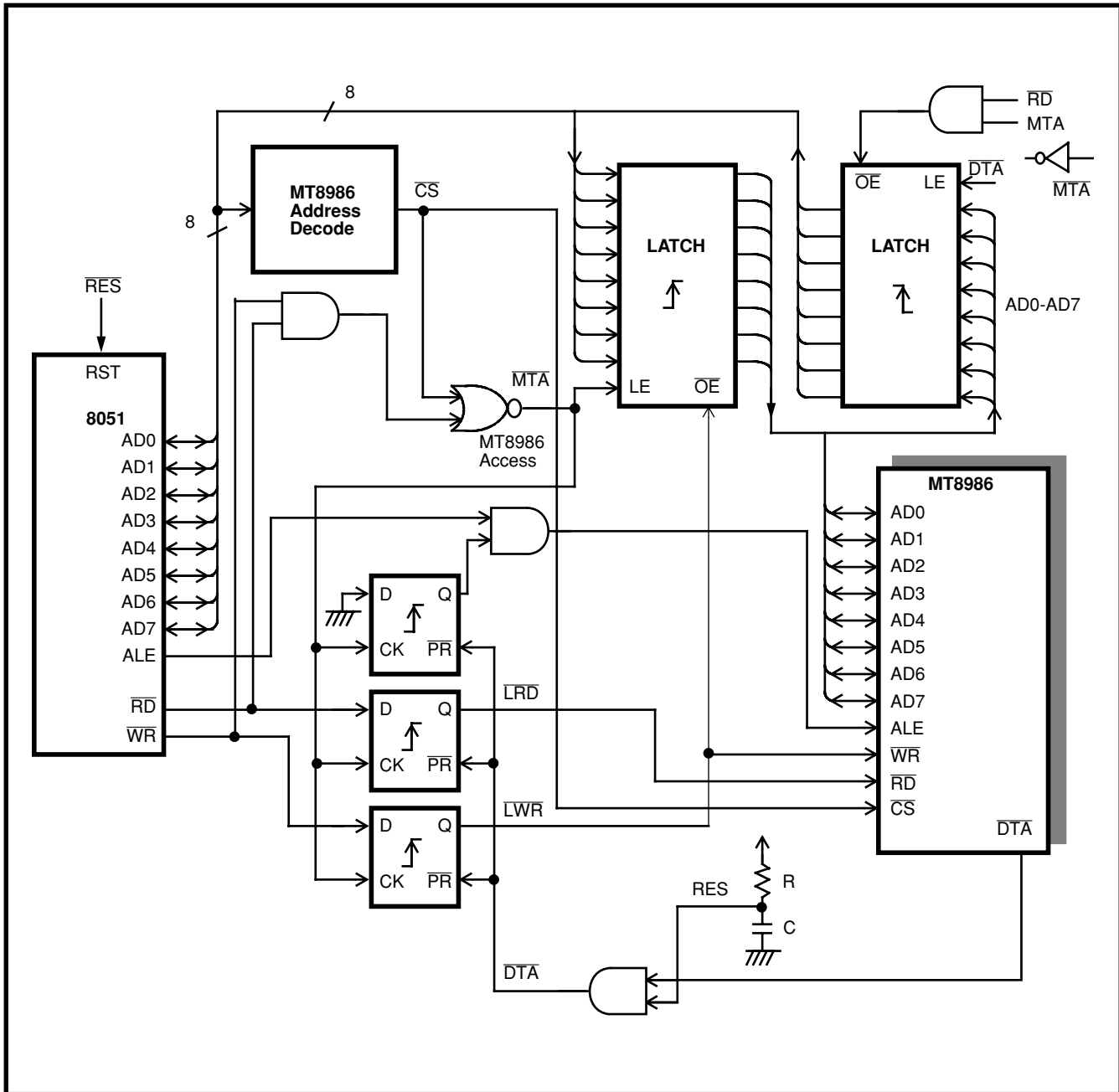


Figure 13 - 1024-Channel Non-Blocking Switch Matrix with Serial Streams at 2.048 Mb/s



### Figure 14 - Interfacing the MT8986 to the 8051 Microcontroller

during a read cycle whenever  $\overline{DTA}$  goes low. When writing to the MT8986, one write operation is sufficient. However, when reading MT8986, two read operations with the same address are required, with the second being valid.

Enough time need to be provided between two CPU accesses to allow the first access to complete; i.e., to allow for an internal MT8986 reaction over the first  $\overline{\text{RD}}/\overline{\text{WR}}$  access. For a read operation, a minimum of 1220 ns have to be guaranteed between two successive accesses. For write, at least 800 ns has to be respected.

**Absolute Maximum Ratings\***

	Parameter	Symbol	Min	Max	Units
1	$V_{DD} - V_{SS}$		-0.3	7	V
2	Voltage on Digital Inputs	$V_I$	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Voltage on Digital Outputs	$V_O$	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current at Digital Outputs	$I_O$		40	mA
5	Storage Temperature	$T_S$	-65	+150	°C
6	Package Power Dissipation	$P_D$		2	W

\* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

**Recommended Operating Conditions** - Voltages are with respect to ground ( $V_{SS}$ ) unless otherwise stated.

	Characteristics	Sym	Min	Typ <sup>‡</sup>	Max	Units	Test Conditions
1	Operating Temperature	$T_{OP}$	-40	25	+85	°C	
2	Positive Supply	$V_{DD}$	4.75	5.0	5.25	V	
3	Input Voltage	$V_I$	0		$V_{DD}$	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

**DC Electrical Characteristics** - Voltages are with respect to ground ( $V_{SS}$ ) unless otherwise stated.

	Characteristics	Sym	Min	Typ <sup>‡</sup>	Max	Units	Test Conditions
1	INPUTS	Supply Current	$I_{DD}$	10	15	mA	Outputs unloaded
2		Input High Voltage	$V_{IH}$	2.0		V	
3		Input Low Voltage	$V_{IL}$		0.8	V	
4		Input Leakage (input pins) Input Leakage (I/O pins)	$I_{IL}$	34	5 100	μA	$V_I$ between $V_{SS}$ and $V_{DD}$
5		Input Pin Capacitance	$C_I$	8		pF	
6	OUTPUTS	Output High Voltage	$V_{OH}$	2.4		V	$I_{OH} = 10$ mA
7		Output High Current	$I_{OH}$	10	15	mA	Sourcing. $V_{OH}=2.4$ V
8		Output Low Voltage	$V_{OL}$		0.4	V	$I_{OL} = 5$ mA
9		Output Low Current	$I_{OL}$	5	10	mA	Sinking. $V_{OL} = 0.4$ V
10		High Impedance Leakage	$I_{OZ}$		5	μA	$V_O$ between $V_{SS}$ and $V_{DD}$
11		Output Pin Capacitance	$C_O$	8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

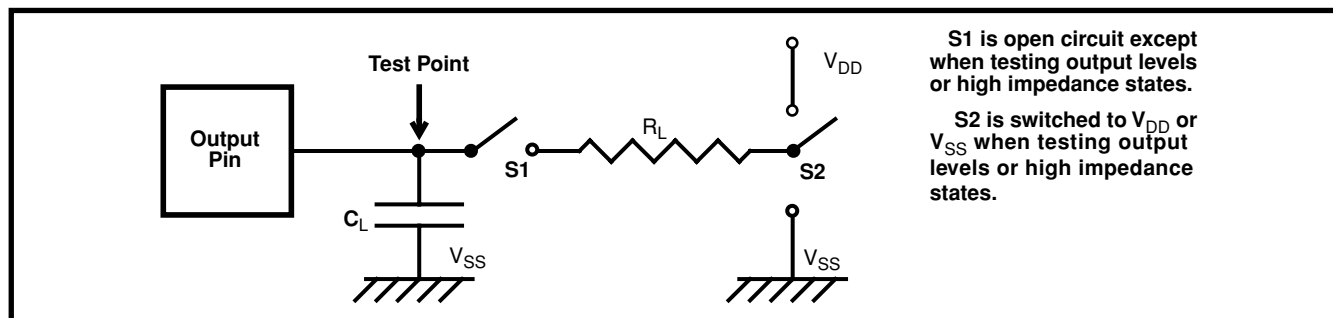


Figure 15 - Output Test Load

AC Electrical Characteristics† – ST-BUS Timing (2.048 Mb/s)

Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Frame Pulse width	t <sub>FRW</sub>		244		ns	
2	Frame Pulse setup time	t <sub>FRS</sub>	10		190	ns	
3	Frame Pulse hold time	t <sub>FRH</sub>	20		190	ns	
4	STo delay Active to Active	t <sub>DAA</sub>		45	100	ns	C <sub>L</sub> =150 pF
5	STi setup time	t <sub>STIS</sub>	20			ns	
6	STi hold time	t <sub>STIH</sub>	20			ns	
7	Clock period	t <sub>CLK</sub>	190	244	300	ns	
8	CK Input Low	t <sub>CL</sub>	85	122	150	ns	
9	CK Input High	t <sub>CH</sub>	85	122	150	ns	
10	Clock Rise/Fall Time	t <sub>r</sub> ,t <sub>f</sub>			10	ns	

† Timing is over recommended temperature & power supply voltages (V<sub>DD</sub>=5V±5%, V<sub>SS</sub>=0V, T<sub>A</sub>=−40 to 85°C).

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

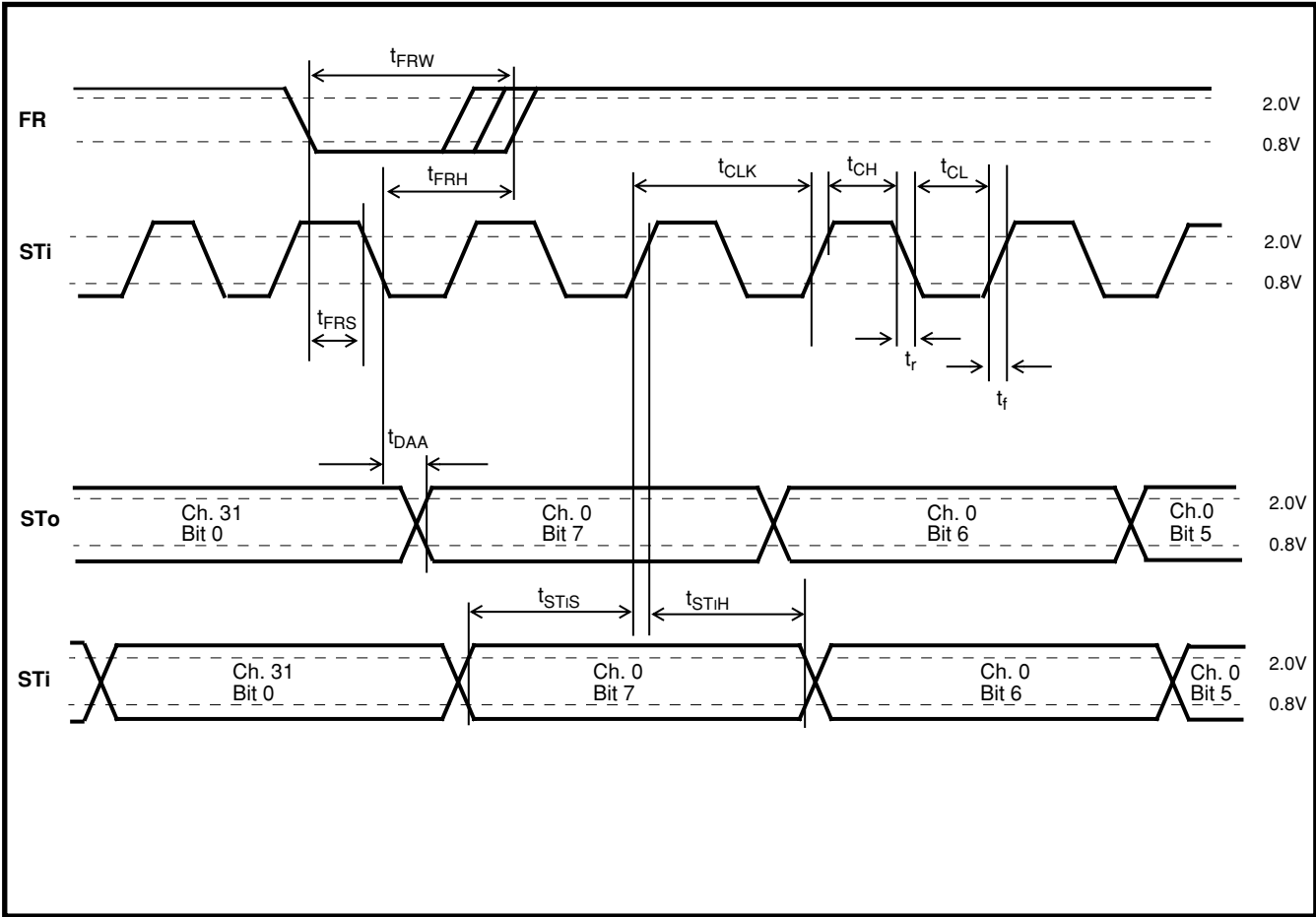


Figure 16 - ST-BUS Timing (CLKM bit=0)



**AC Electrical Characteristics<sup>†</sup> - GCI Timing (2.048 Mb/s)**

Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Min	Typ <sup>‡</sup>	Max	Units	Test Conditions
1	Clock Period	$t_{CK}$	150	244	300	ns	
2	Pulse Width	$t_{CL}$ , $t_{CH}$	73	122	150	ns	
3	Frame Width High	$t_{WFH}$		244		ns	
4	Frame Setup	$t_{FRS}$	10		190	ns	
5	Frame Hold	$t_{FRH}$	20		190	ns	
6	Data Delay/Clock Active to Active	$t_{DAA}$		45	100	ns	$C_L=150$ pF
7	Serial Input Setup	$t_{STIS}$	20			ns	
8	Serial Input Hold	$t_{STIH}$	20			ns	
9	Clock Rise/Fall Time	$t_r$ , $t_f$			10	ns	

<sup>†</sup> Timing is over recommended temperature & power supply voltages ( $V_{DD}=5V\pm5\%$ ,  $V_{SS}=0V$ ,  $T_A=-40$  to  $85^\circ\text{C}$ ).

<sup>‡</sup> Typical figures are at  $25^\circ\text{C}$  and are for design aid only: not guaranteed and not subject to production testing.

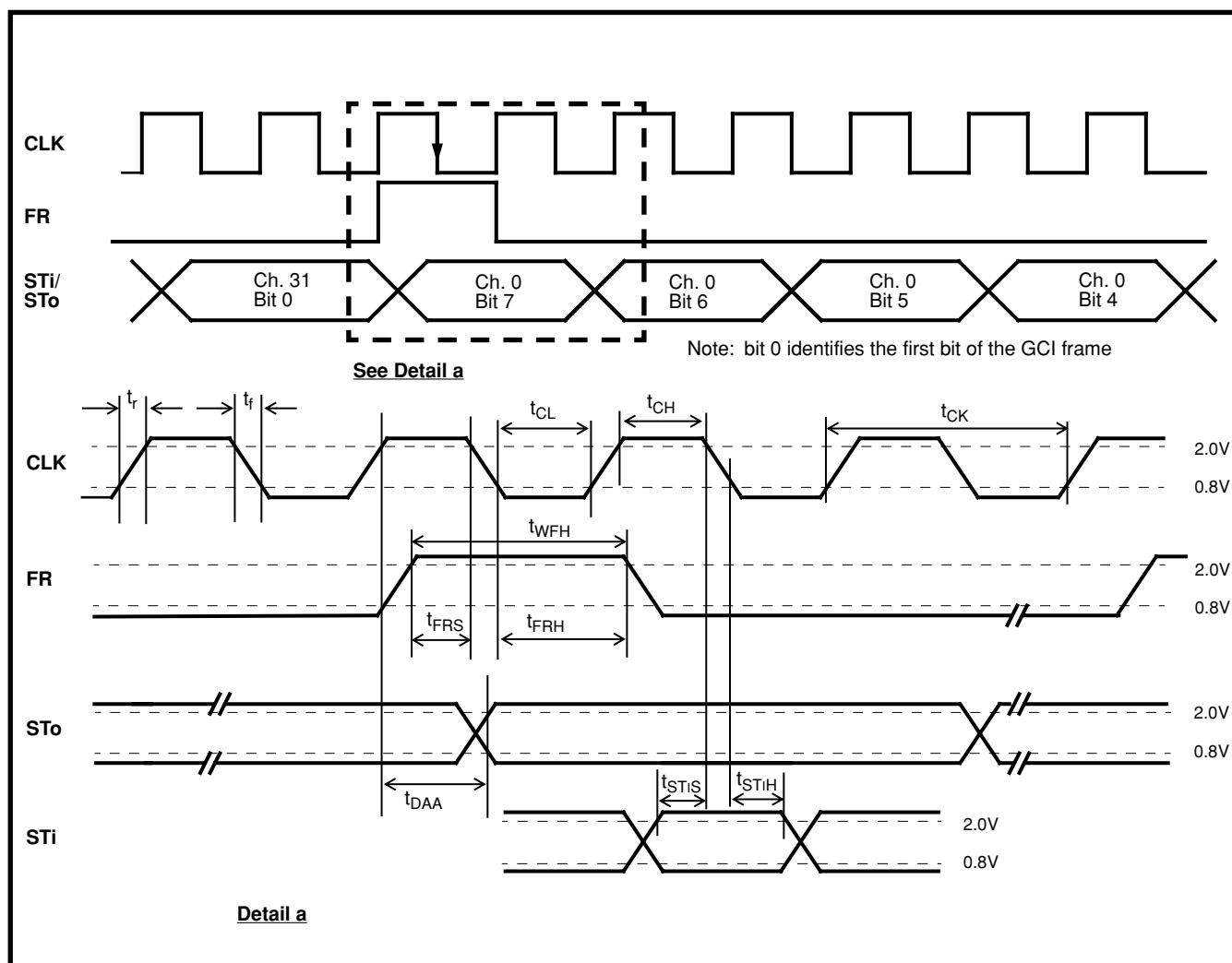


Figure 17 - GCI Timing (CLKM bit=0)

## AC Electrical Characteristics<sup>†</sup> - Serial Streams for ST-BUS and GCI Backplanes (2.048 Mb/s)

		Characteristics	Sym	Min	Typ <sup>‡</sup>	Max	Units	Test Conditions
1	O U T P U T S	STo0/9 Delay - Active to High Z	$t_{SAZ}$			100	ns	$R_L=1\text{ K}\Omega^*$ , $C_L=150\text{ pF}$
2		STo0/9 Delay - High Z to Active	$t_{SZA}$			100	ns	$C_L=150\text{ pF}$
3		Output Driver Enable Delay	$t_{OED}$			65	ns	$R_L=1\text{ K}\Omega^*$ , $C_L=150\text{ pF}$
4		CSTo Output Delay	$t_{XCD}$	0		60	ns	$C_L=150\text{ pF}$

<sup>†</sup> Timing is over recommended temperature & power supply voltages.

<sup>‡</sup> Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

\* High Impedance is measured by pulling to the appropriate rail with  $R_L$ , with timing corrected to cancel time taken to discharge  $C_L$ .

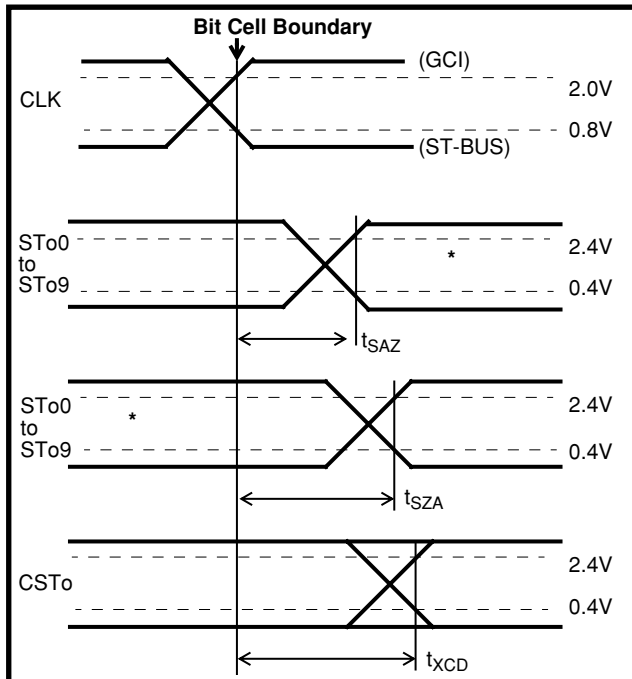


Figure 18 - Serial Outputs and External Control

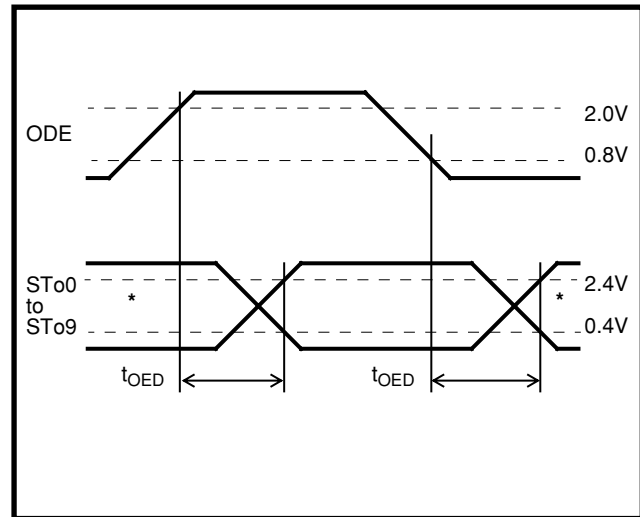


Figure 19 - Output Driver Enable

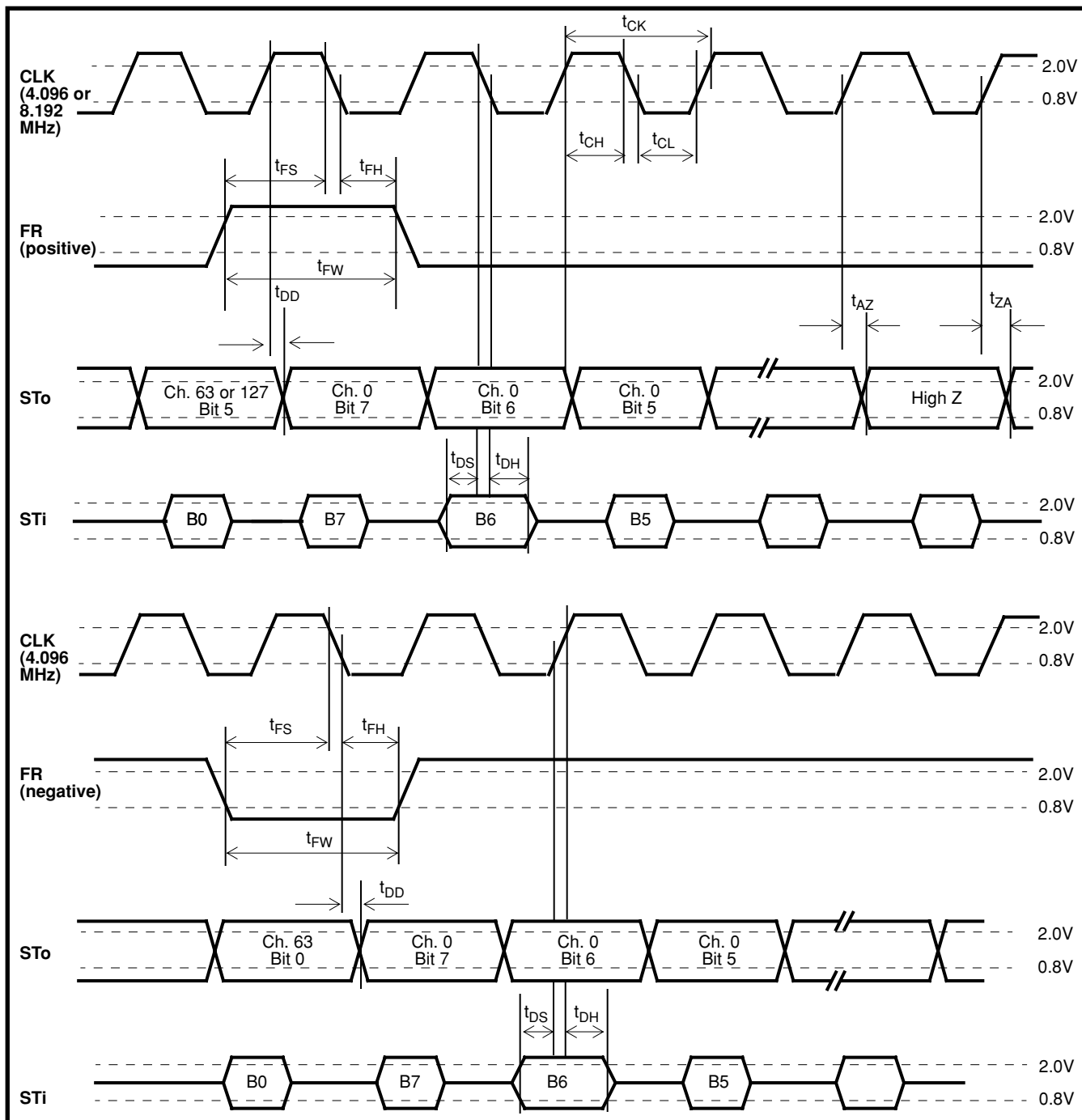
## AC Electrical Characteristics - Serial Streams at 4.096 and 8.192 Mb/s (refer to Figures 20-25)

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Clock Period	$t_{CK}$					
	4.096Mb/s		190	244	300	ns	
	8.192Mb/s		110	122	150	ns	
2	Clock Pulse High	$t_{CH}$					
	4.096Mb/s		85	122	150	ns	
	8.192Mb/s		50	60	70	ns	
3	Clock Pulse Low	$t_{CL}$					
	4.096Mb/s		85	122	150	ns	
	8.192Mb/s		50	60	70	ns	
4	Frame Sync Setup	$t_{FS}$					
	4.096Mb/s		10		190	ns	
	8.192Mb/s		10		90	ns	
5	Frame Sync Hold	$t_{FH}$					
	4.096Mb/s		20		190	ns	
	8.192Mb/s		20		90	ns	

**AC Electrical Characteristics - Serial Streams at 4.096 and 8.192 Mb/s**  
**(refer to Figures 20-25)**

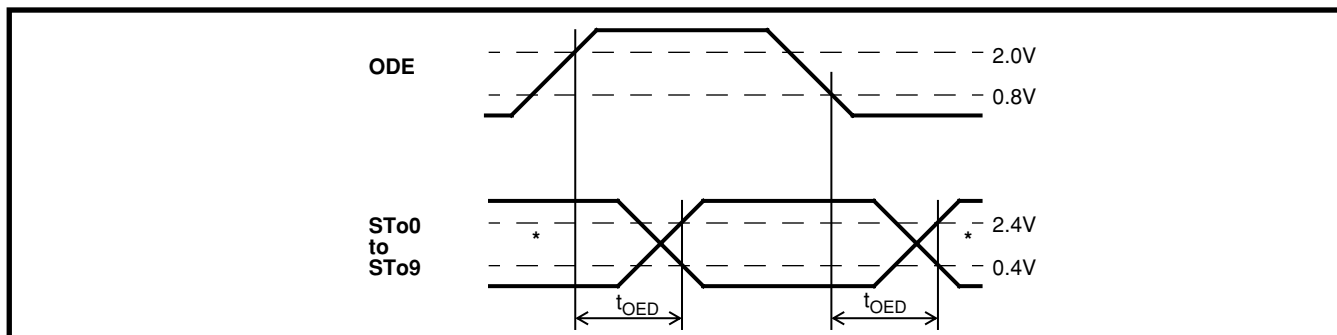
	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
6	Frame Sync Width 4.096Mb/s 8.192Mb/s	$t_{FW}$		244 122		ns ns	
7	Valid Data Delay from CK Input 4.096Mb/s 8.192Mb/s	$t_{DD}$		40 30	80 45	ns ns	$C_L=150\text{ pF}$ $C_L=50\text{ pF}$
8	Input Data Setup 4.096Mb/s 8.192Mb/s	$t_{DS}$	0 0			ns ns	
9	Input Data Hold 4.096Mb/s 8.192Mb/s	$t_{DH}$	20 20			ns ns	
10	STo Delay from Active to High Z 4.096Mb/s 8.192Mb/s	$t_{AZ}$			80 45	ns ns	$C_L=150\text{ pF}$ , $R_L=1\text{ K}\Omega^*$ $C_L=50\text{ pF}$ , $R_L=1\text{ K}\Omega^*$
11	STo Delay from High Z to Active 4.096Mb/s 8.192Mb/s	$t_{ZA}$			80 45	ns ns	$C_L=150\text{ pF}$ $C_L=50\text{ pF}$
12	Output Drive Enable Delay 4.096Mb/s 8.192Mb/s	$t_{OED}$			65 65	ns ns	$C_L=150\text{ pF}$ , $R_L=1\text{ K}\Omega^*$ $C_L=50\text{ pF}$ , $R_L=1\text{ K}\Omega^*$

\* High Impedance is measured by pulling to the appropriate rail with  $R_L$ , with timing corrected to cancel time taken to discharge  $C_L$ .



**Figure 20 - Serial Interface Timing (CLKM bit=1, DMO bit=0) - 4.096 and 8.192 Mb/s**

Note: For 8.192 Mb/s clock, only the positive polarity frame pulse is accepted by the MT8986 device.



**Figure 21 - Output Driver Enable for Streams at 4.096 and 8.192 Mb/s**

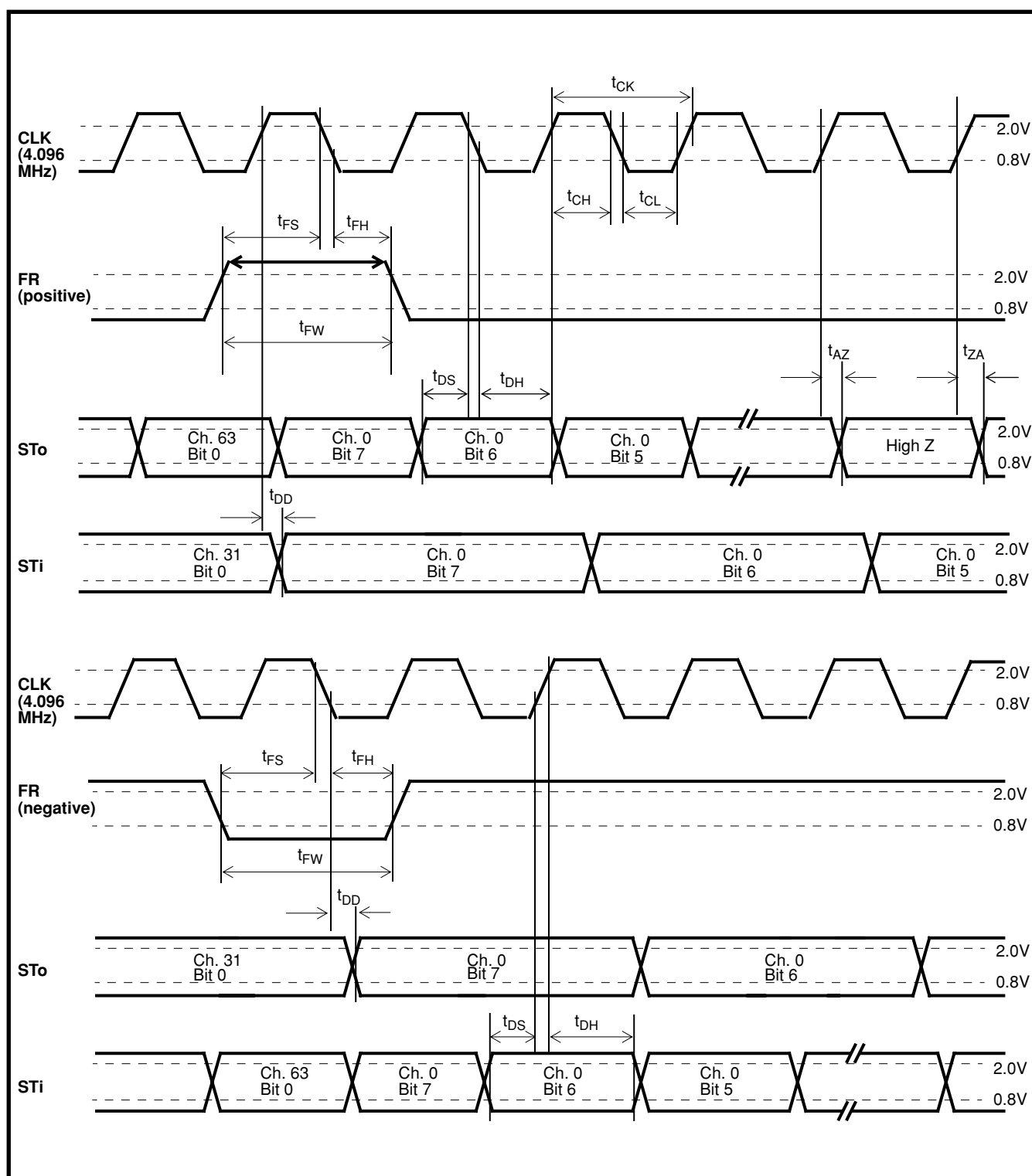


Figure 22 - Rate Conversion Mode (DMO bit=1) - 4 Mb/s to 2 Mb/s

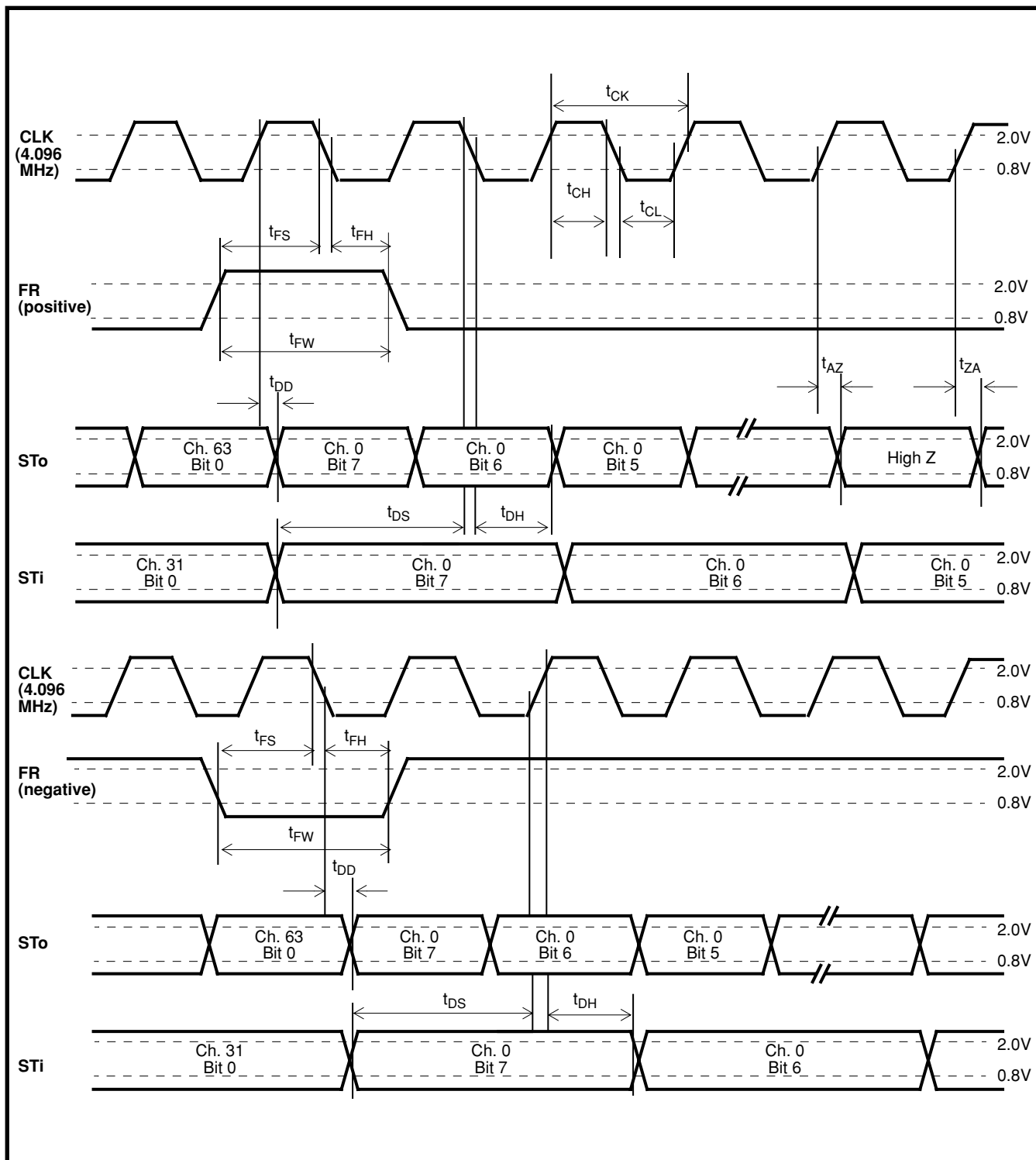


Figure 23 - Rate Conversion Mode (DMO bit=1) - 2 Mb/s to 4 Mb/s

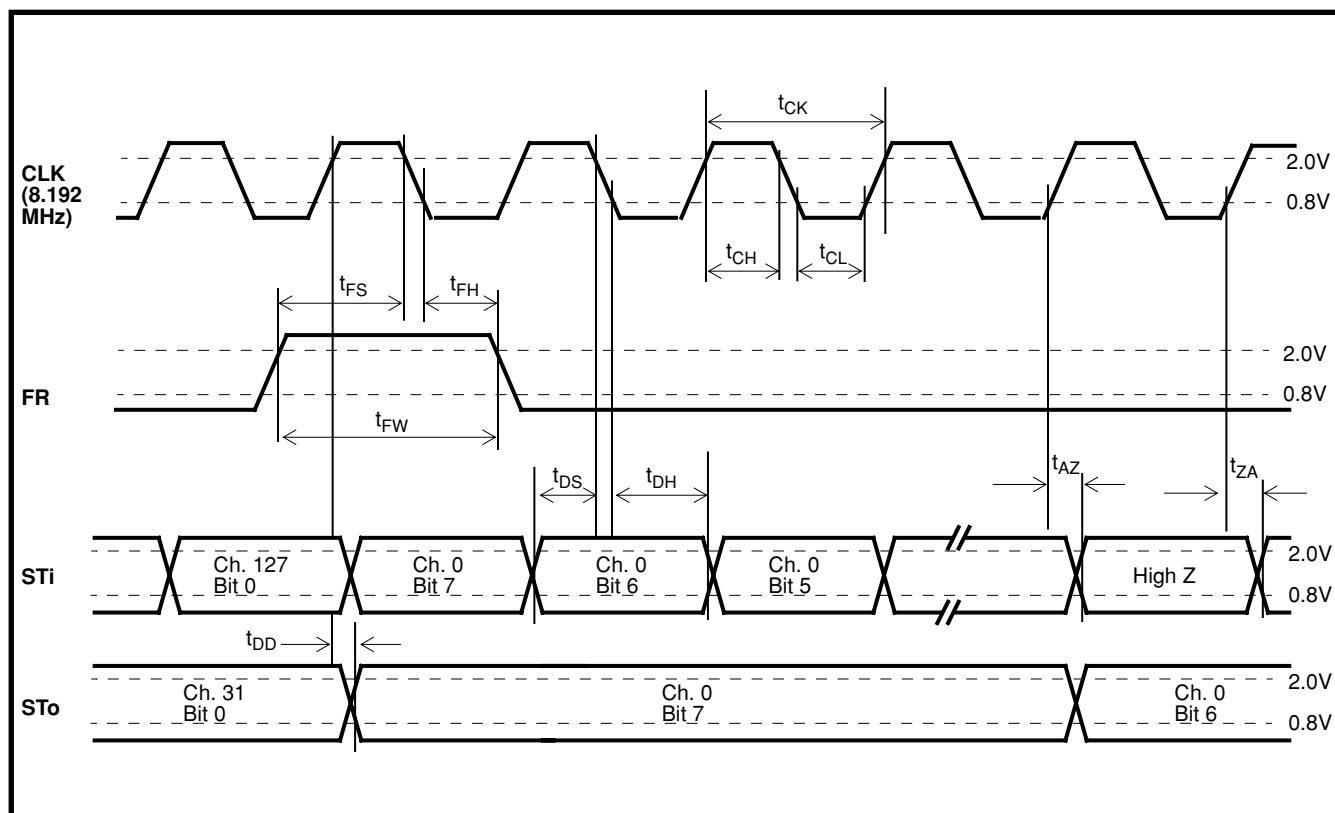


Figure 24 - Rate Conversion Mode (DMO bit=1) - 8 Mb/s to 2 Mb/s

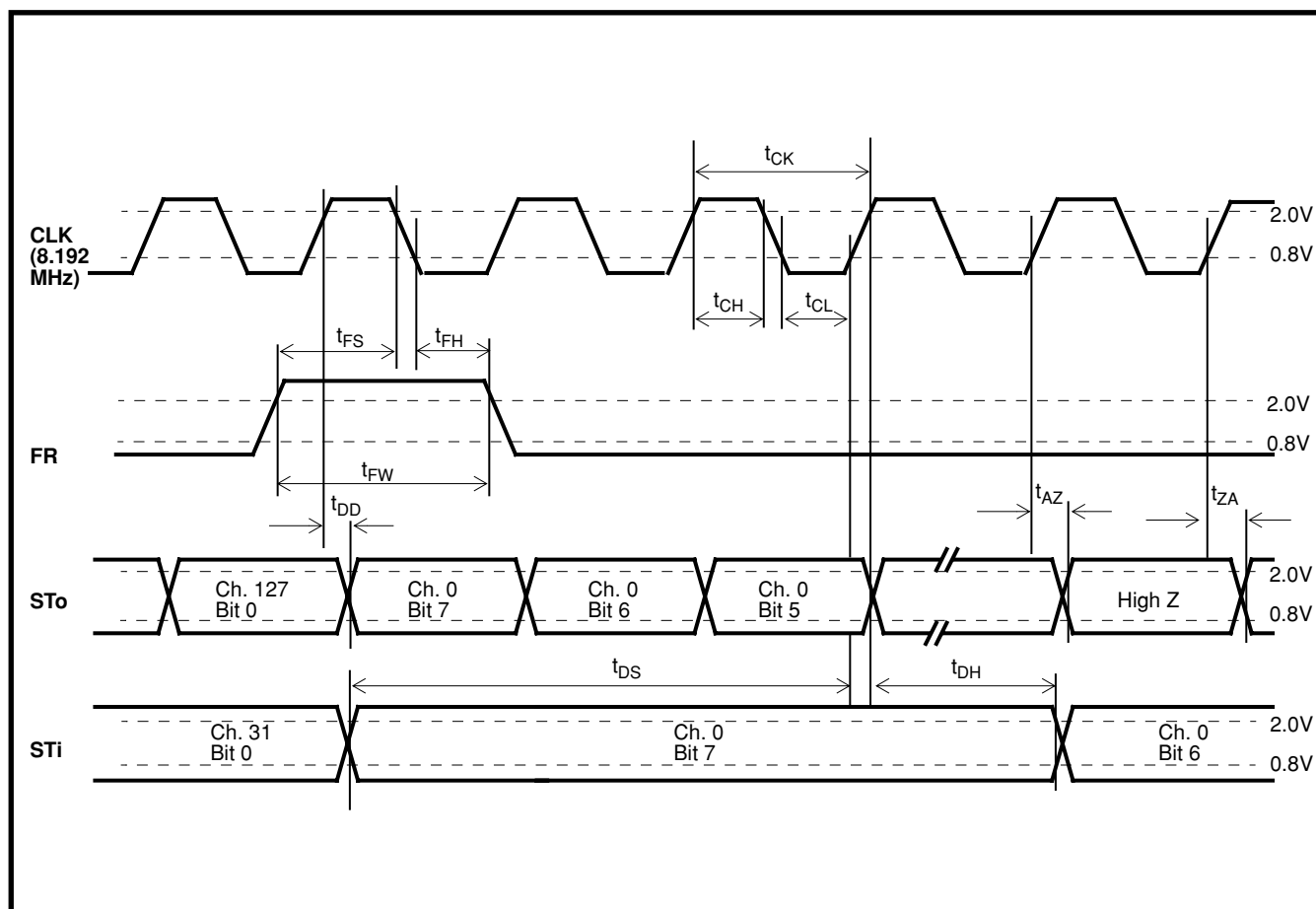


Figure 25 - Rate Conversion Mode (DMO bit=1) - 2 Mb/s to 8 Mb/s

## AC Electrical Characteristics† - Intel/National- HPC Multiplexed Bus Mode

Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ALE pulse width	$t_{ALW}$	20			ns	
2	Address setup from ALE falling	$t_{ADS}$	8			ns	
3	Address hold from ALE falling	$t_{ADH}$	9			ns	
4	$\overline{RD}$ active after ALE falling	$t_{ALRD}$	9			ns	
5	Data setup from $\overline{DTA}$ Low on Read	$t_{DDR}$	10			ns	$C_L=150$ pF
6	$\overline{CS}$ hold after $\overline{RD}/\overline{WR}$	$t_{CSRW}$	0			ns	
7	$\overline{RD}$ pulse width (fast read)	$t_{RW}$		80		ns	
8	$\overline{CS}$ setup from $\overline{RD}$	$t_{CSR}$	0			ns	
9	Data hold after $\overline{RD}$	$t_{DHR}$	10	50	90	ns	$C_L=150$ pF, $R_L=1$ K $\Omega$ *
10	$\overline{WR}$ pulse width (fast write)	$t_{WW}$		90		ns	
11	$\overline{WR}$ delay after ALE falling	$t_{ALWR}$	10			ns	
12	$\overline{CS}$ setup from $\overline{WR}$	$t_{CSW}$	0			ns	
13	Data setup from $\overline{WR}$ (fast write)	$t_{DSW}$	90			ns	
14	Valid Data Delay on write (slow write)	$t_{SWD}$			122	ns	
15	Data hold after $\overline{WR}$ inactive	$t_{DHW}$	8			ns	
16	Acknowledgement Delay: Reading Data Memory Reading/Writing Conn. Memories Writing to Control & Mode Reg. Reading from Control & Mode Reg.	$t_{AKD}$		560 300/370 47 60	1220 730/800 95 125	ns ns ns ns	$C_L=150$ pF
17	Acknowledgement Hold Time	$t_{AKH}$	10	60	110	ns	$C_L=150$ pF, $R_L=1$ K $\Omega$ *

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

\* High Impedance is measured by pulling to the appropriate rail with  $R_L$ , with timing corrected to cancel time taken to discharge  $C_L$ .



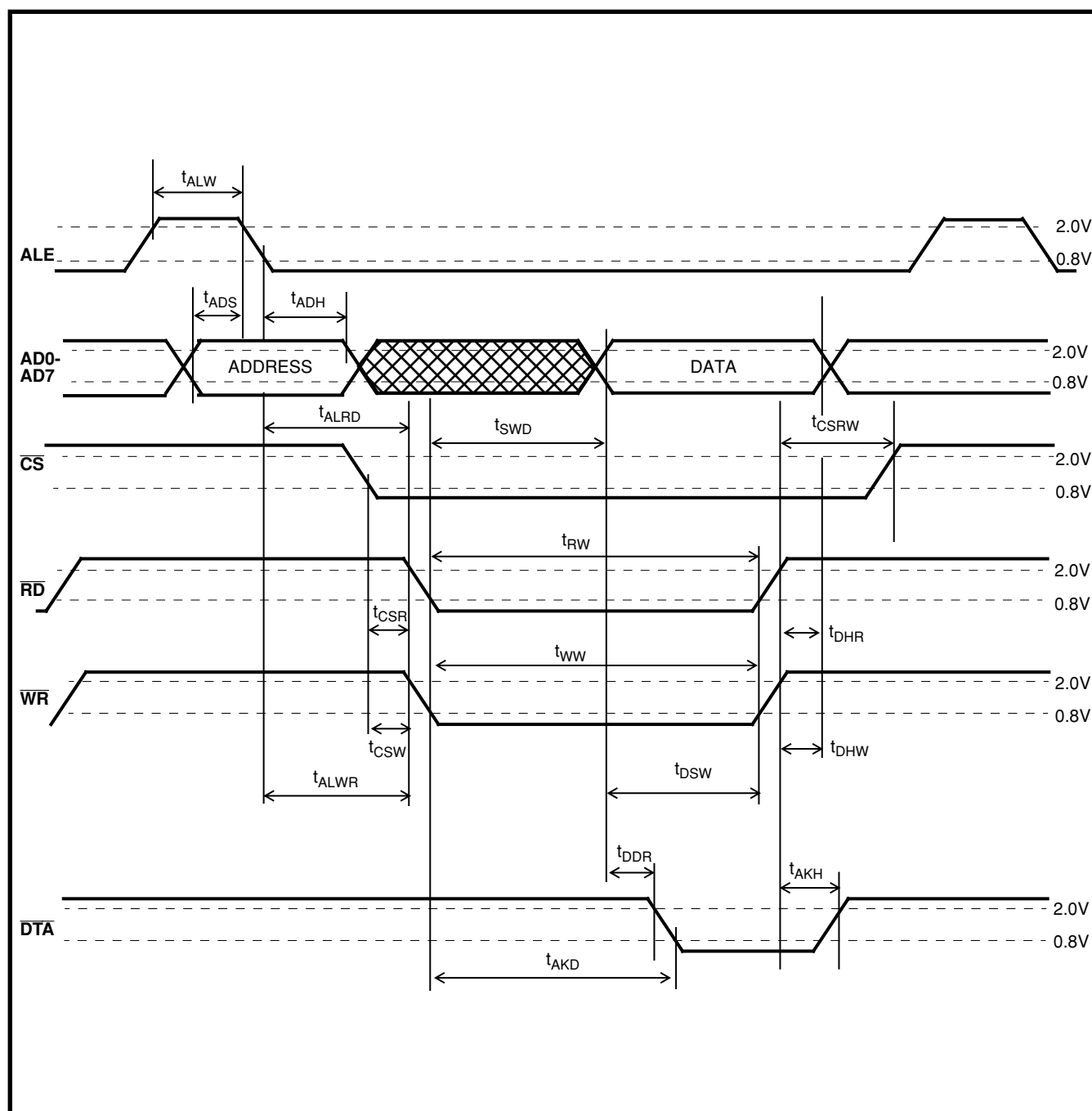


Figure 26 - Intel/National Multiplexed Bus Timing

**AC Electrical Characteristics<sup>†</sup> - Motorola Multiplexed Bus Mode**

Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Min	Typ <sup>‡</sup>	Max	Units	Test Conditions
1	AS pulse width	t <sub>ASW</sub>	80			ns	
2	Address setup from AS falling	t <sub>ADS</sub>	8			ns	
3	Address hold from AS falling	t <sub>ADH</sub>	9			ns	
4	Data setup from $\overline{DTA}$ Low on Read	t <sub>DDR</sub>	10			ns	C <sub>L</sub> =150 pF
5	$\overline{CS}$ hold after DS falling	t <sub>CSH</sub>	0			ns	
6	$\overline{CS}$ setup from DS rising	t <sub>CSS</sub>	0			ns	
7	Data hold after write	t <sub>DHW</sub>	8			ns	
8	Data setup from DS - write (fast write)	t <sub>DWS</sub>	25			ns	
9	Valid Data Delay on write (slow write)	t <sub>SWD</sub>			122	ns	
10	R/ $\overline{W}$ setup from DS rising	t <sub>RWS</sub>	60			ns	
11	R/ $\overline{W}$ hold after DS falling	t <sub>RWH</sub>	9			ns	
12	Data hold after read	t <sub>DHR</sub>	10	50	90	ns	C <sub>L</sub> =150 pF, R <sub>L</sub> =1 K $\Omega$ *
13	DS delay after AS falling	t <sub>DSH</sub>	10			ns	
14	Acknowledgement Delay: Reading Data Memory Reading/Writing Conn. Memories Writing Control & Mode Regs. Reading from Control & Mode Regs.	t <sub>AKD</sub>		560 300/370 47 73	1220 730/800 95 125	ns ns ns ns	C <sub>L</sub> =150 pF
15	Acknowledgement Hold Time	t <sub>AKH</sub>	10	60	110	ns	C <sub>L</sub> =150 pF, R <sub>L</sub> =1 K $\Omega$ *

<sup>†</sup> Timing is over recommended temperature & power supply voltages.

<sup>‡</sup> Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

\* High Impedance is measured by pulling to the appropriate rail with R<sub>L</sub>, with timing corrected to cancel time taken to discharge C<sub>L</sub>.

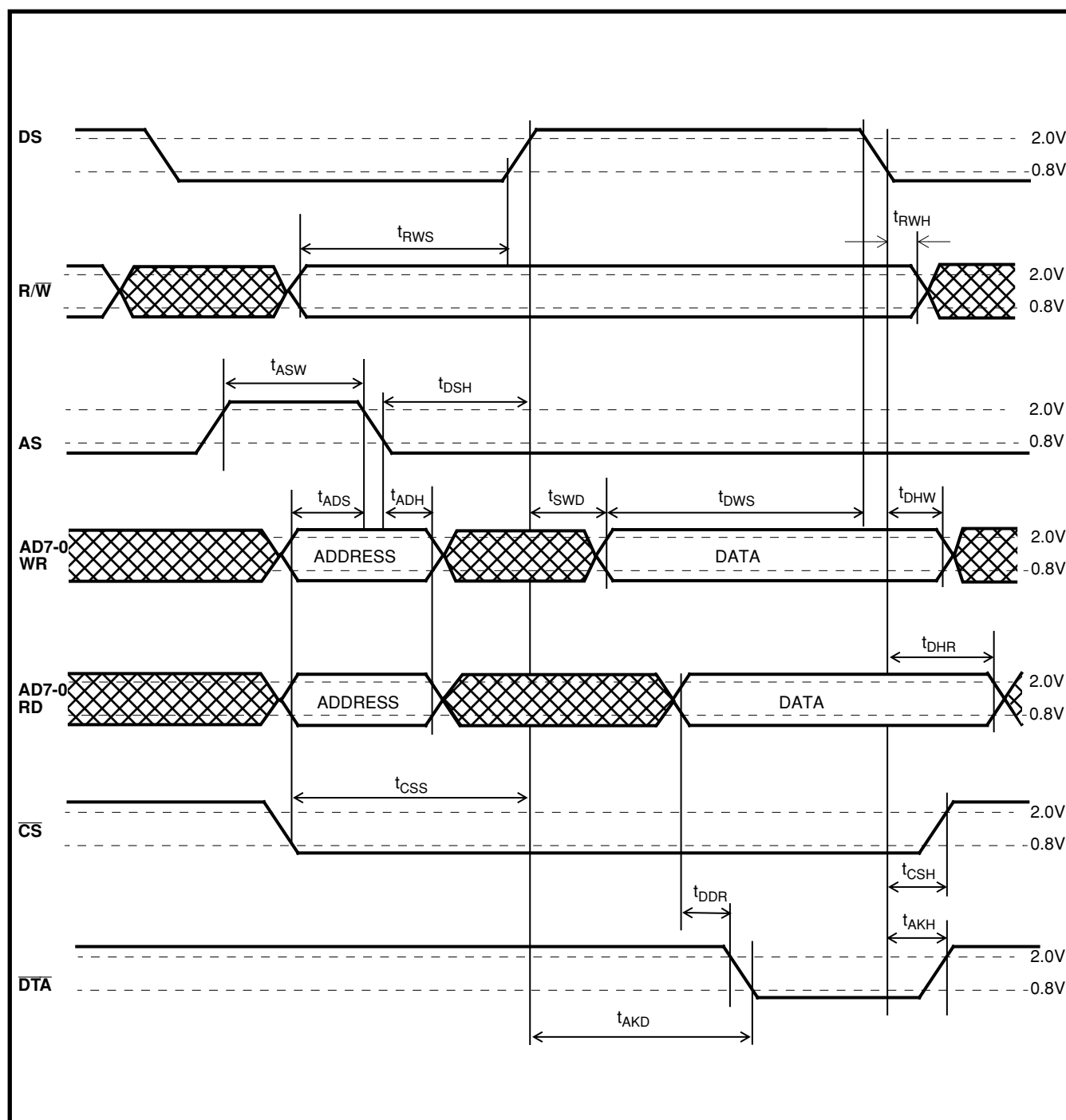


Figure 27 - Motorola Multiplexed Bus Timing

## AC Electrical Characteristics<sup>†</sup> - Motorola Non-Multiplexed Bus Mode

Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Min	Typ <sup>‡</sup>	Max	Units	Test Conditions
1	$\overline{CS}$ Setup from DS rising	$t_{CSS}$	0			ns	
2	R/ $\overline{W}$ Setup from DS rising	$t_{RWS}$	30			ns	
3	Add setup from DS rising	$t_{ADS}$	5			ns	
4	$\overline{CS}$ hold after DS falling	$t_{CSH}$	0			ns	
5	R/ $\overline{W}$ hold after DS falling	$t_{RWH}$	5			ns	
6	Add hold after DS falling	$t_{ADH}$	5			ns	
7	Data setup from $\overline{DTA}$ Low on Read	$t_{DDR}$	10			ns	$C_L=150$ pF
8	Data hold on read	$t_{DHR}$	10	50	90	ns	$C_L=150$ pF, $R_L=1$ K $\Omega^*$
9	Data setup on write (fast write)	$t_{DSW}$	20			ns	
10	Valid Data Delay on write (slow write)	$t_{SWD}$			122	ns	
11	Data hold on write	$t_{DHW}$	8			ns	
12	Acknowledgement Delay: Reading Data Memory Reading/Writing Conn. Memories Writing Control & Mode Regs. Reading from Control & Mode Regs.	$t_{AKD}$		560 300/370 47 70	1220 730/800 95 155	ns ns ns ns	$C_L=150$ pF
13	Acknowledgement Hold Time	$t_{AKH}$	10	60	110	ns	$C_L=150$ pF, $R_L=1$ K $\Omega^*$

<sup>†</sup> Timing is over recommended temperature & power supply voltages .

<sup>‡</sup> Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

\* High Impedance is measured by pulling to the appropriate rail with  $R_L$ , with timing corrected to cancel time taken to discharge  $C_L$ .

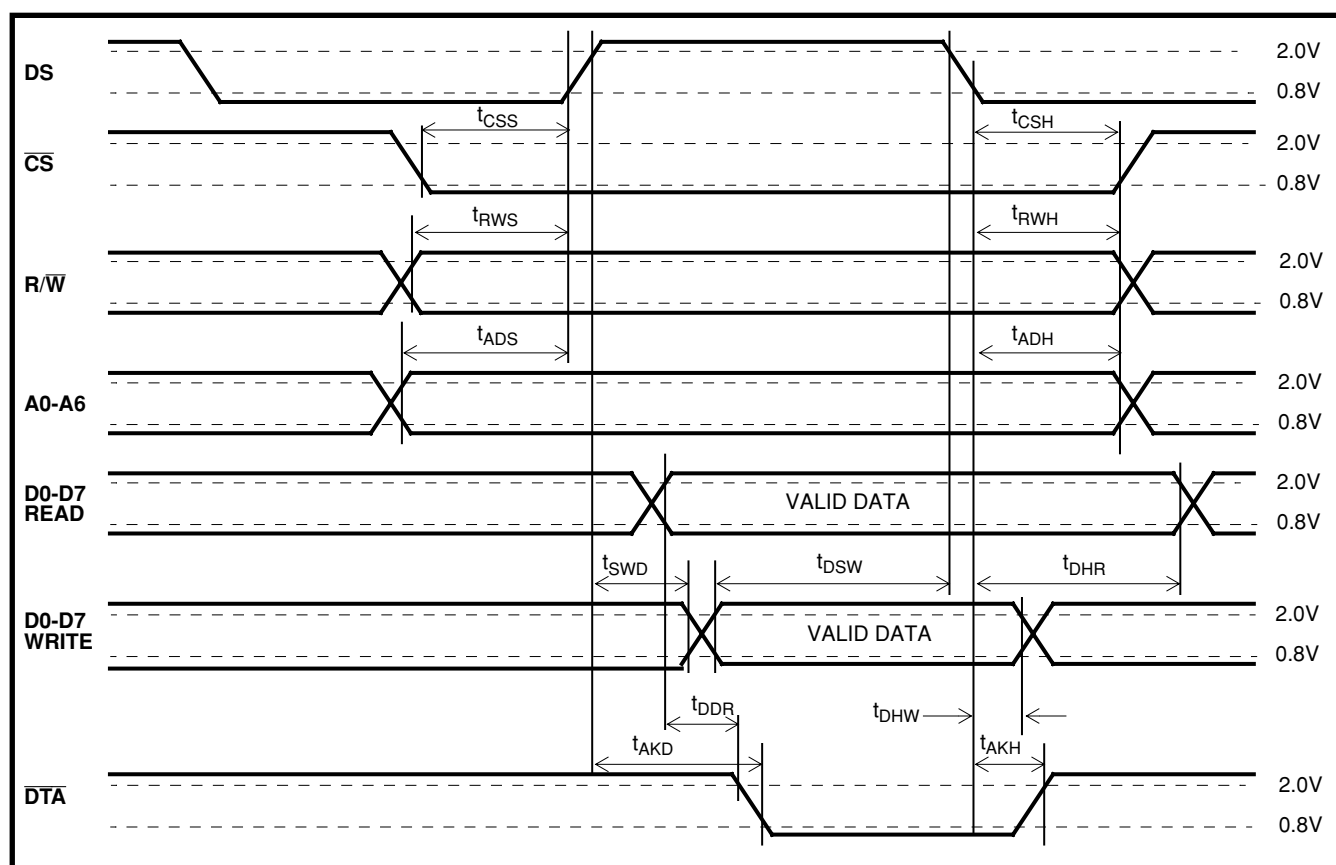
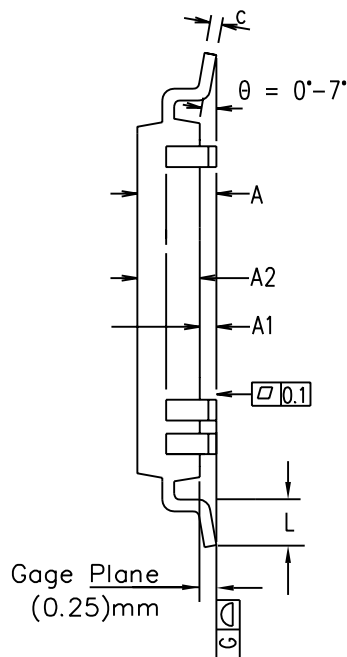
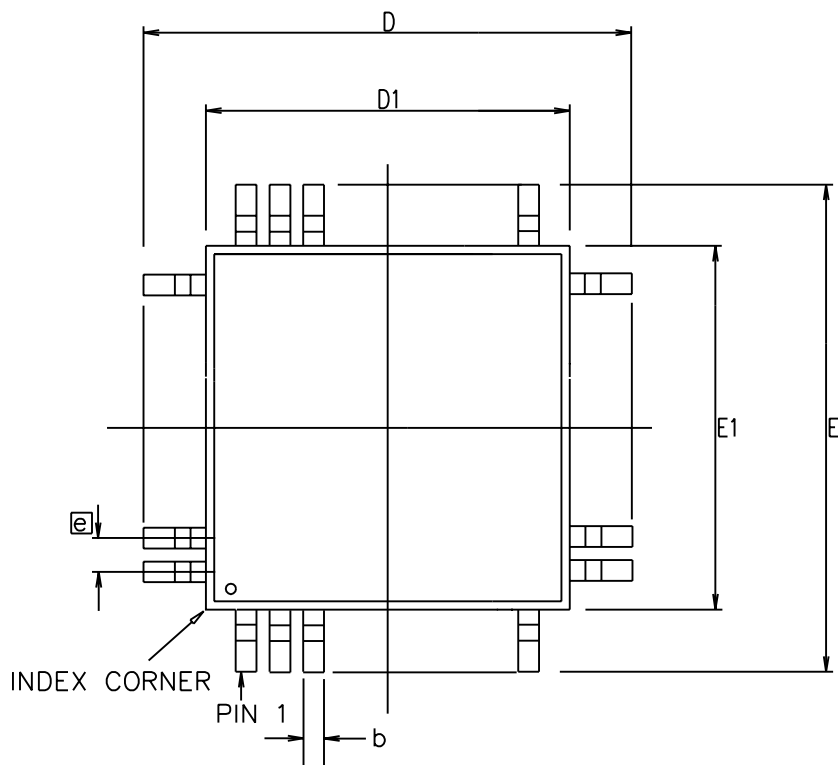


Figure 28 - Motorola Non-Multiplexed Bus Timing

Notes:



Symbol	Control Dimensions in millimetres		Altern. Dimensions in inches	
	MIN	MAX	MIN	MAX
A	—	2.45	—	0.096
A1	0.25	—	0.010	—
A2	1.95	2.10	0.077	0.083
D	13.90	BSC	0.547	BSC
D1	10.00	BSC	0.394	BSC
E	13.90	BSC	0.547	BSC
E1	10.00	BSC	0.394	BSC
L	0.73	1.03	0.029	0.041
e	0.80	BSC.	0.031	BSC.
b	0.30	0.45	0.012	0.018
c	0.11	0.23	0.004	0.009
Pin features				
N	44			
ND	11			
NE	11			
NOTE	SQUARE			

Conforms to JEDEC MO-112 AA-1 Iss. B

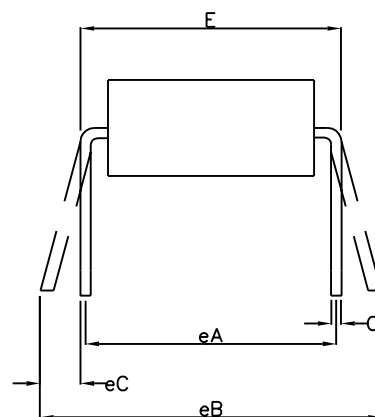
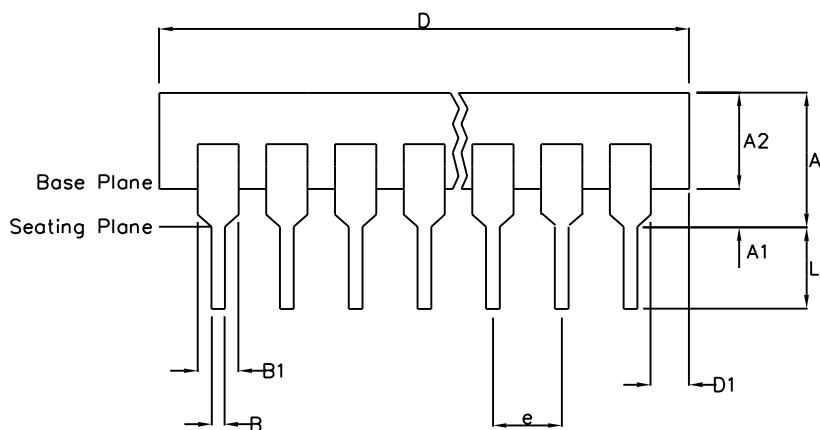
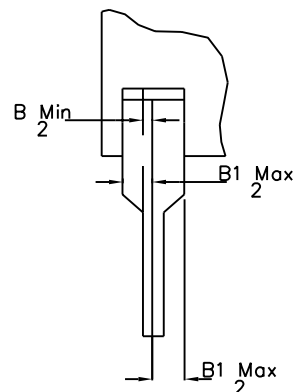
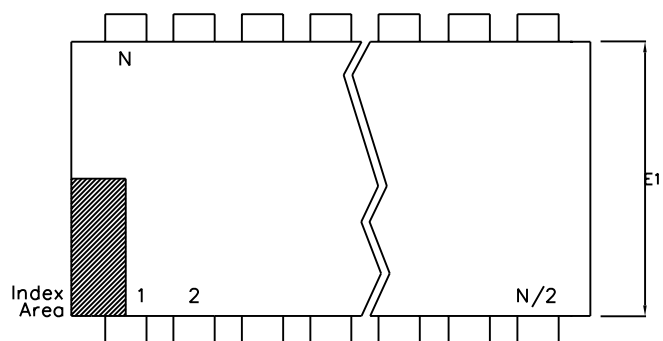
#### Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar prorusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

This drawing supersedes 418/ED/51210/011 issue 15 (Swindon)

© Zarlink Semiconductor 2002 All rights reserved.					Package Code <b>QB</b>	
ISSUE	3	4	5	6	Previous package codes <b>GP / L</b>	Package Outline for 44 lead MQFP (10 x 10 x 2.0mm) 3.9mm Footprint
ACN	203205	204755	207046	212835		
DATE	16Oct97	23Jun98	29Jun99	21May02		<b>GPD00234</b>
APPRD.						






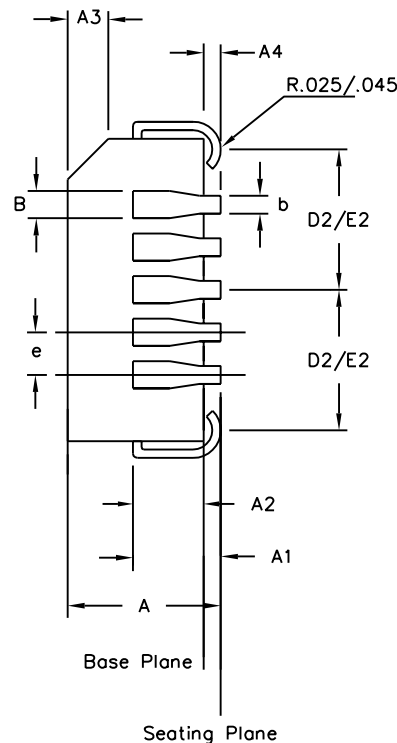
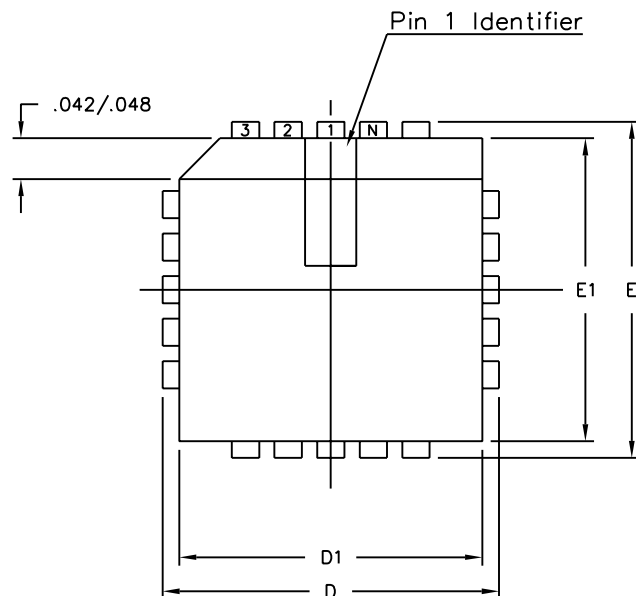
	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	50.29	53.21	1.980	2.095
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54	BSC	0.100	BSC
eA	15.24	BSC	0.600	BSC
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	40		40	
Conforms to Jedec MS-011AC ISS.B				

Notes:

1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

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ISSUE	1	2	3			Previous package codes	Package Outline for 40 lead PDIP
ACN	7010	203533	213103			DP / E	
DATE	20Apr95	25Nov97	15Jul02				
APPRD.							GPD000073





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	—	0.51	—
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050	BSC	1.27	BSC
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

#### Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

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ISSUE	1	2	3	
ACN	5958	207470	213094	
DATE	15Aug94	10Sep99	15Jul02	
APPRD.				



Previous package codes

HP / P

Package Code QA

Package Outline for  
44 lead PLCC

GPD000003



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