QUICKSWITCH® PRODUCTS HIGH-SPEED CMOS SYNCHROSWITCH™ 32:8 MUX/DEMUX WITH ACTIVE TERMINATORS

IDTQS34XST253

FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- Bidirectional signal flow
- Flow-through pinout
- Zero propagation delay, zero ground bounce
- 8 banks of 4:1 Mux/Demux
- Port select synchronous to the clock
- Clock enable and asynchronous enable
- "Bus-hold" terminators on the Demux side
- Undershoot clamp diodes on all switch and control pins
- Asynchronous SEL option
- Break-before-make feature
- Available in 80-pin MillipaQ (Q3)
- Bus-hold eliminates floating bus lines and reduces static power consumption

APPLICATIONS

- Video, audio, graphics switching, muxing

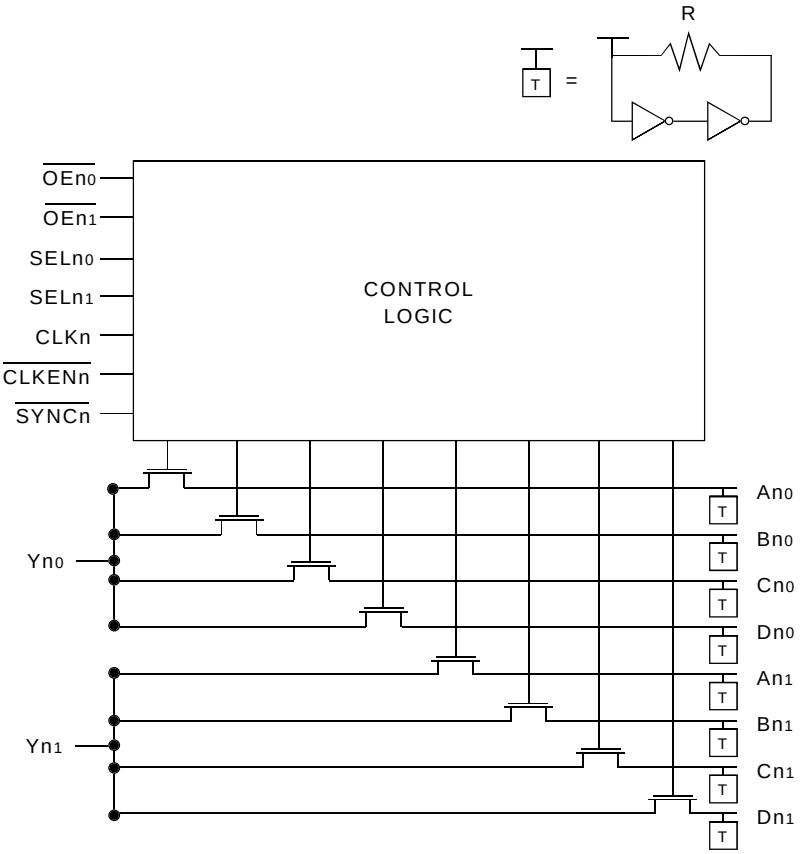
DESCRIPTION:

The QS34XST253 is a high-speed CMOS 32:8 multiplexer/demultiplexer with active terminators (bus-hold circuits) on the demux side. It is organized as four independent dual 4:1 mux/demux blocks. Port selection and connection, controlled by SEL signals, can be either asynchronous or synchronous. In the synchronous mode, the A, B, C, or D port to Y port connection is updated on the rising edge of the input clock CLK. Once the port-to-port connection is made, data flow can be bi-directional with a typical 250ps propagation delay through the switch. Clock Enable, overriding Asynchronous Enable, and Asynchronous Select controls provide additional design flexibility.

The bus-hold circuits latch the last data driven on the demux side, providing infinite hold time and glitch-free signal transitions. Synchronous controls and bus-hold ease timing constraints in many high speed data mux/demux applications, such as bank interleaving. The QS34XST253 is available in the space-saving, 80-pin dual-in-line MillipaQ package.

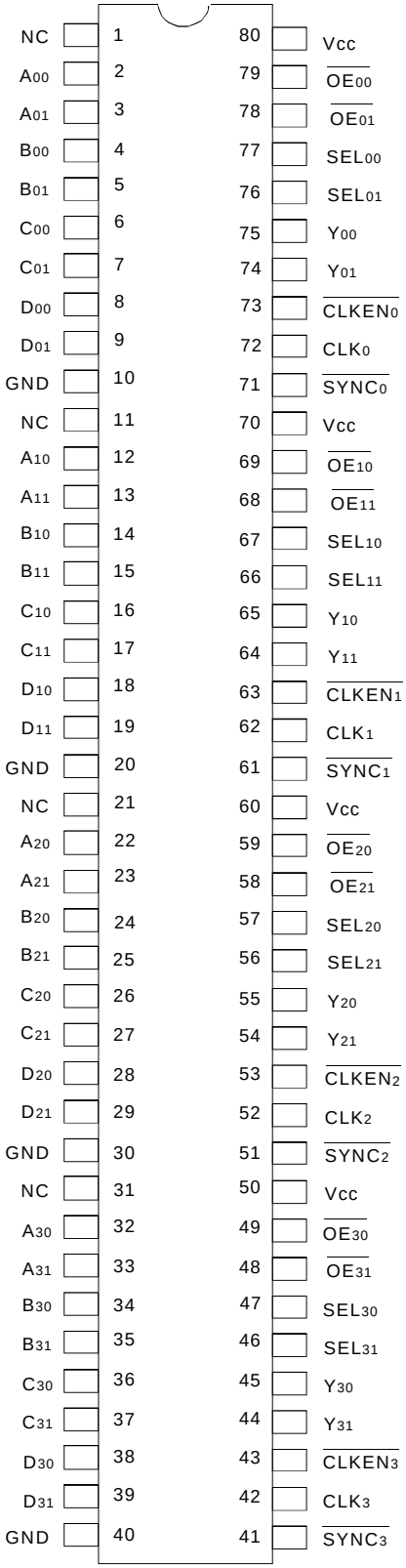
The QS34XST253 is characterized for operation at -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



NOTE: One of four blocks shown.

PIN CONFIGURATION



MILLIPAQ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Supply Voltage to Ground	– 0.5 to +7	V
V_{TERM}(3)	DC Switch Voltage V_S	– 0.5 to +7	V
V_{TERM}(3)	DC Input Voltage V_{IN}	– 0.5 to +7	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	-3	V
I_{OUT}	DC Output Current	120	mA
P_{MAX}	Maximum Power Dissipation (T_A = 85°C)	1.16	W
T_{STG}	Storage Temperature	– 65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc Terminals.
3. All terminals except Vcc.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, V_{IN} = 0V, V_{OUT} = 0V)

Pins		Typ.	Max. (1)	Unit
Control Inputs		4	5	pF
Quickswitch Channels	Demux	6	7	pF
(Switch OFF)	Mux	13	15	pF

NOTE:
1. This parameter is guaranteed at characterization but not production tested.

PIN DESCRIPTION

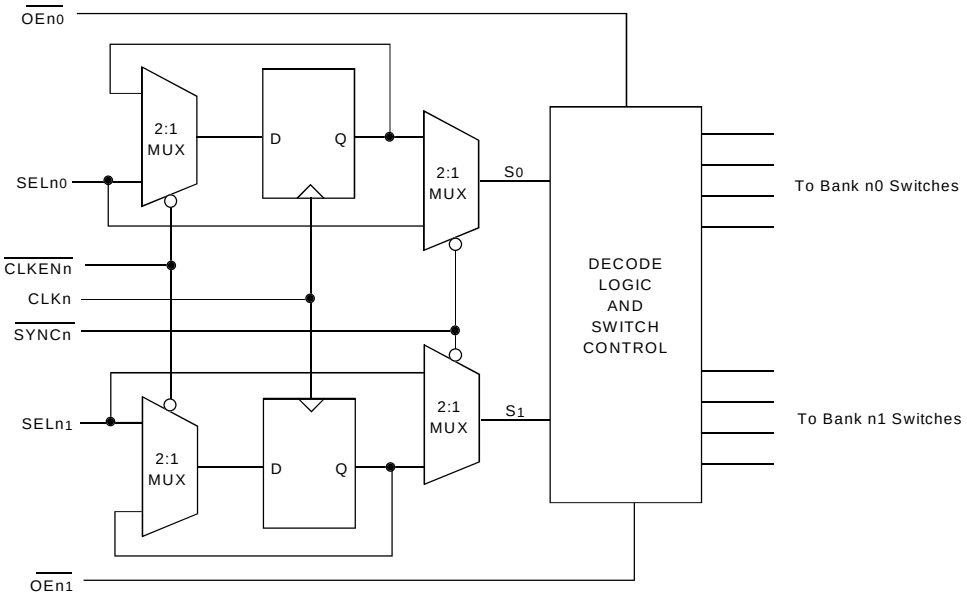
Pin Names	I/O	Description
An0 - Dn0	I/O	Demux Ports
An1 - Dn1	I/O	Demux Ports
Yn0, Yn1	I/O	Mux Ports
SELn0, SELn1	I	Select Inputs
CLKn	I	Clock
$\overline{\text{CLKENn}}$	I	Clock Enable
$\overline{\text{OEn0}}$, $\overline{\text{OEn1}}$	I	Output Enable
$\overline{\text{SYNCn}}$	I	Synchronous Selection Enable

FUNCTION TABLE(1)

Control Inputs							MUX Ports	
$\overline{SYNCn}$	$\overline{OEn_0}$	$\overline{OEn_1}$	CLKn	$\overline{CLKENn}$	$SELn_0$	$SELn_1$	Yn_0	Yn_1
L	L	L	↑	L	L	L	An_0	An_1
L	L	L	↑	L	H	L	Bn_0	Bn_1
L	L	L	↑	L	L	H	Cn_0	Cn_1
L	L	L	↑	L	H	H	Dn_0	Dn_1
L	H	H	↑	L	X	X	Hold Previous Data (2) (Switch OFF)	Hold Previous Data (2) (Switch OFF)
L	L	L	↑	H	X	X	Hold Previous Mux connection (3) (Switch ON)	Hold Previous Mux connection (3) (Switch ON)
L	H	H	↑	H	X	X	Hold Previous Data (4) (Switch OFF)	Hold Previous Data (4) (Switch OFF)
H	L	L	X	X	L	L	An_0	An_1
H	L	L	X	X	H	L	Bn_0	Bn_1
H	L	L	X	X	L	H	Cn_0	Cn_1
H	L	L	X	X	H	H	Dn_0	Dn_1
H	H	H	X	X	X	X	Hold Previous Data (Switch OFF)	Hold Previous Data (Switch OFF)

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = Low-to-High Transition
2. Mux switches are turned off and the terminators (last value latches) hold the previous data state. The port connections can be changed by the SEL input.
3. The contents of the "Mux select register" are unchanged and the previous Mux connection is unchanged. The output (Mux port) data state will depend on the present data state of the input (Demux port).
4. The contents of the "Mux select register" are unchanged and the last value latch holds the previous data state.

CONTROL LOGIC (1)



NOTE:
1. One of four blocks.

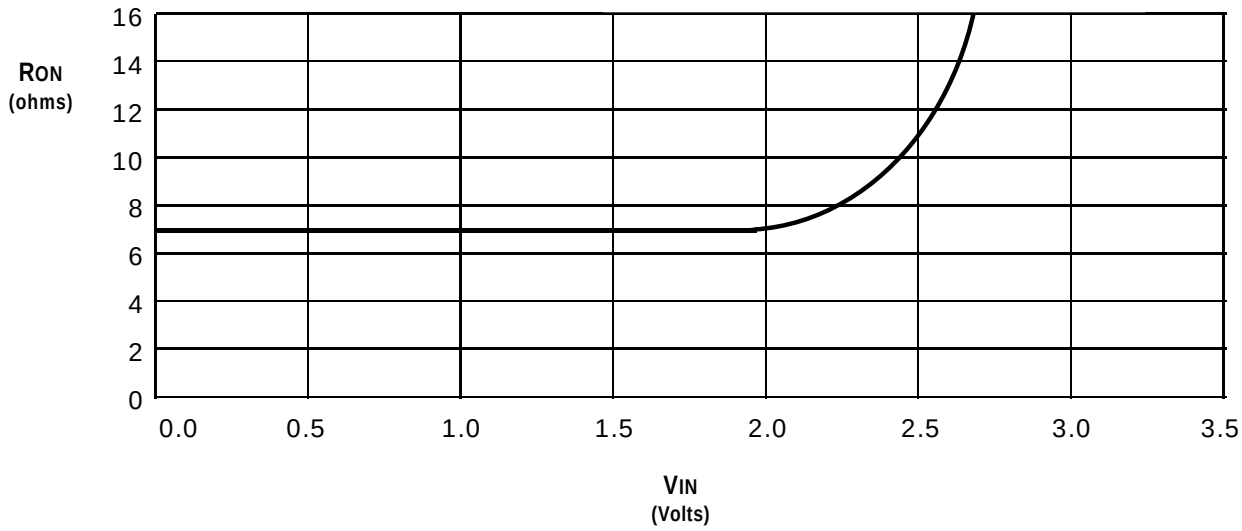
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins		2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Pins		—	—	0.8	V
I_{IN}	Input Leakage Current (Control Inputs)	0V ≤ V_{IN} ≤ Vcc		—	—	±1	µA
R_{ON}	Switch On Resistance (2)	Vcc = Min., V_{IN} = 0V, I_{ON} = 30mA		—	7	9	Ω
		Vcc = Min., V_{IN} = 2.4V, I_{ON} = 15mA		—	10	13	
I_{BHL}	Input Hold Current (3,4)	Vcc = 4.5V	V_{IN} = 0.8V	60	—	—	µA
I_{BHH}	(A, B, C, D)	Switch OFF	V_{IN} = 2V	– 60	—	—	
I_{BH}	Input Current (6)	Vcc = Max.	V_{IN} = 0V or Vcc	—	—	±20	µA
	(A, B, C, D)		0.8 < V_{IN} < 2V	—	—	±500(5)	

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Measured by voltage drop between A/B and Y pin at indicated current through the switch.
3. I_{BHL} is the minimum sustaining "sink" current at the input for V_{IN} = 0.8V. This parameter signifies the latching capability of the bus-hold circuit in logic LOW state.
4. I_{BHH} is the minimum sustaining "source" current at the input for V_{IN} = 2V. This parameter signifies the latching capability of the bus-hold circuit in logic HIGH state.
5. An external driver must provide at least I_{BH} during transition to guarantee that the bus-hold input will change states.
6. I_{BH} is the magnitude of the input current specified under two conditions:
   a) Input voltage at GND or Vcc. This indicates the input current under steady-state condition.
   b) Input voltage between 0.8V and 2V (TTL input threshold range). This indicates the maximum input current during transient condition. The driver connected to the input must overcome this current requirement in order to switch the logic state of the bus-hold circuit.

TYPICAL ON RESISTANCE vs V_{IN} AT Vcc = 5V



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or Vcc, f = 0	12	µA
ΔI_{CC}	Power Supply Current per Control Input HIGH [2]	V_{CC} = Max., V_{IN} = 3.4V, f = 0	1.5	mA
I_{CCD}	Dynamic Power Supply Current per MHz[3]	V_{CC} = Max., A/B/C/D and Y pins open Control Input Toggling at 50% Duty Cycle	0.25	mA/MHz

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven control input. (V_{IN} = 3.4V, Control Pins only.) A/B/C/D and Y pins do not contribute to ΔI_{CC}.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A/B/C/D and Y inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

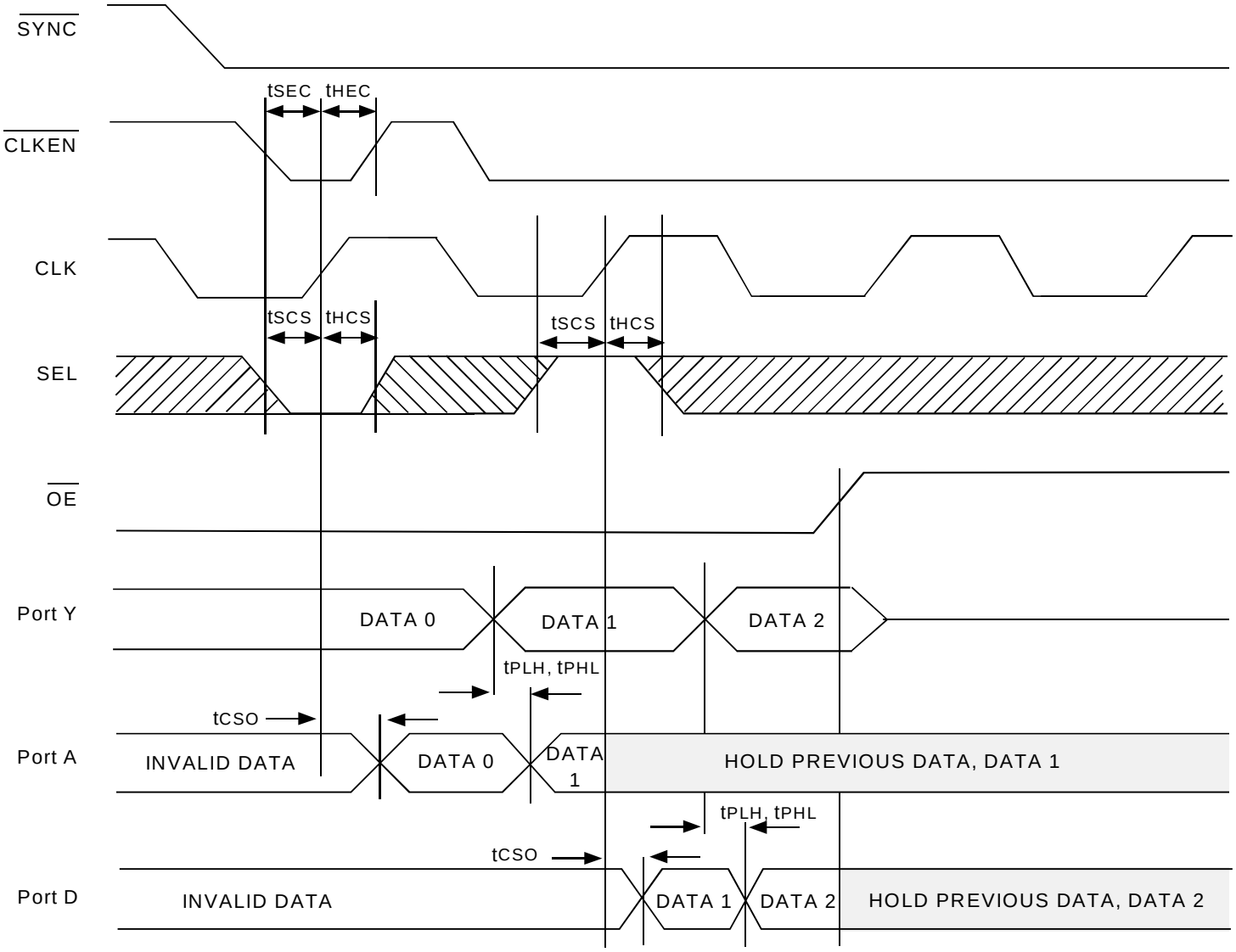
T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay [1,2] A/B/C/D to Y, Y to A/B/C/D	—	0.25	—	ns
t_{SEC}	Clock Enable to Clock Setup Time	3	—	—	ns
t_{HEC}	Clock Enable to Clock Hold Time	0	—	—	ns
t_{CSO}	Clock to Switch Turn-On Delay [3]	0.5	—	7	ns
t_{ASO}	Asynchronous Select to Switch Turn-On Delay [3]	0.5	—	7	ns
t_W	Clock Pulse Width (High)	3	—	—	ns
t_{SCS}	SEL to Clock Setup Time	3	—	—	ns
t_{HCS}	SEL to Clock Hold Time	0	—	—	ns
t_{PZL} t_{PZH}	Asynchronous Enable to Switch Turn-On Delay [3]	1.5	—	5.2	ns
t_{PLZ} t_{PHZ}	Asynchronous Enable to Switch Turn-Off Delay [1,3]	1.5	—	4.8	ns

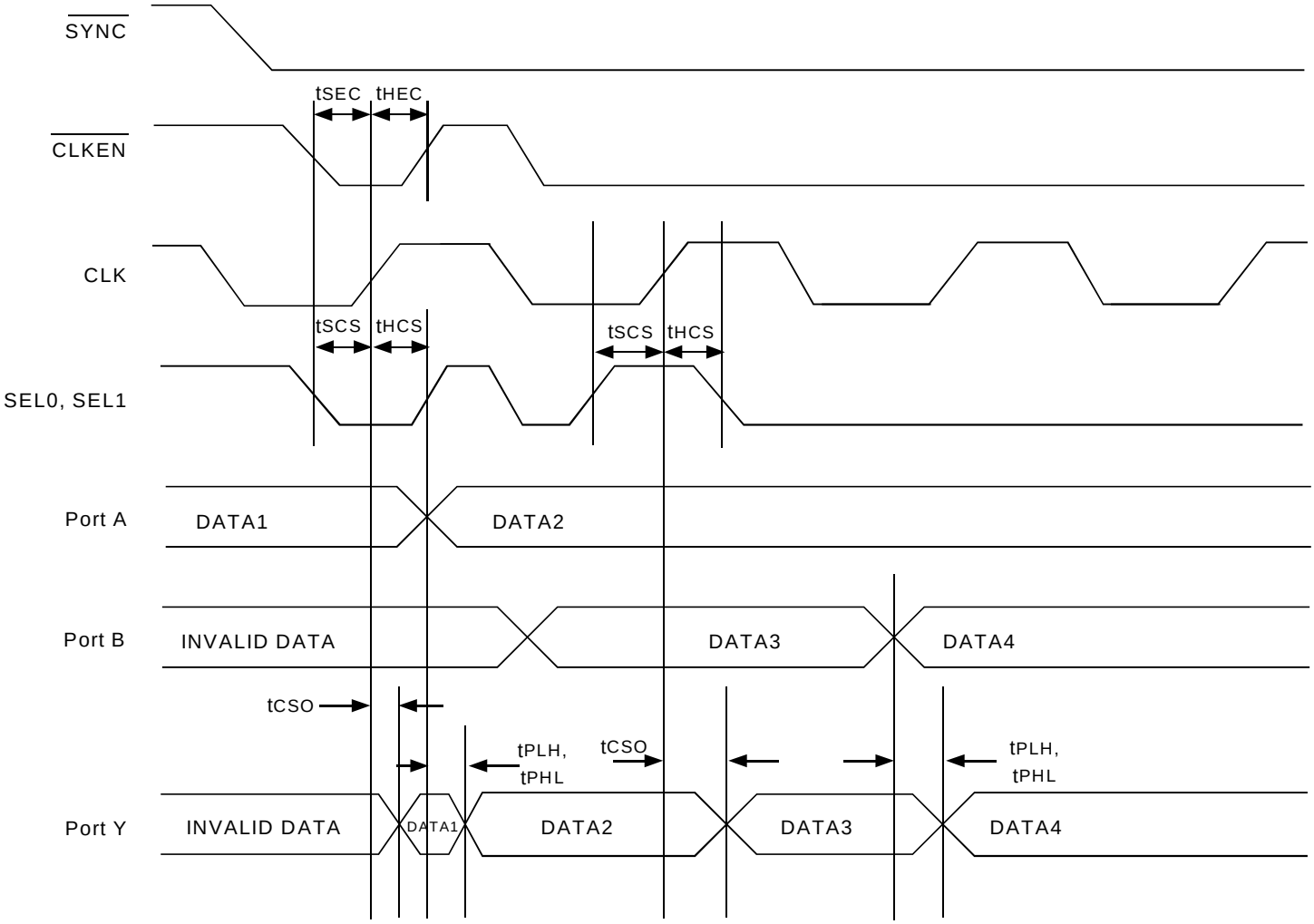
NOTES:
1. This parameter is guaranteed but not production tested.
2. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
3. Minimums guaranteed but not production tested.

TIMING WAVEFORMS - SYNCHRONOUS MODE, DEMUX FUNCTION



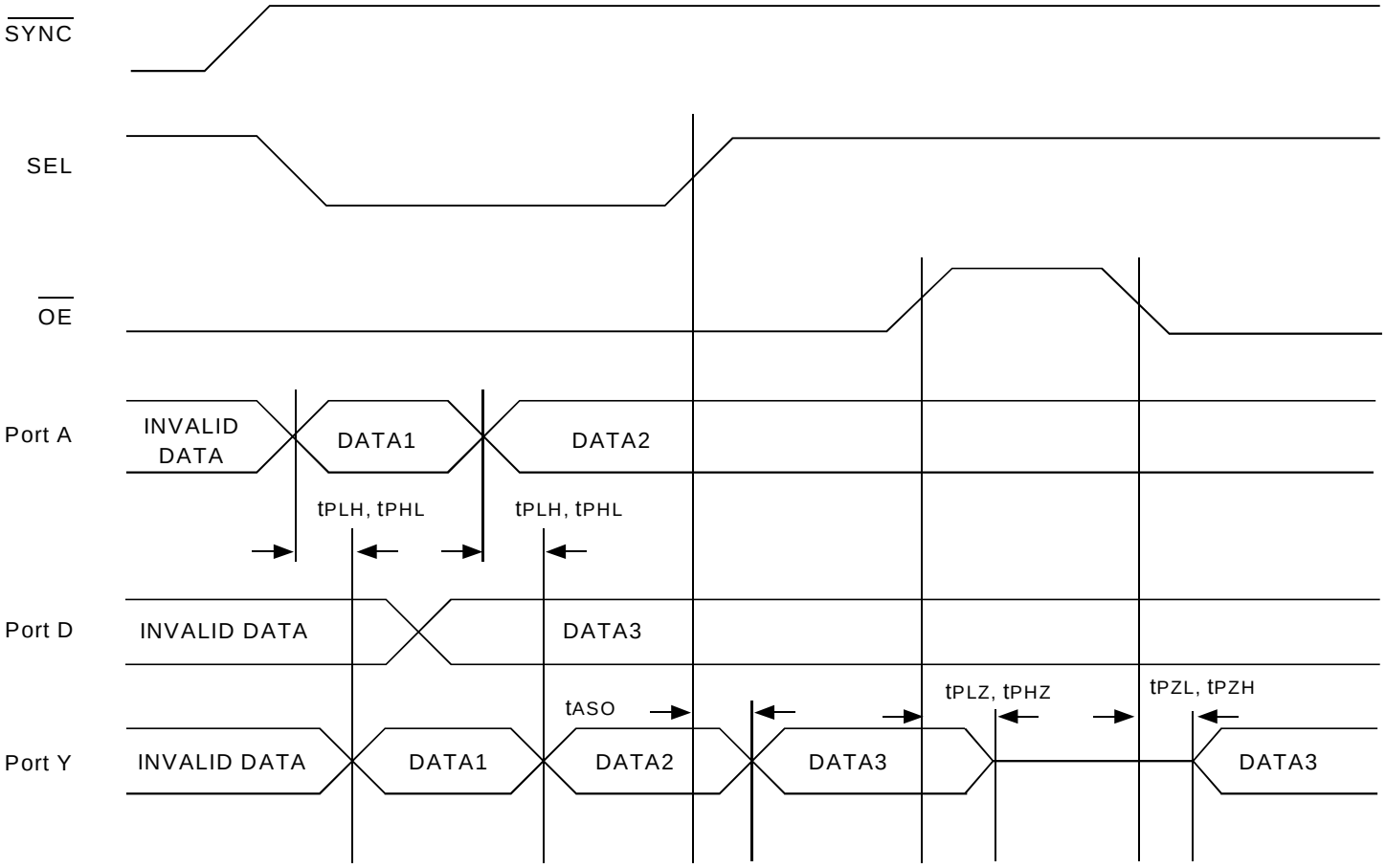
EXAMPLE: PORT Y TO PORT A/PORT D

TIMING WAVEFORMS - SYNCHRONOUS MODE, MUX FUNCTION



EXAMPLE: PORT A/PORT D TO PORT Y

TIMING WAVEFORMS - ASYNCHRONOUS MODE, MUX FUNCTION

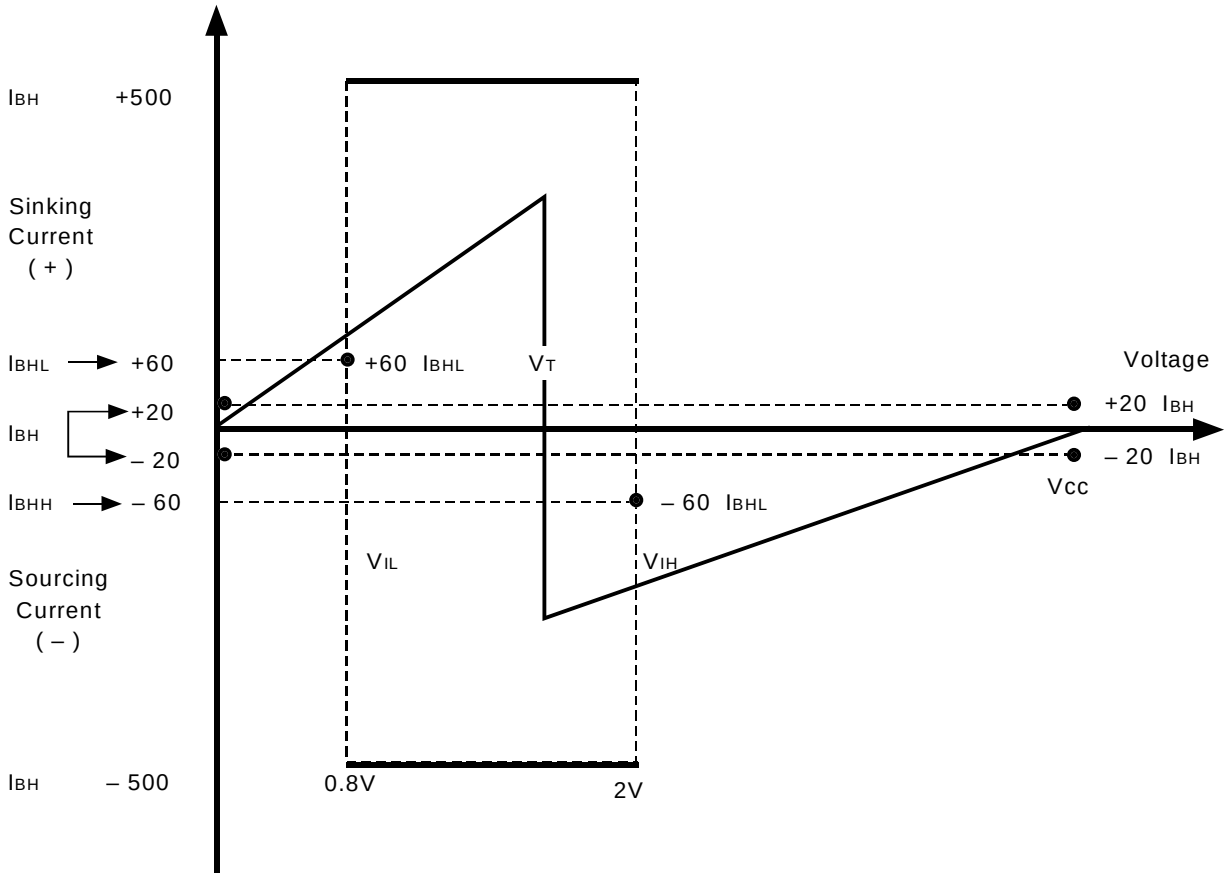


EXAMPLE: PORT A/PORT D TO PORT Y

ACTIVE TERMINATOR OR "BUS-HOLD" CIRCUIT

The Active Terminator circuit, also known as the bus-hold circuit, is configured as a "weak latch" with positive feedback. When connected to a TTL or CMOS input port, the bus-hold circuit holds the last logic state at the input when the input is "disconnected" from the driver. When the output of a device connected to such an input attempts a logic level transition, it will overdrive the bus-hold circuit. The primary benefit of a bus-hold circuit is that it prevents CMOS inputs from floating, a situation which should be avoided to prevent spurious switching of inputs and unnecessary power dissipation. Bus-hold is a better solution than the traditional approach of using resistive termination to Vcc or GND to prevent bus floating, because the bus-hold circuit does not consume any static power.

V-I CHARACTERISTICS OF BUS-HOLD CIRCUIT

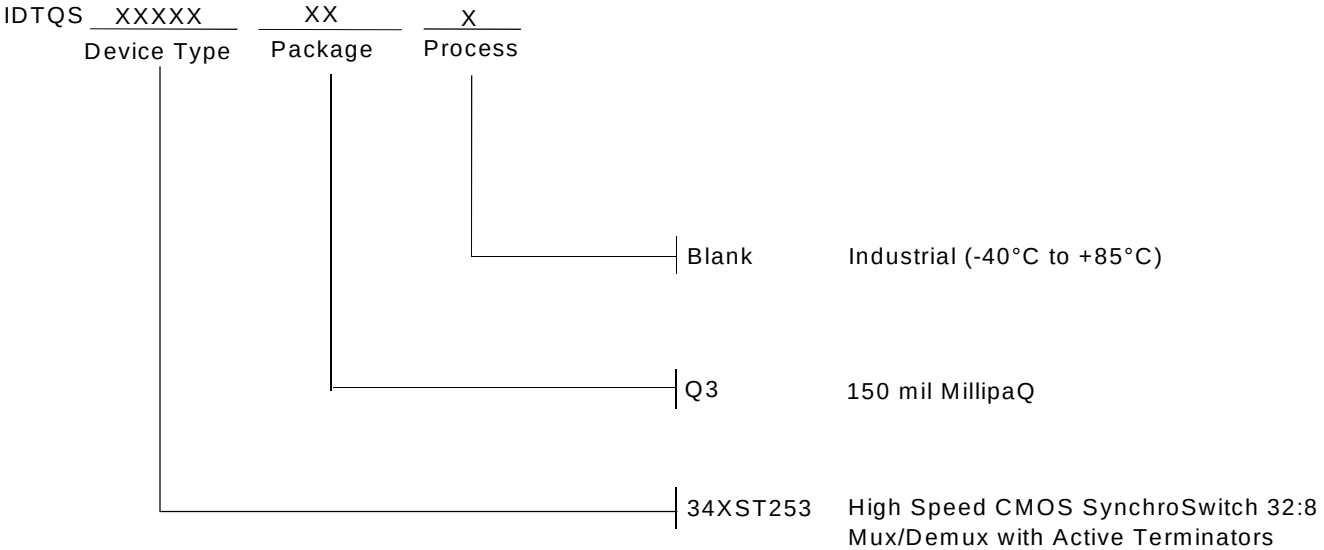


$V_T \equiv$ Threshold Voltage $\approx 1.5V$

$V_{IL} \approx .8$ $V_{IH} \approx 2V$

This figure shows the input V-I characteristics of a typical bus-hold implementation. The input characteristics resemble a resistor. As the input voltage is increased from 0 volts, the input "sink" current increases linearly. When the TTL threshold of the circuit is reached (typically 1.5 volts), the latch changes the logic state due to positive feedback and the direction of the current is reversed. As the input voltage is further increased towards Vcc, the input "source" current begins to decrease, reaching the lowest level at V_{IN} = Vcc.

ORDERING INFORMATION



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