Discontinued Product

OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM65522/65P522

8-Bit Microcontroller with A/D Converter

GENERAL DESCRIPTION

The MSM65522 is a high-performance 8-bit microcontroller that employs OKI original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65522 is capable of high-speed processing, and includes 8K bytes of program memory, 384 bytes of data memory (RAM), timers, serial ports and an A/D converter on chip. Also available is the MSM65P522, which replaces the on-chip program memory with one-time PROM.

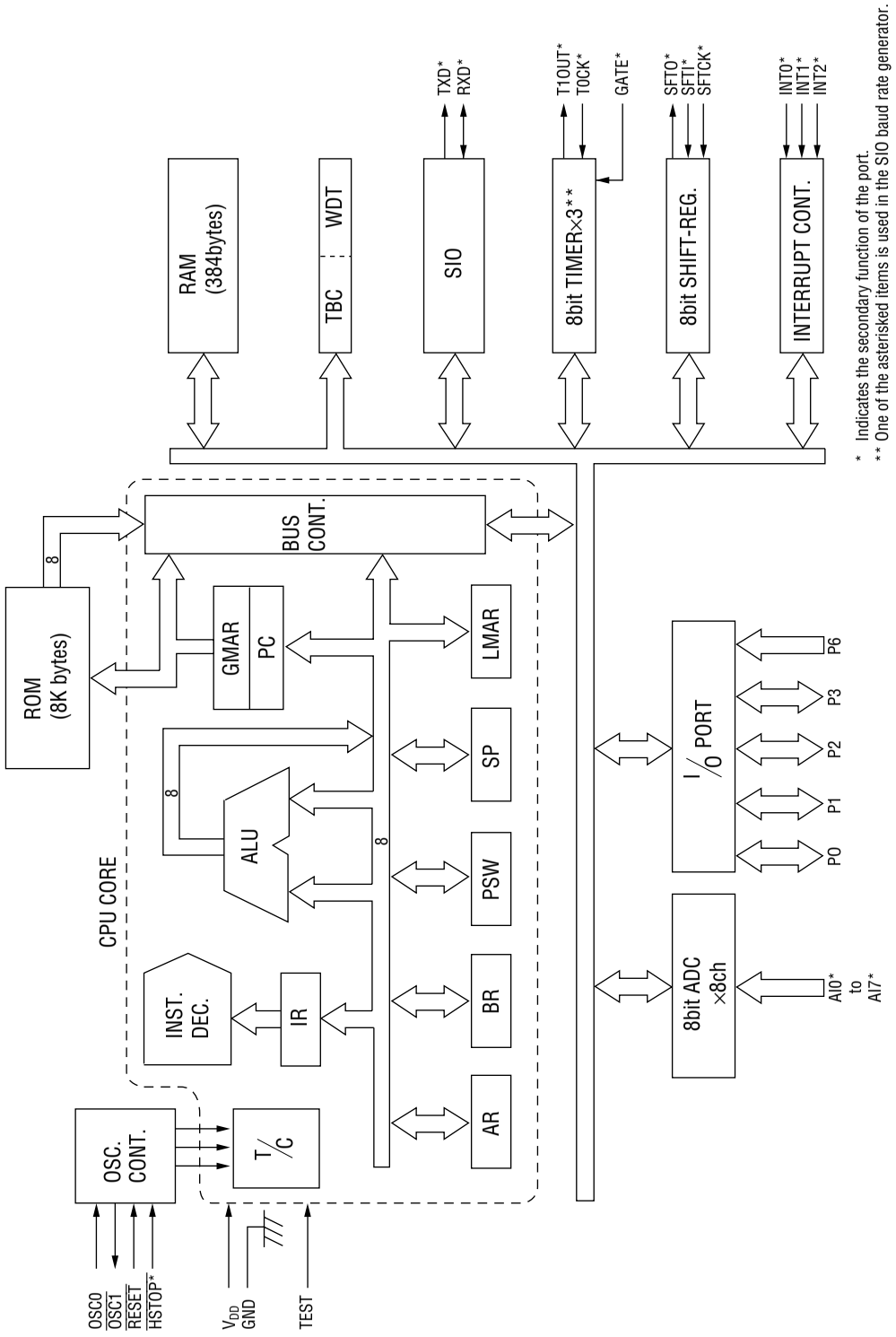
FEATURES

- Operating range
  - Operating frequency : 1 to 10MHz (V_{DD}=4.5 to 5.5V)
    1 to 5MHz (V_{DD}=2.7 to 5.5V)
  - Operating voltage : 2.7 to 5.5V
  - Operating temperature : – 40 to +85°C
- Memory space
  - Internal program memory : 8K bytes
  - Internal data memory : 384 bytes
- Minimum instruction execution time : 400ns @ 10 MHz
- Powerful instruction set : 81 basic instructions
  8/16-bit operation instructions
  Bit manipulation instructions
  Compound function instructions
- Abundant addressing modes
- I/O ports : 8-bit × 3
  4-bit × 1
  Input only port : 8-bit × 1
- Timers : 8-bit auto-reload timer × 3
  (One timer is shared by the baud rate generator. Combining the 8-bit timers, it is possible to use the timers as a 16-bit timer (1 channel).)
  Watchdog timer × 1
- Counters : Time base counter (14-bit) × 1
- Serial ports : Shift register × 1
  Serial port with baud rate generator (UART/Synchronous) × 1
- A/D converter : 8 bits × 8 channels
- External interrupts : 3
- Interrupt sources : 11
- Package Options
  - 42-pin plastic shrink DIP (SDIP42-P-600-1.78) : (Product name:MSM65522-×××SS, MSM65P522-×××SS)
  - 42-pin plastic DIP (DIP42-P-600-2.54) : (Product name:MSM65522-×××RS, MSM65P522-×××RS)
  - 44-pin plastic QFP (QFP44-P-910-0.80-2K) : (Product name:MSM65522-×××GS-2K, MSM65P522-×××GS-2K)
  - 44-pin plastic QFJ (QFJ44-P-S650-1.27) : (Product name:MSM65522-×××JS, MSM65P522-×××JS)

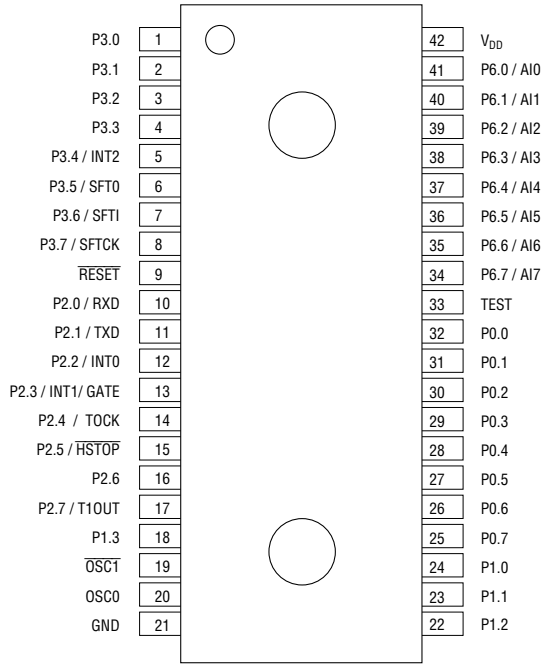
  ××× indicates the code number.

* Specifications are subject to change without notice.

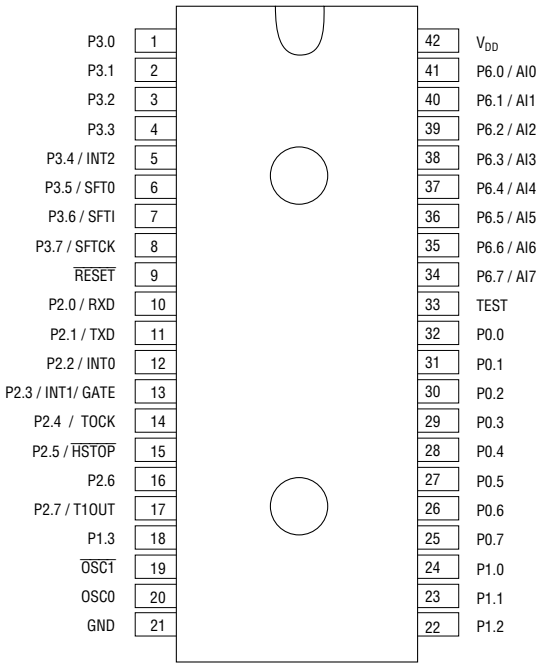
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

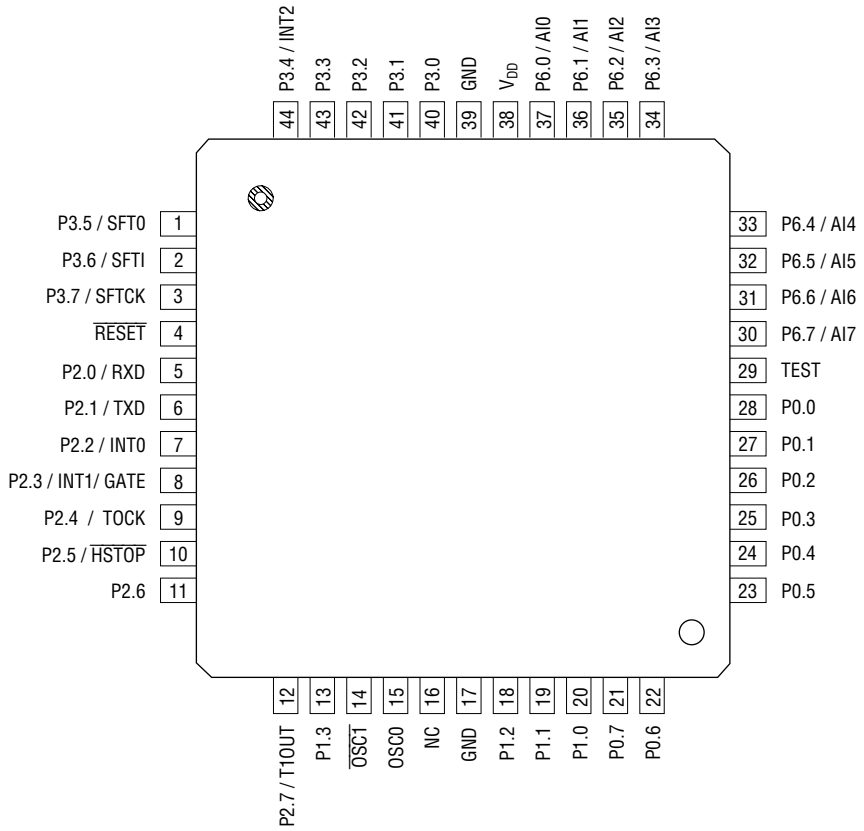


42-Pin Plastic Shrink DIP



42-Pin Plastic DIP

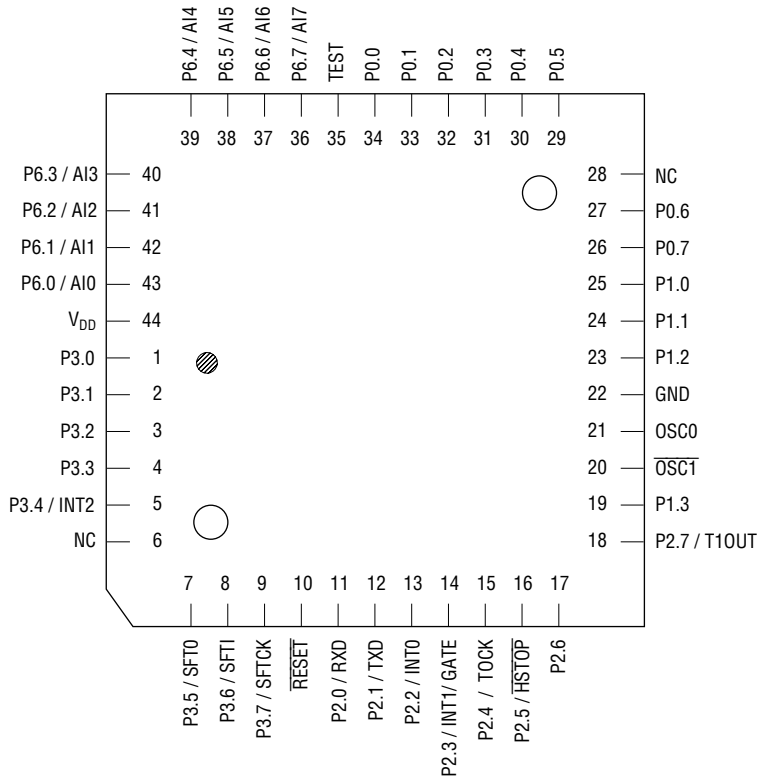
PIN CONFIGURATION (TOP VIEW) (Continued)



NC: No-connection pin

44-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (Continued)



NC: No-connection pin

44-Pin Plastic QFJ

PIN DESCRIPTION

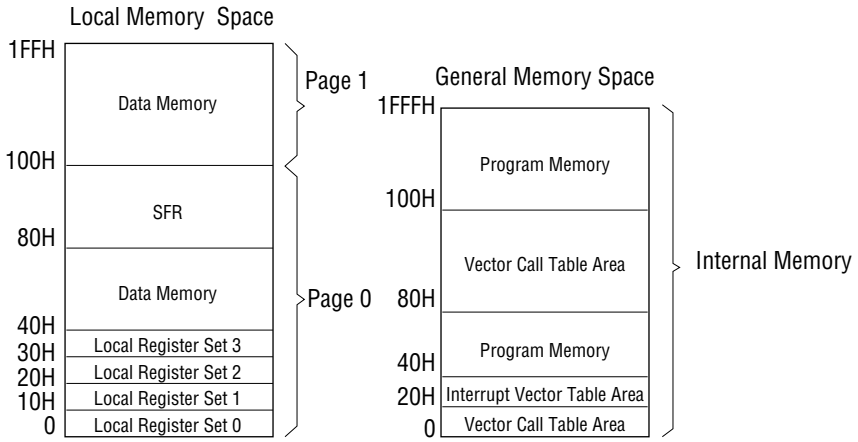
Basic Functions

Function	Symbol	Type	Description
Power Supply	V_{DD}	—	+5V digital power supply (common to analog power supply)
	GND	—	0V digital ground (common to analog ground)
Oscillation	OSC0	I	Oscillator input pin: connects to a crystal oscillator (or ceramic resonator) or external clock. The master clock and external clock are used as the system clock without frequency division.
	$\overline{OSC1}$	O	Oscillator input pin: connects to a crystal oscillator (or ceramic resonator). When an external clock is input to OSC0, leave $\overline{OSC1}$ open.
Control	$\overline{RESET}$	I	System reset input: when this pin goes low, the internal state of the chip is initialized and program execution restarts from address 0040H. The input is pulled up to V_{DD} with an internal pull-up resistor.
	TEST	I	Test input pin: connects to ground pin.
Port	P0.0 to P0.7	I/O	8-bit input/output port (Port 0)
	P1.0 to P1.3	I/O	8-bit input/output port (Port 1)
	P2.0 to P2.7	I/O	8-bit input/output port (Port 2): input or output can be selected for each bit by the port 2 direction register (P2DIR). In addition to their input/output port functions, the pins of port 2 have secondary functions: see the next table.
	P3.0 to P3.7	I/O	8-bit input/output port (Port 3): input or output can be selected for each bit by the port 3 direction register (P3DIR). In addition to their input/output port functions, the pins of port 3 have secondary functions: see the next table.
	P6.0/AI0 to P6.7/AI7	I	8-bit input port (Port 6): Functions as analog input channel during A/D conversion.

Secondary Functions

Function	Symbol	Type	Description
Serial Port	RXD	I/O	P2.0 secondary functions. UART: Input pin for a synchronous communication receive data. Synchronous: Input/output pin for serial port transmit/receive data.
	TXD	O	P2.1 secondary functions. UART: Input pin for a synchronous communication receive data. Synchronous: Output pin for serial port synchronizing clock.
External interrupt	INT0	I	Secondary function of P2.2 input pin for external interrupt 0. The interrupt can be triggered by the rising edge, falling edge, or both edges of rising or falling.
	INT1/Gate	I	Secondary function of P2.3 input pin for external interrupt 1. The interrupt can be triggered by the rising edge, falling edge, or both rising and falling edges. Also used as a gate signal input pin for gating the counter of timer 0.
	INT2	I	Secondary function of P3.4 input pin for external interrupt 2. The interrupt can be triggered by the rising edge, falling edge, or both rising and falling edges.
Control	$\overline{\text{HSTOP}}$	I	Secondary function of P2.0 input pin for hardware stop mode. If this pin goes low while the HSTP bit in SBYCON is set to 1, the chip enters hard stop mode. In hardware stop mode the clock stops and the CPU and on-chip peripheral functions shut down to conserve power.
Shift Registers	SFTO	O	P3.5 secondary functions. Shift register data output pin.
	SFTI	I	P3.6 secondary functions. Shift register data output pin.
	SFTCK	I/O	P3.7 secondary functions. Shift register synchronizing clock input/output pin. In master mode: clock output In slave mode: clock input
Timer 0	T0CK	I	Secondary function of P2.4: external clock input pin for timer 0.
Timer 1	T1OUT	O	Secondary function of P2.7: outputs a waveform with twice the cycle of the overflow interval of timer 1.
A/D Converter	AI0 to AI7	O	Secondary function of P6.0 to P6.7: functions as analog input channel in A/D conversion.

MEMORY MAPS


Local Memory Space
1FFH
Data Memory
100H
SFR
80H
Data Memory
40H
30H
20H
10H
0
Local Register Set 3
Local Register Set 2
Local Register Set 1
Local Register Set 0
Page 1
Page 0
General Memory Space
1FFFH
Program Memory
100H
Vector Call Table Area
80H
Program Memory
40H
20H
Interrupt Vector Table Area
0
Vector Call Table Area
Internal Memory

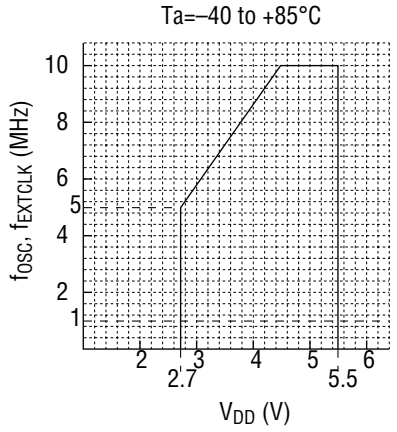
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	
Output Voltage	V_O		–0.3 to V_{DD}+0.3	
Analog Input Voltage	V_{AI}		–0.3 to V_{DD}+0.3	
Power Dissipation	P_D	Ta=25°C per package	400	mW
		Ta=25°C per one output	50	
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	$f_{OSC} \leq 10$ MHz	4.5 to 5.5	V
		$f_{OSC} \leq 5$ MHz	2.7 to 5.5	
Analog Input Voltage	V_{AI}	—	0 to V_{DD}	
Memory Hold Voltage	V_{DDMH}	f_{OSC}=0 Hz	2.0 to 5.5	
Operating Frequency *1	f_{OSC}	V_{DD}=4.5 to 5.5	1 to 10	MHz
		V_{DD}=2.7 to 4.5	1 to 5	
External Clock Operating Frequency	f_{EXTCLK}	V_{DD}=4.5 to 5.5	0 to 10	MHz
		V_{DD}=2.7 to 4.5	0 to 5	
Operating Temperature	T_{OP}	—	–40 to +85	°C

*1 This is due to the standard of a crystal oscillator or resonator.



* Operating Frequency is more than 1MHz.

Figure 1. Supply Voltage vs. Operating frequency

ELECTRICAL CHARACTERISTICS

DC Characteristics 1 (V_{DD}=4.5 to 5.5V, 5V Version)

(GND=0V, Ta=–40 to +85°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Schmitt Trigger Circuit Input Voltage	*1	V_{T-}	—	$0.3V_{DD}$	—	—	V
		V_{T+}		—	—	$0.7V_{DD}$	
		$\triangle V_T$		—	1.0	—	
"H" Input Voltage 1	*2	V_{IH1}	—	$0.3V_{DD}$+0.7	—	V_{DD}+0.3	
"H" Input Voltage 2	*3	V_{IH2}	—	$0.7V_{DD}$	—	V_{DD}+0.3	
"L" Input Voltage	*4	V_{IL}	—	–0.3	—	$0.3V_{DD}$-0.3	
"H" Output Voltage 2		V_{OH}	I_{OH}=–400µA	V_{DD}–0.4V	—	—	
"L" Output Voltage 1		V_{OL}	I_{OL}=1.6mA	—	—	0.4	
Input Leakage Current 1	*5	I_{LI1}	V_I=V_{DD}/0V	—	—	±1	µA
Input Leakage Current 2	*6	I_{LI2}	V_I=V_{DD}/0V	—	—	±10	
Pull-up Resistor	*7	R_{RST}	V_I=0V	30	50	80	KΩ
Input Capacitance		C_I	f=1MHz, Ta=25°C	—	5	—	pF
Current Consumption	*8	I_{DDS}	5V, Stop mode	—	2	50	µA
Current Consumption		I_{DD}	f_{OSC}=10MHz, 5V, no load	—	25	35	mA

*1 P0 to P3 (Includes secondary function inputs)
*2 P6
*3 OSC0 and $\overline{\text{RESET}}$
*4 P6, OSC0, $\overline{\text{RESET}}$
*5 P6
*6 Excludes P6. $\overline{\text{RESET}}$ sets to V_{DD} and TEST sets to 0V
*7 $\overline{\text{RESET}}$
*8 The ports set for input mode are V_{DD} or 0V, the ports except these are no load and A/D converter is not active.

DC Characteristics 2 (2.7 to 4.5V, 3V Version)

(GND=0V, Ta=–40 to +85°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Schmitt Trigger Circuit Input Voltage	*1	V_{T-}	—	$0.3V_{DD}$	—	—	V
		V_{T+}		—	—	$0.7V_{DD}$	
		$\triangle V_T$		—	0.5	—	
"H" Input Voltage	*2	V_{IH1}	—	$0.3V_{DD}+0.7$	—	$V_{DD}+0.3$	
"H" Input Voltage	*3	V_{IH2}	—	$0.7V_{DD}+0.3$	—	$V_{DD}+0.3$	
"L" Input Voltage	*4	V_{IL}	—	–0.3	—	$0.3V_{DD}–0.3$	
"H" Output Voltage		V_{OH}	I_{OH}=–20µA	$V_{DD}–0.1$	—	—	
"L" Output Voltage		V_{OL}	I_{OL}=20µA	—	—	0.1	
Input Leakage Current 1	*5	I_{LI1}	$V_I=V_{DD}/0V$	—	—	±1	µA
Input Leakage Current 1	*6	I_{LI1}	$V_I=V_{DD}/0V$	—	—	±1	
Pull-up Resistor	*7	R_{RST}	V_I=0V	30	50	80	KΩ
Input Capacitance		C_I	f=1MHz, Ta=25°C	—	5	—	pF
Current Consumption	*8	I_{DDS}	3V, stop mode	1	—	25	µA
Current Consumption		I_{DD}	5MHz, 3V, no load	10	6	15	mA

*1 P0 to P3 (Includes secondary function inputs)
*2 P6
*3 OSC0 and $\overline{\text{RESET}}$
*4 P6, OSC0, $\overline{\text{RESET}}$
*5 P6
*6 Excludes P6. $\overline{\text{RESET}}$ sets to V_{DD} and TEST sets to 0V.
*7 $\overline{\text{RESET}}$
*8 The ports except these are no load, and A/D converter active.

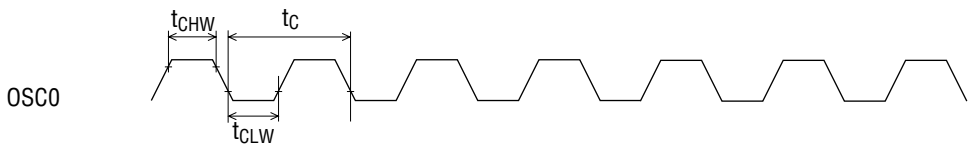
AC Characteristics

CPU control (OSC0 Clock)

(V_{DD}=2.7 to 5.5 V, GND=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Period	t_C	V_{DD}=4.5 to 5.5 V	100	—	ns
"L" Clock Pulse Width	t_{CLW}		45	—	
"H" Clock Pulse Width	t_{CHW}		45	—	
Clock Period	t_C	V_{DD}=2.7 to 4.5 V	200	—	
"L" Clock Pulse Width	t_{CLW}		90	—	
"H" Clock Pulse Width	t_{CHW}		90	—	

CPU control (OSC0 Clock)



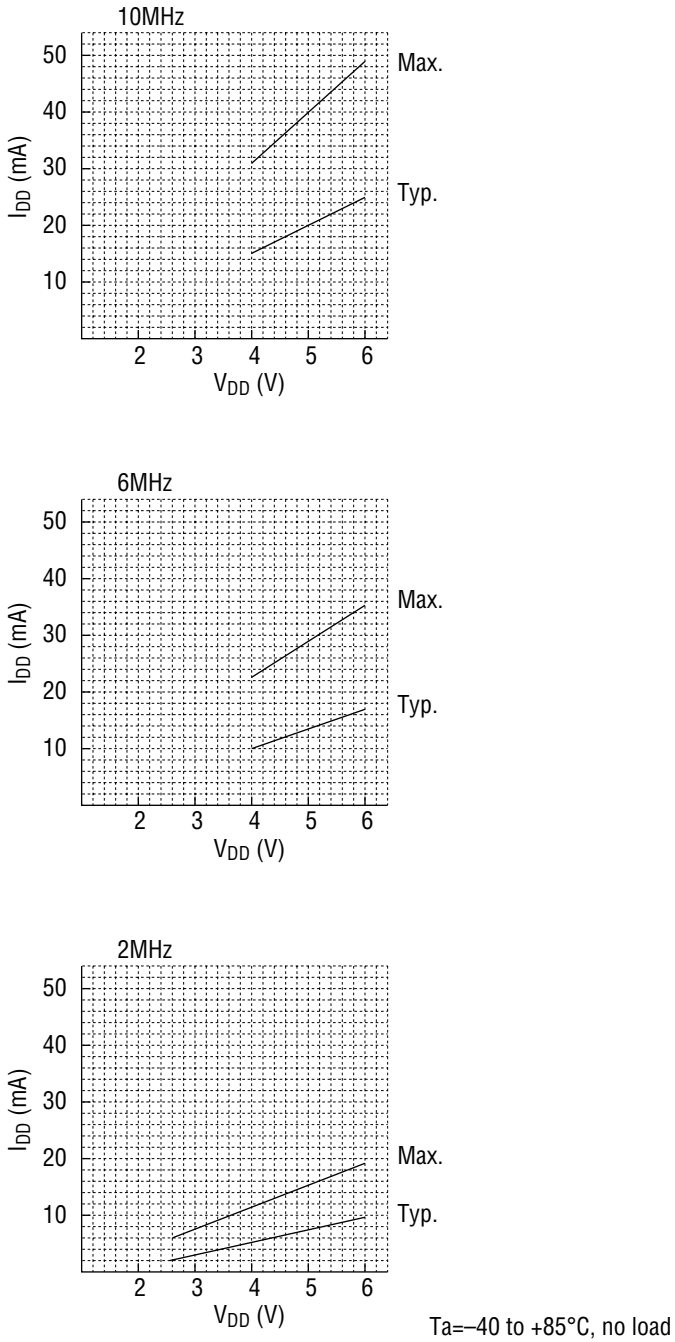


Figure 2. Voltage vs. Current

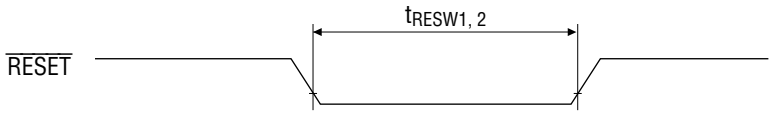
- **CPU control**

(V_{DD}=2.7 to 5.5V, GND=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ Pulse Width *1	t_{RESW1}	—	20	—	ns
$\overline{\text{RESET}}$ Pulse Width *2	t_{RESW2}	—	*3	—	—

*1 Excluding power ON, stop mode and hard stop mode.
*2 In power ON, stop mode and hard stop mode.
*3 Oscillation stabilization time depends on resonator.

$\overline{\text{RESET}}$ Pulse Width



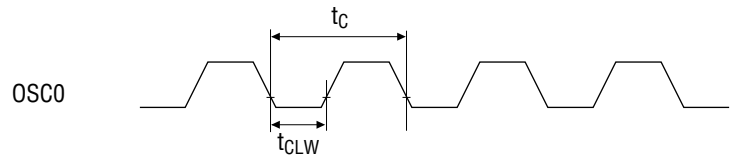
- **Peripheral control 1**

(V_{DD}=2.7 to 5.5V, GND=0V, Ta=–40 to +85°C)

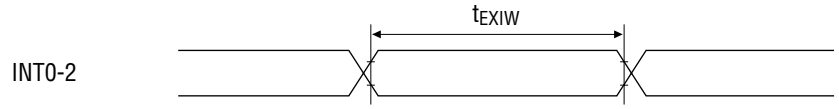
Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Period	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
			V_{DD}=2.7 to 4.5V	200	—	
EXI	External Interrupt Pulse Width	t_{EXIW}	—	4 t_C	—	
T0	External Clock Pulse Width	t_{T0CW}		4 t_C	—	
	GATE Pulse Width	t_{T0GW}		1 t_{T0CLK} *1	—	

*1 t_{T0CLK} : Timer 0 count clock period selected by T0CON.

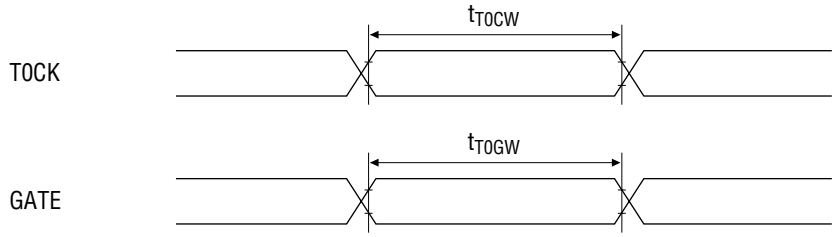
1) OSC0



2) EXI Pulse Width



3) T0

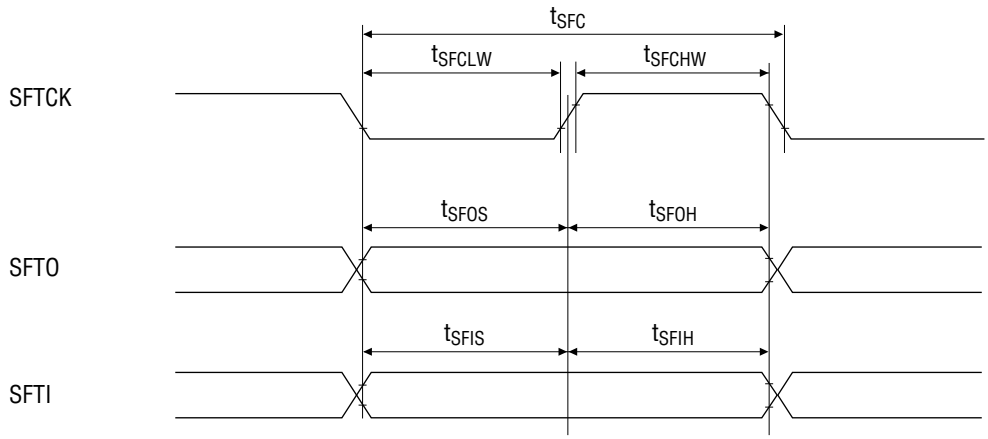


- **Peripheral control 2**

(V_{DD}=AV_{DD}=2.7 to 5.5V, GND=0V, Ta=–40 to +85°C)

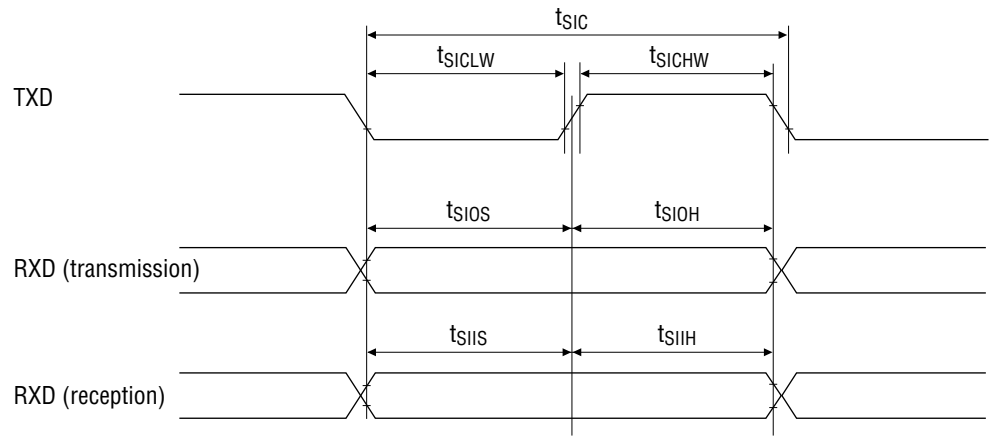
Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Period	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
			V_{DD}=2.7 to 4.5V	200	—	
SFT	SFTCK Period	t_{SFC}	C_L=100pF	8 t_C	—	
	SFTCK "L" Pulse Width	t_{SFCLW}		4 t_C–20	—	
	SFTCK "H" Pulse Width	t_{SFCHW}		4 t_C–20	—	
	SFTO Setup Time	t_{SFOS}		t_{SFCLW}–100	—	
	SFTO Hold Time	t_{SFOH}		t_{SFCHW}–100	—	
	SFTI Setup Time	t_{SFIS}		100	—	
	SFTI Hold Time	t_{SFIH}		100	—	
SIO (Clock Synchro-nous Mode)	Synchronous Clock Period	t_{SIC}		8 t_C	—	
	Synchronous Clock "L" Pulse Width	t_{SICLW}		4 t_C–20	—	
	Synchronous Clock "H" Pulse Width	t_{SICHW}		4 t_C–20	—	
	Output Data Setup Time	t_{SIOS}		6 t_C–100	—	
	Output Data Hold Time	t_{SIOH}		2 t_C–100	—	
	Input Data Setup Time	t_{SIIS}		t_C+t_{CLW}+100	—	
	Input Data Hold Time	t_{SIIH}		0	—	

1) SFT



2) SIO

(Clock Synchronous Mode)



A/D Converter Characteristics

(V_{DD}=4.5 to 5.5V/2.7 to 4.5V, GND=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	See the recommended circuit (Fig. 3). Analog input source impedance $R_I \leq 5k\Omega$	—	8	—	bit
Absolute Error	E_L		—	—	+1.5/+2 –1.5/–2	LSB
Differential Linearity Error	E_D		—	—	±0.5/±1	LSB
Zero Point Error	E_{ZS}		—	—	+1.5/+2	LSB
Full Scale Error	E_{FS}		—	—	–1.5/–2	LSB
Crosstalk	E_{CT}	See the measuring circuit (Fig. 4).	—	—	±0.5/±1	LSB
Conversion time *	t_{CONV}	f_{OSC}=10 MHz / 5 MHz	—	16/32	—	µs/CH

* 14.8/2.96µs/CH for the one time conversion follows setting the GO bit.

Definitions of Terms

(1) Resolution
The minimum distinguishable analog value. For 8 bits, 2^8=256, i.e. (V_{RH}–V_{RL}) ÷ 256.

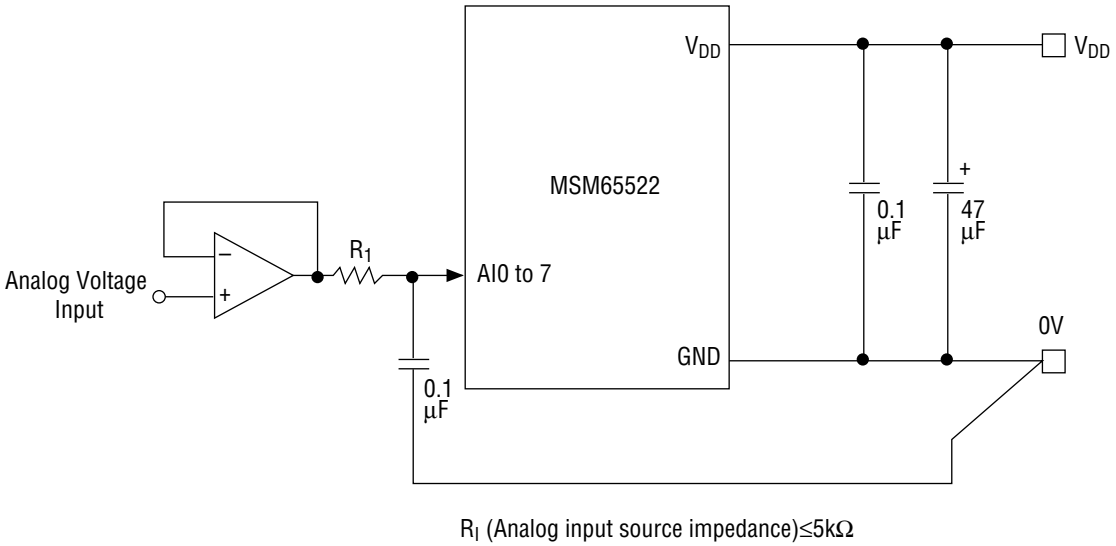
(2) Linearity Error
The variance between the ideal conversion characteristics as an 8-bit A/D converter and actual conversion characteristics (does not include quantatized error).

The ideal conversion characteristics refer to steps of the voltage between V_{RH} and V_{RL} into 256 intervals.

(3) Differential Linearity Error
Indicates the smoothness of the conversion. The width of analog input voltage corresponding to the change by one bit of digital output is 1 LSB = (V_{RH}-V_{RL}) ÷ 256 ideally. The variance between this ideal bit size and bit size at arbitrary point in the conversion range.

(4) Zero Scale Error
The variance between the ideal conversion characteristics at the switching point of digital outputs "000H to 001H" and actual conversion characteristics.

(5) Full Scale Error
The variance between the ideal conversion characteristics at the switching point of digital outputs "0FEH to 0FFH" and actual conversion characteristics.



R_I (Analog input source impedance)≤5kΩ

Figure 3. Recommended Circuit

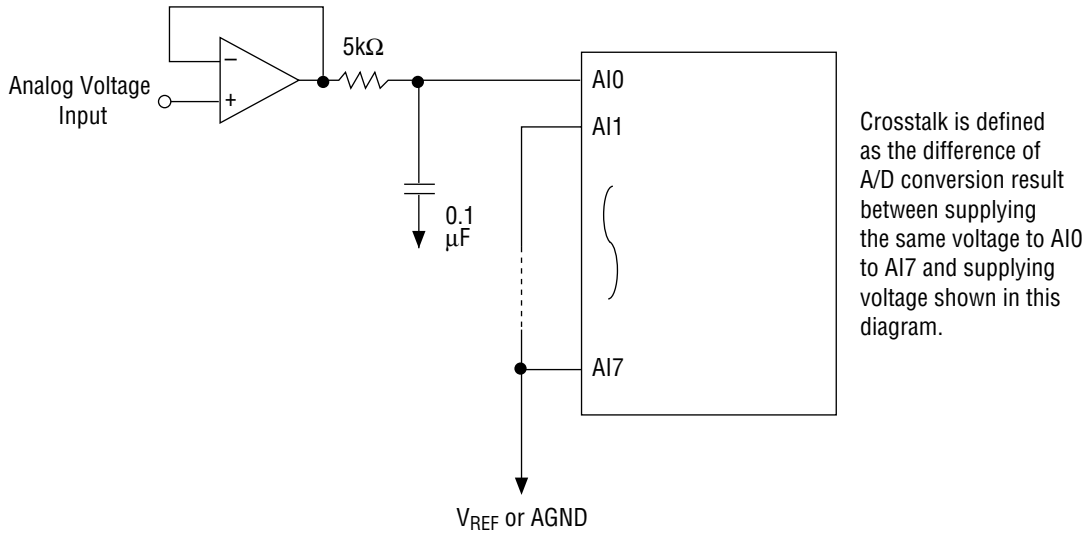
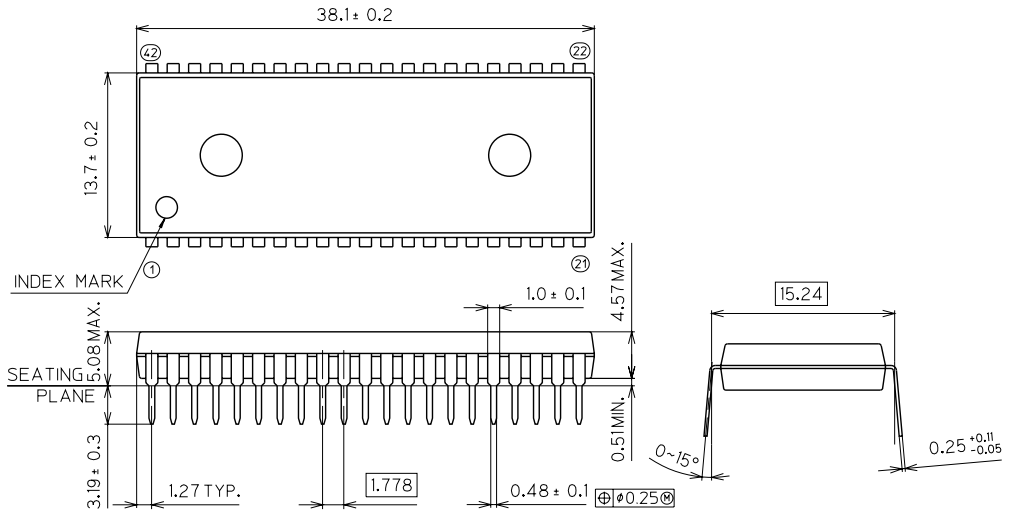


Figure 4. Crosstalk Measuring Circuit

PACKAGE DIMENSIONS

(Unit : mm)

SDIP42-P-600-1.78



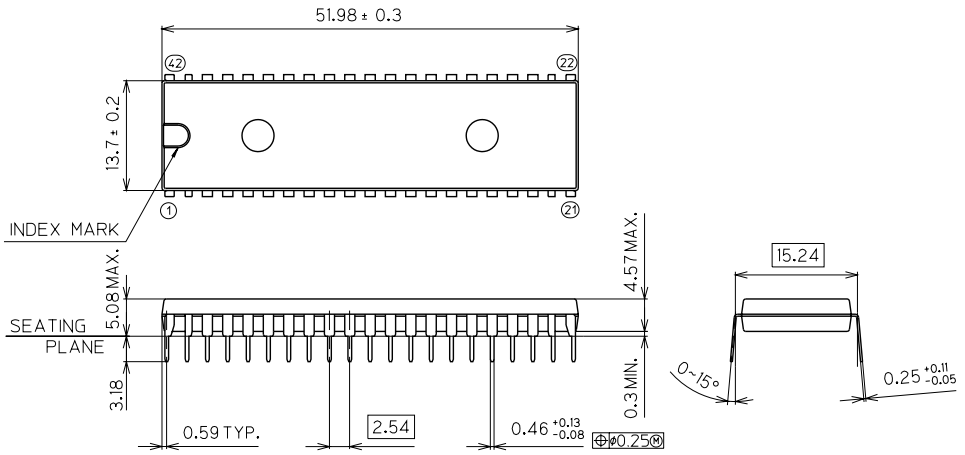
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	4.52 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

DIP42-P-600-2.54



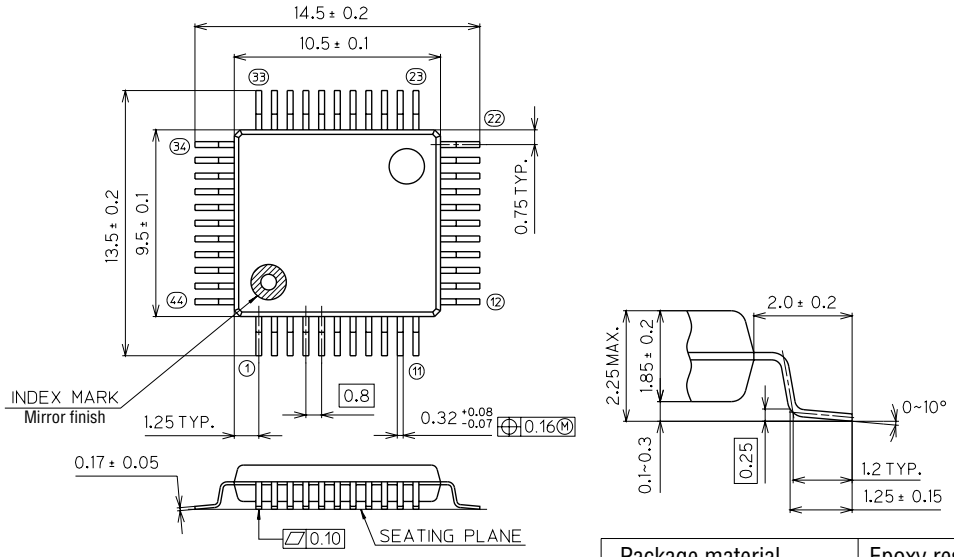
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.20 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K



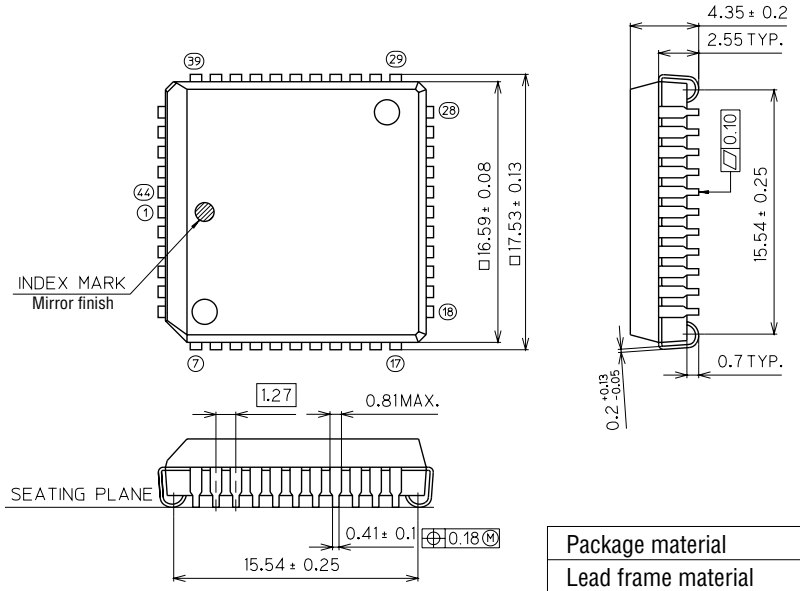
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFJ44-P-S650-1.27



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	2.00 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).