



### N-Channel Reduced $Q_g$ , Fast Switching WFET

#### CHARACTERISTICS

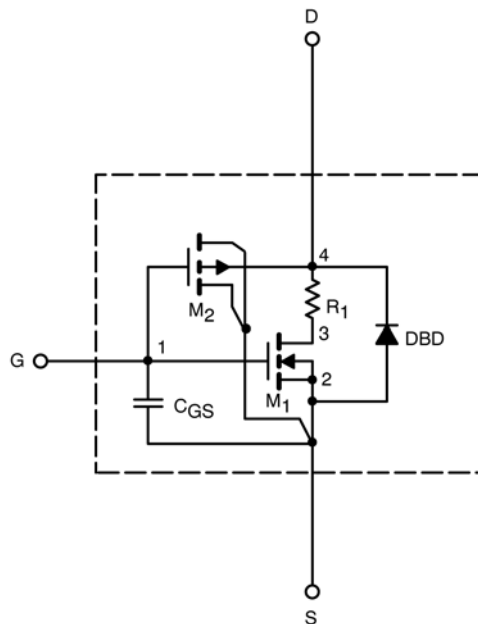
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the  $-55$  to  $125^\circ\text{C}$  Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the  $-55$  to  $125^\circ\text{C}$  temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
<b>Static</b>					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.9		V
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	686		A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 12.5\text{A}$	0.006	0.006	$\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 10\text{A}$	0.009	0.009	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 12.5\text{A}$	45	46	S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.7\text{A}$	0.73	0.73	V
<b>Dynamic<sup>b</sup></b>					
Input Capacitance	$C_{iss}$	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	1626	1465	pF
Output Capacitance	$C_{oss}$		360	360	
Reverse Transfer Capacitance	$C_{rss}$		136	150	
Total Gate Charge	$Q_g$	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 12.5\text{A}$	22	25	nC
			11	12	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 12.5\text{A}$	3.7	3.7	
Gate-Drain Charge	$Q_{gd}$		3.1	3.1	

Notes

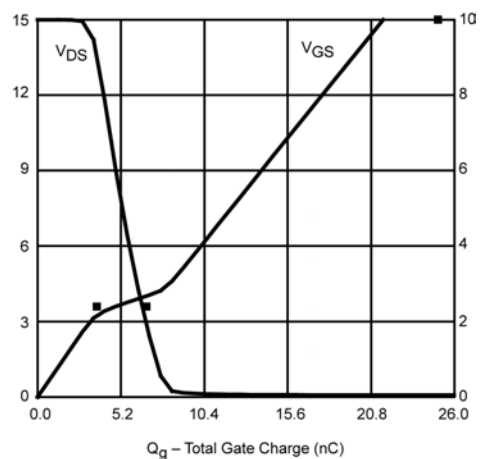
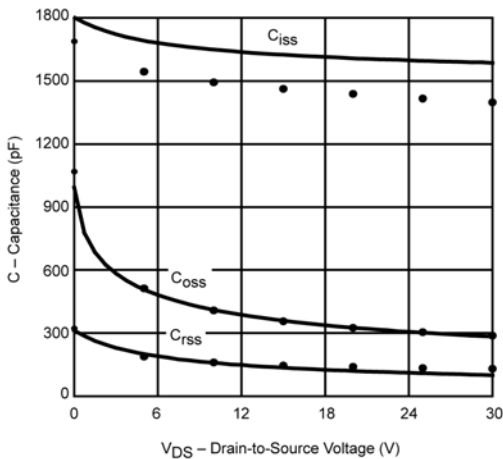
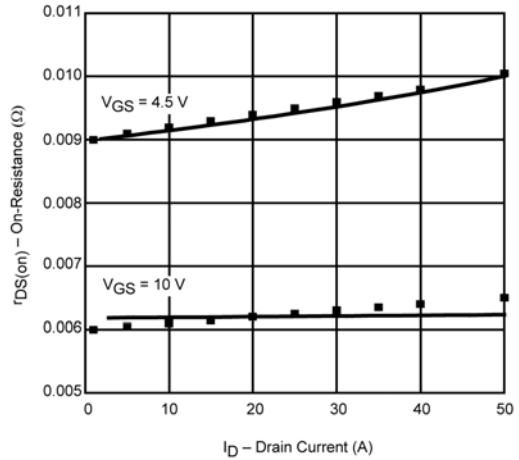
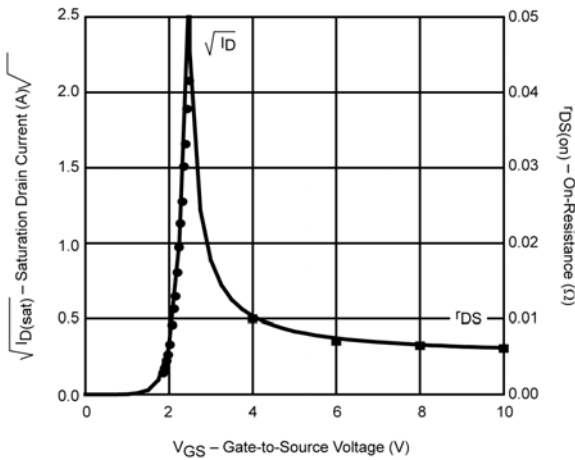
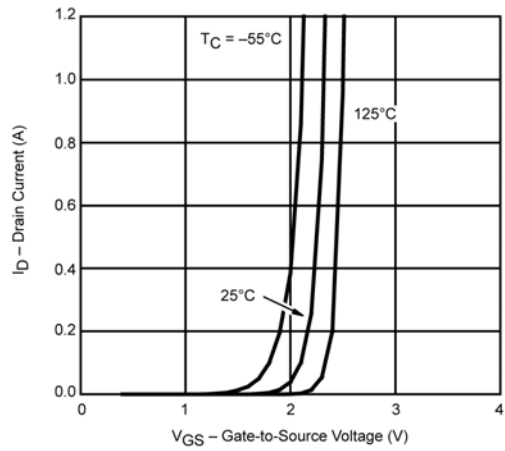
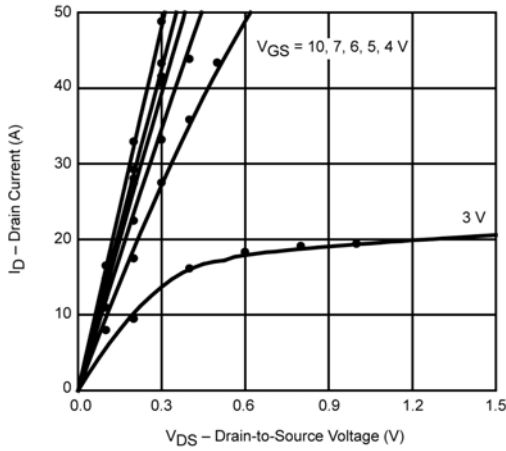
- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.



# SPICE Device Model Si7392ADP

## Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.