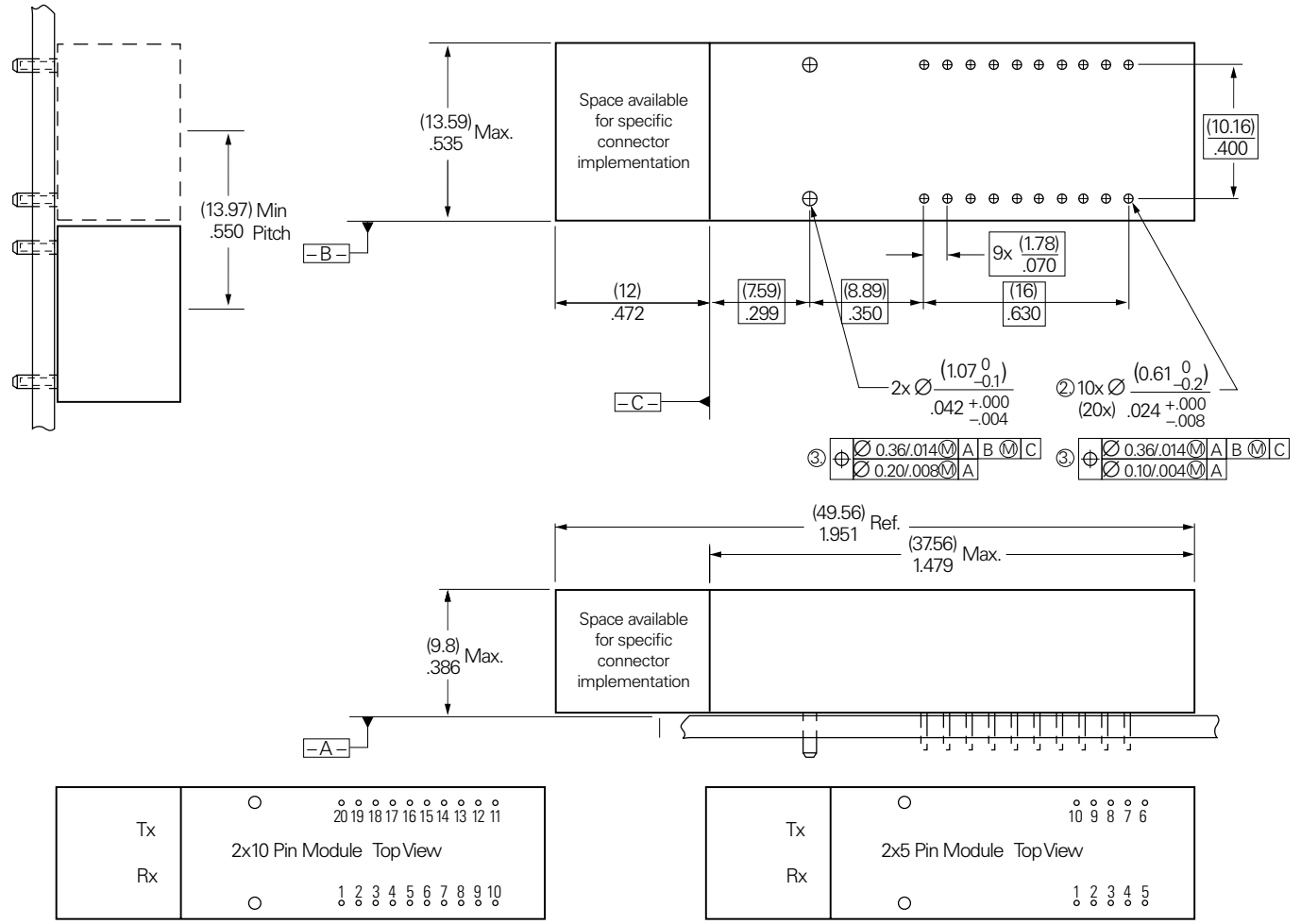
SIEMENS

V23818-C8-R10

Small Form Factor
Multimode 1300 nm LED Ethernet/Fast Ethernet/FDDI/ATM
155/194 MBd 2x5 Transceiver with MT-RJ Connector

Preliminary

Dimensions in (mm) inches



FEATURES

- **Small Form Factor transceiver unit for MT-RJ connector**
- **RJ-45 style connector system**
- **Half the size of SC Duplex 1x9 transceiver**
- **Fully compliant with all major standards**
- **SONET OC3**
- **Single power supply (+3.3 V)**
- **Extremely low power consumption < 0.7 W**
- **PECL differential inputs and outputs**
- **System optimized for 62.5/50 µm graded index fiber**
- **Multisource footprint**
- **Small footprint for high channel density**
- **UL-94 V-0 certified**
- **ESD Class 2 per MIL-STD 883 Method 3015**
- **Compliant with FCC (Class B) and EN 55022**
- **For distances of up to 2 km**

APPLICATIONS

- **ATM switches/bridges/routers, FDDI, Ethernet, Fast Ethernet**
- **Local area networks**
- **High speed computer links**
- **Switching systems**

Absolute Maximum Ratings

Exceeding any one of these values may destroy the device immediately.

Supply Voltage (V_{CC}–V_{EE}) ..... –0.5 V to 7 V
Data Input Levels (PECL) (V_{IN}) ..... V_{EE}–V_{CC}
Differential Data Input Voltage ..... 3 V
Operating Ambient Temperature (T_{AMB}) ..... 0 °C to 70°C
Storage Ambient Temperature (T_{STG}) ..... –40 °C to 85°C
Humidity/Temperature Test Condition (R_H) ..... 85%/85°C
Soldering Conditions, Temp/Time (T_{SOLD}/t_{SOLD})
(MIL-STD 883C, Method 2003) ..... 270 °C/10 s
ESD Resistance (all pins to V_{EE}, human body) ..... 1.5 kV
Output Current (I_O) ..... 50 mA

DESCRIPTION

The Siemens Ethernet/Fast Ethernet/FDDI/ATM transceiver—part of Siemens Small Form Factor transceiver family—is fully compliant with the Asynchronous Transfer Mode (ATM) OC-3 standard, the Fiber Distributed Data Interface (FDDI) Low Cost Fiber Physical Layer Medium Dependent (LCF-PMD) draft standard[1], and the FDDI PMD standard[2].

This transceiver supports the MT-RJ connectorization concept. It is compatible with RJ-45 style backpanels for fiber-to-the-desktop applications while providing the advantages of fiber optic technology. The receptacle accepts the new MT-RJ connector. The Small Form Factor is specially developed for distances of up to 2 km.

These transceivers also support 10 Base Fx 1300 nm with DC-free balanced coding (Manchester, 8B/10B).

Fast Ethernet was developed because of the higher bandwidth requirement in local area networking. It is based on the proven effectiveness of millions of installed Ethernet systems.

ATM was developed because of the need for multimedia applications, including real time transmission. The data rate is scalable and the ATM protocol is the basis of the broadband public networks being standardized in the International Telegraph and Telephone Consultative Committee (CCITT). ATM can also be used in local private applications.

FDDI is a Dual Token Ring standard developed in the U.S. by the Accredited National Standards Committee (ANSC) X3T9, within the Technical Committee X3T9.5. It is applied to the local area networks of stations, transferring data at 100 Mbits/s with a 125 MBaud transmission rate.

The inputs/outputs are PECL compatible and the unit operates with 3.3 V power supply. As an option, the data output stages can be switched to static levels during absence of light, as indicated by the Signal Detect function. It can be directly interfaced with available chipsets.

Regulatory Compliance

Feature	Standard	Comments
Electromagnetic Interference (EMI)	FCC Class B EN 55022 Class B CISPR 22	Noise frequency range: 30 MHz to 1 GHz
Immunity: Electrostatic Discharge	EN 61000-4-2 IEC 1000-4-2	Discharges of ± 15kV with an air discharge probe on thereceptacle cause no damage.
Immunity: Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 1000-4-3	With a field strength of 10 V/m rms, noise frequency ranges from 10 MHz to 1 GHz
Eye Safety	IEC 825-1	Class 1

Notes

1. FDDI Token Ring, Low Cost Fiber Physical Layer Medium Dependent (LCF-PMD) ANSI X3T9.5 / 92 LCF-PMD / Proposed Rev. 1.3, September 1, 1992. American National Standard.
2. FDDI Token Ring, Physical Layer Medium Dependent (PMD) ANSI X3.166-1990 American National Standard. ISO/IEC 9314-3: 1990.

TECHNICAL DATA

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	T_{AMB}	0		70	°C
Power Supply Voltage	V_{CC}–V_{EE}	3	3.3	3.6	V
Supply Current	I_{CC}			230	mA
Transmitter					
Data Input High Voltage	V_{IH}–V_{CC}	–1165		–880	mV
Data Input Low Voltage	V_{IL}–V_{CC}	–1810		–1475	
Threshold Voltage	V_{BB}–V_{CC}	–1380		–1260	
Input Data Rise/Fall, 20%–80%	t_R, t_F	0.4		1.3	ns
Data High Time[2]	t_{on}			1000	
Receiver					
Output Current	I_O			25	mA
Input Duty Cycle Distortion	t_{DCD}			1.0	ns
Input Data Dependent Jitter	t_{DDj}				
Input Random Jitter	t_{RJ}			0.76	
Input Center Wavelength	I_C	1260		1380	nm
Electrical Output Load[3]	R_L		50		W

Notes

1. For V_{CC}–V_{EE} (min., max.). 50% duty cycle. The supply current (I_{CC2}+I_{CC3}) does not include the load drive current (Icc1). Add max. 45 mA for the three outputs. Load is 50 Ω into V_{CC} –2V.
2. To maintain good LED reliability, the device should not be held in the ON state for more than the specified time. Normal operation should be done with 50% duty cycle.
3. To achieve proper PECL output levels the 50 Ω termination should be done to V_{CC} –2 V. For correct termination see the application notes.

Transmitter Electro-Optical Characteristics

Transmitter	Symbol	Min.	Typ.	Max.	Units
Data Rate	DR			170	MBaud
Launched Power (Average) into 62.5 µm Fiber[1, 2]	P_O	–20	–16	–14	dBm
Center Wavelength[2, 3]	λ_C	1270		1360	nm
Spectral Width (FWHM)[2, 4]	D_I			170	
Output Rise/Fall Time, 10%–90%[2, 5]	t_R, t_F	0.6		2.5	ns
Temperature Coefficient of Optical Output Power	TCp			0.03	dB/°C
Extinction Ratio (Dynamic)[2, 6]	ER			10	%
Optical Power Low[7]	P_{TD}			–45	dBm
Overshoot	OS			10	%
Duty Cycle Distortion[8, 9]	t_{DCD}			0.6	ns
Data Dependent Jitter[8, 10]	t_{DDJ}			0.3	
Random Jitter[8, 11]	t_{RJ}			0.6	

Notes

1. Measured at the end of 5 meters of 62.5/125/0.275 graded index fiber using calibrated power meter and a precision test ferrule. Cladding modes are removed. Values valid for EOL and worst-case temperature.
2. The input data pattern is a 12.5 MHz square wave pattern.
3. Center wavelength is defined as the midpoint between the two 50% levels of the optical spectrum of the LED.
4. Spectral width (full width, half max) is defined as the difference between 50% levels of the optical spectrum of the LED.
5. 10% to 90% levels. Measured using the 12.5 MHz square wave pattern with an optoelectronic measurement system (detector and oscilloscope) having 3 dB bandwidth ranging from less than 0.1 MHz to more than 750 MHz.
6. Extinction Ratio is defined as PL/PH x 100%. Measurement system as in Note 5.
7. Optical Power Low is the output power level when a steady state low data pattern (FDDI Quiet Line state) is used to drive the transmitter. Value valid <1 ms after input low.
8. Test method as for FDDI-PMD. Jitter values are peak-to-peak.
9. Duty Cycle Distortion is defined as 0.5 [(width of wider state) minus (width of narrower state)]. It is measured with stream of Idle Symbols (62.5 MHz square wave).
10. Measured with the same pattern as for FDDI-PMD.
11. Measured with the Halt Line state (12.5 MHz square wave).

Receiver Electro-Optical Characteristics

Receiver	Symbol	Min.	Typ.	Max.	Units
Data Rate	DR	5		170	MBaud
Sensitivity (Average Power)[1]	P_{IN}		–33	–31	dBm
Sensitivity (Average Power) Center[2]			–35.5		
Saturation (Average Power)[2]	P_{SAT}	–14	–11		
Duty Cycle Distortion[3, 4]	t_{DCD}			1	ns
Deterministic Jitter[4, 5]	t_{DJ}			1	
Random Jitter[4, 6]	t_{RJ}				
Signal Detect Assert Level[7]	P_{SDA}	–42.5		–30	dBm
Signal Detect Deassert Level[8]	P_{SDD}	–45		–31.5	
Signal Detect Hysteresis	P_{SDA}–P_{SDD}	1.5			dB
Output Low Voltage[9]	V_{OL}–V_{CC}	–1810		–1620	mV
Output High Voltage[9]	V_{OH}–V_{CC}	–1025		–880	
Output Data Rise/Fall Time, 20%–80%	t_R, t_F			1.3	ns
Output SD Rise/Fall Time, 20%–80%				40	

Notes

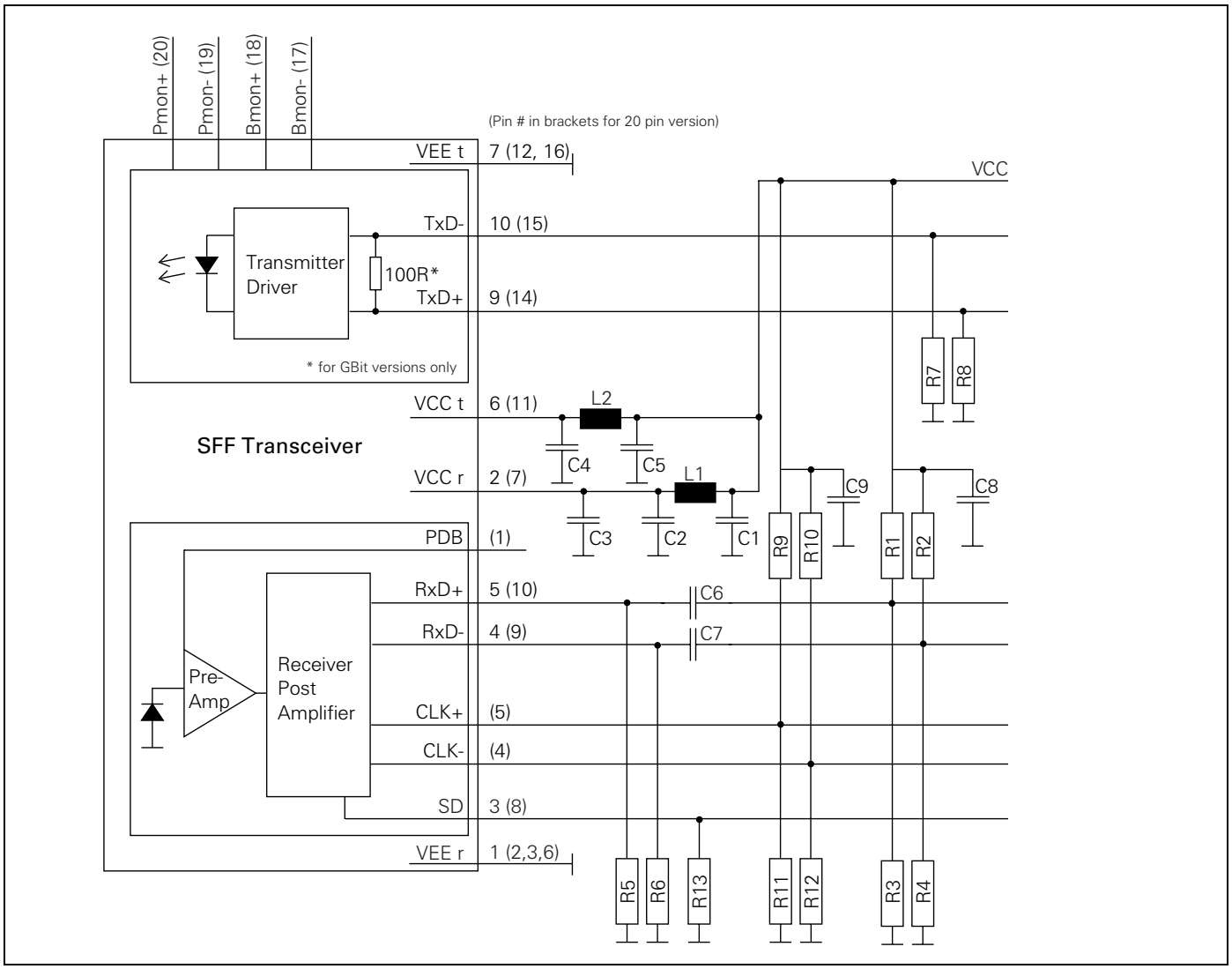
1. For a bit error rate (BER) of less than 1x10E–12 over a receiver eye opening of least 1.5 ns. Measured with a 2^{23}–1 PRBS at 155 MBd.
2. For a BER of less than 1x10E-12. Measured in the center of the eye opening with a 2^{23}-1 PRBS at 155 MBd.
3. Measured at an average optical power level of –20 dBm with a 62.5 MHz square wave.
4. All jitter values are peak-to-peak. RX output jitter requirements are not considered in the ATM standard draft. In general the same requirements as for FDDI are met.
5. Measured at an average optical power level of –20 dBm.
6. Measured at –33 dBm average power.
7. An increase in optical power through the specified level will cause the SIGNAL detect output to switch from a Low state to a High state.
8. A decrease in optical power through the specified level will cause the SIGNAL detect output to switch from a High state to a Low state.
9. PECL compatible. Load is 50 Ω into V_{CC} –2 V. Measured under DC conditions. For dynamic measurements a tolerance of 50 mV should be added.

Pin Description

Pin Name		Level/Logic	Pin#	Description
V_{EEr}	Receiver Signal Ground	N/A	1	
V_{CCr}	Receiver Power Supply	N/A	2	
SD	Signal Detect	PECL	3	Normal Operation: Logic "1" Output Fault Condition: Logic "0" Output
RD-	Received Data Out Bar	PECL	4	No internal terminations will be provided.
RD+	Received Data Out	PECL	5	No internal terminations will be provided.
V_{CCt}		N/A	6	Transmitter Power Supply
V_{EEt}		N/A	7	Transmitter Signal Ground
TDis		TTL	8	Optional use for Laser based products only.
TD+		PECL	9	Transmitter Data In
TD-		PECL	10	Transmitter Data In Bar See TD+ pin for terminations
MS	MS	N/A	MS	Mounting Studs The mounting studs are provided for transceiver mechanical attachment to the circuit board. They also provide an optional connection of the transceiver to the equipment chassis ground. The holes in the circuit board must be tied to chassis ground.

APPLICATION NOTES

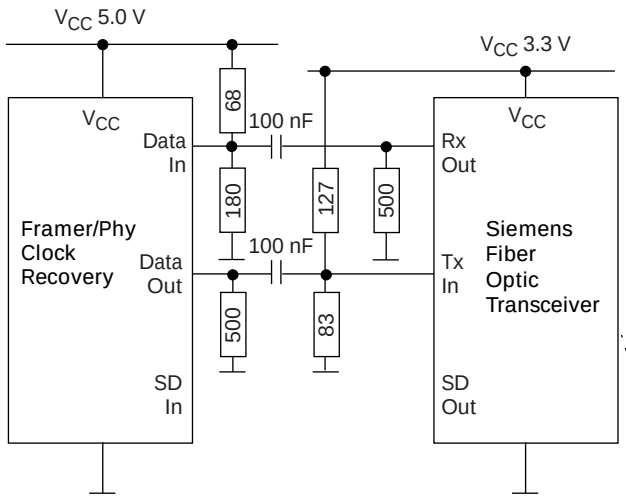
2x5 Pin Row Transceiver



Multimode 1300 nm LED Transceiver

Solutions for connecting a Siemens +3.3 V Fiber Optic Transceiver to a +5.0 V Framer-/Phy-Device.

Figure 1. Common GND



Inputs and outputs are differential and should be doubled. Signal Detect (SD) is single ended (if used).

Figure 1a. Circuitry for SD (Differential) and Common GND

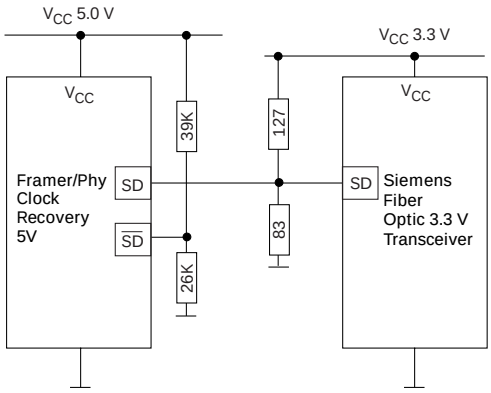


Figure 1b. Circuitry for SD (Single Ended) and Common GND

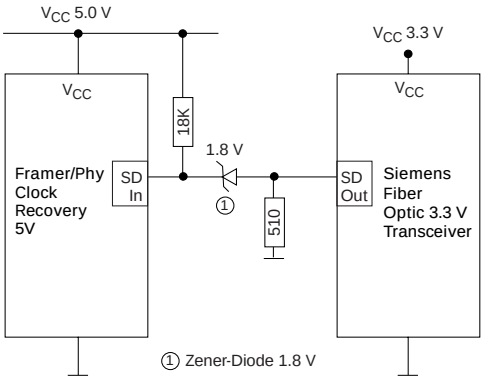
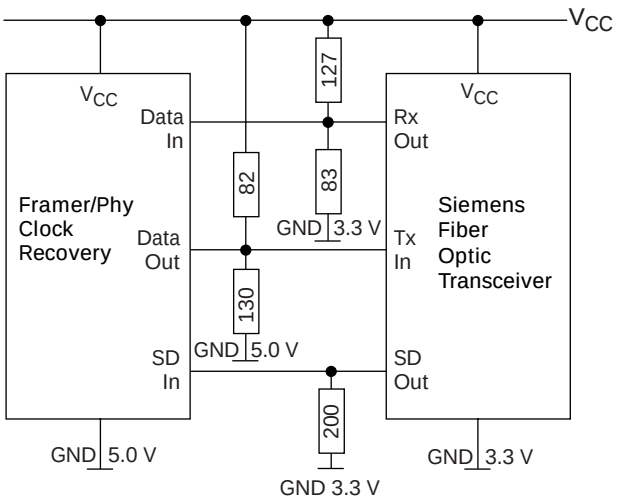


Figure 2. Common V_{CC}



Inputs and outputs are differential and should be doubled. Signal Detect (SD) is single ended.

Siemens Microelectronics, Inc. • Optoelectronics Division • 19000 Homestead Road • Cupertino, CA 95014 USA
Siemens Semiconductor Group • Fiber Optics • Wernerwerkdamm 16 • Berlin D-13623, Germany
Siemens K. K. • Fiber Optics • Takanawa Park Tower • 20-14, Higashi-Gotanda, 3-chome, Shinagawa-ku • Tokio 141, Japan
www.smi.siemens.com/opto/fo/fo.html (USA) • www.siemens.de/Semiconductor/products/37/376.htm (Germany)