PM5346

S/UNI-LITE

INTERFACING OF THE S/UNI-LITE TO CATV HEADEND MPEG CIRCUITRY

APPLICATION NOTE

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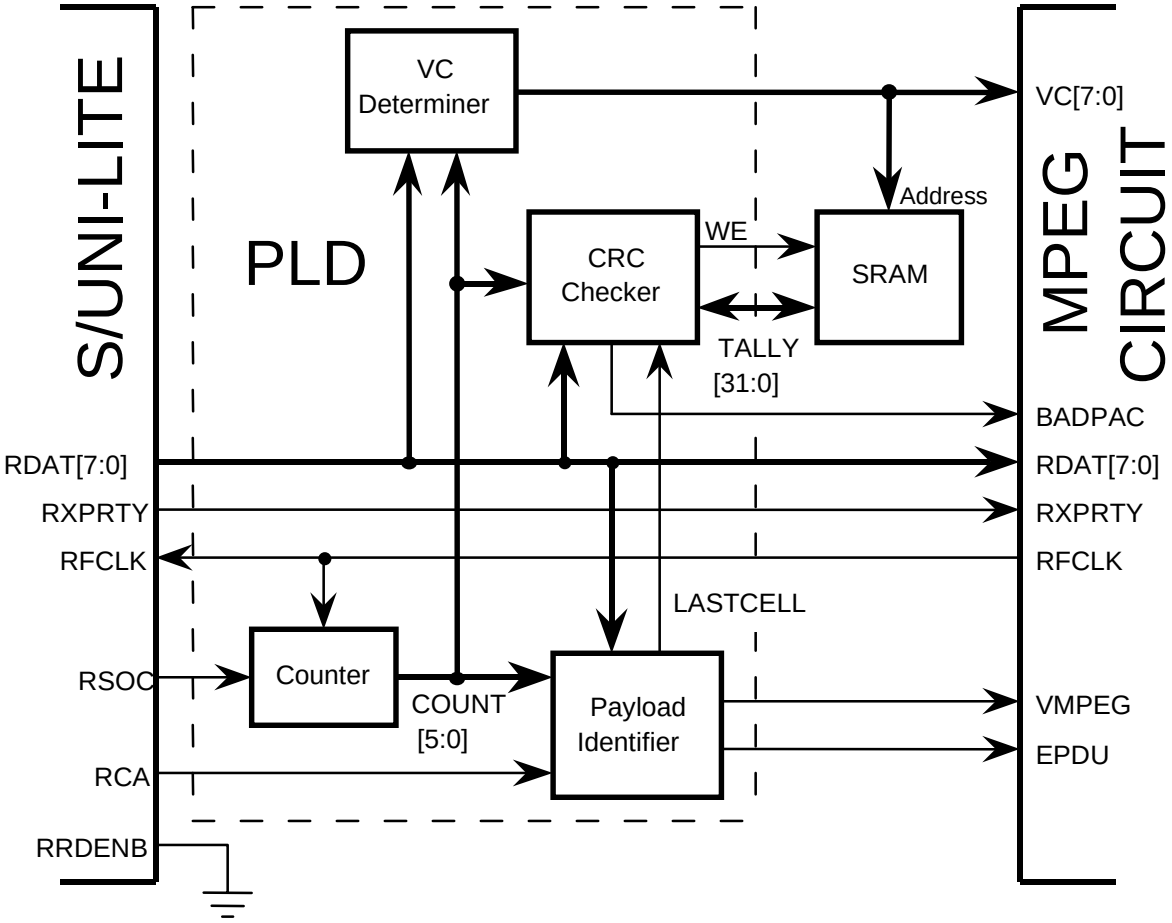
1 PMC S/UNI-LITE TO CATV HEADEND MPEG CIRCUITRY

This document describes how circuitry can be added to PMC-Sierra's S/UNI-LITE device (ATM UNI for 155 Mbit/s SONET - with integrated clock recovery) to facilitate the extraction of up to 256 MPEG streams carried in AAL5 cells. With this additional circuitry the S/UNI-LITE can be employed to connect ATM networks to CATV headend MPEG circuitry. The two main tasks of the interface circuitry are to identify the MPEG stream associated with each cell, and to perform a CRC check of each AAL5 PDU (each MPEG packet). The additional circuitry can be implemented with a PLD (programmable logic device) and a small SRAM.

Figure 1 - S/UNI-LITE Interfacing with CATV Headend MPEG Circuitry



1.1 Functional Description

Figure 1 shows the interfacing of a S/UNI-LITE device to the MPEG circuitry in a CATV headend. As stated previously, all of the necessary interface functionality can be fulfilled with a PLD and a SRAM.

The basic idea of the interface circuitry is to have the S/UNI-LITE continuously output ATM cells it has extracted from the SONET link. It is assumed that the MPEG circuitry can handle the payload contents of the cells as soon as they are output. As the cells are output from the S/UNI-LITE, the VC Determiner (a PLD functional block) inspects their headers to determine, through consideration of VPI/VCI values, what virtual circuit (VC) they are associated with. Each VC is a single MPEG stream. The circuit can handle an unlimited number of such VCs - although 128 or 256 would be the number typically desired.

The payload contents of each cell are passed on to the MPEG circuitry as RDAT[7:0]. In parallel with this passing of cell payload contents, a VMPEG signal (Valid MPEG) is passed which indicates whether the data on RDAT at any time is a byte from the payload of a valid cell. In addition, the VC value is passed to indicate what MPEG stream RDAT is associated with.

VC is also used to address the SRAM to facilitate CRC calculations. The SRAM contains the ongoing CRC calculation "tally" for each AAL5 PDU (MPEG packet). With VC as the address, intermediate CRC tallies (between cells in the same packet) are stored and later recovered for further calculation. When the last cell in a PDU arrives, the final CRC calculation for the whole PDU is compared to the expected value (a fixed constant) and the validity of the PDU is determined. If the CRC value is invalid, a BADPAC notification is sent to the MPEG circuitry in conjunction with the VC of the PDU concerned. This indication of an invalid PDU allows the MPEG circuitry to respond in some way.

The interface circuitry does not have to handle invalid ATM cell headers (identified through the use of the cell HEC byte) as the S/UNI-LITE can be programmed to discard all cells that have invalid headers. There is no point in indicating the occurrence of such cells to the MPEG circuitry, as there is no way of determining exactly which MPEG stream (VC) they are related to.

1.2 Description of Signals

The following signals exist in the interface between the S/UNI-LITE and the MPEG circuitry (all those to and from the S/UNI-LITE are part of the SCI-PHY interface specification - PMC's superset of the Utopia specification):

Table 1 - Signal Interconnection

SIGNAL	DIRECTION	DESCRIPTION
RDAT[7:0]	S/UNI to MPEG and PLD	Receive Data Carries the ATM cell bytes (header and payload) recovered from the SONET link.
RXPRTY	S/UNI to MPEG and PLD	Receive Parity Odd parity calculation over RDAT bits.
VC[7:0]	PLD to MPEG and SRAM	Virtual Circuit The VC (MPEG stream) number of the cell (MPEG) data on RDAT. Determined from the header of the cell.
BADPAC	PLD to MPEG	Bad Packet After the last cell of a MPEG packet (AAL5 PDU) has passed on RDAT this signal will go high if the CRC check found that packet to be invalid. When it goes high VC will still be indicating the MPEG stream of the packet concerned.
VMPEG	PLD to MPEG	Valid MPEG Indicates when valid MPEG data is passing on RDAT.

SIGNAL	DIRECTION	DESCRIPTION
EPDU	PLD to MPEG	End of PDU Indicates when the last byte of a MPEG packet (AAL5 PDU) is passing on RDAT.
RFCLK	MPEG to S/UNI and PLD	Receive FIFO Clock RFCLK is used to synchronize data transfers from the S/UNI-LITE to the MPEG circuitry. RFCLK may be 25 MHz or lower.
RSOC	S/UNI to PLD	Receive Start of Cell Marks the start of a new ATM cell on RDAT. When RSOC is high the first byte of a cell is present on RDAT.
RCA	S/UNI to PLD	Receive Cell Available Used by the S/UNI-LITE to indicate when a full cell is available to be read. When RRDENB is grounded it indicates (active high) simply that the current byte on RDAT is a byte from a valid ATM cell.

SIGNAL	DIRECTION	DESCRIPTION
RRDENB	S/UNI to ground	Receive Read Enable (active low) Indicates when a cell can be transferred out of the S/UNI-LITE on RDAT. Since it is assumed that the MPEG circuitry can process the ATM cells as soon as they arrive over the SONET link, RRDENB is grounded.
WE	PLD to SRAM	Write Enable Write enable signal for the SRAM.
TALLY[31:0]	PLD to SRAM (bi-directional)	CRC Tally Running value of CRC calculation stored in SRAM.

1.3 Description of the PLD Blocks

The functional blocks in the PLD operate in the following way (true = 1, false = 0, and all values are latched at the end of each RFCLK period):

1.3.1 Counter

Starts a byte count from zero each time RSOC indicates that a new cell is being carried on RDAT. This byte count is used to extract specific contents from each cell (VPI/VCI values for example). Because of the timing involved, the count value will be 0 when the second byte of a cell passes on RDAT, and 51 when the last byte passes. The count is clocked by RFCLK. When the count reaches 63 it stops at that value.

1.3.2 VC Determiner

Determines the VC (MPEG stream) of each cell passing on RDAT. It does so by inspecting the VPI/VCI value of each cell. In its simplest form, VC determination can be made by recovering the least significant 8 bits of the combined VPI/VCI

value. This approach requires that the VPI/VCI values be set at the cell source to fall into a contiguous range. More elaborate schemes for VC determination may be necessary if this assumption cannot be made. In the extreme, a proprietary technique developed by PMC for identifying VCs in the full 28 bit VPI/VCI range could be utilized.

Once VC has been determined it is latched until the next cell passes on RDAT.

1.3.3 Payload Identifier

To determine when the last cell of a PDU has arrived (using its PTI value):

```
LASTCELL = [(COUNT ≠ 2) • LASTCELL] +
           [(COUNT = 2) • RDAT[0] • not(RDAT[2]) • RCA]
```

To determine when a given byte carried on RDAT contains valid MPEG data:

```
VMPEG =   [(COUNT • 42) + (not(LASTCELL) • (COUNT • 50))] •
          (COUNT • 3) • RCA
```

And to determine when the last byte of a MPEG packet is passing on RDAT:

```
EPDU = (COUNT = 42) • LASTCELL • RCA
```

1.3.4 CRC Checker

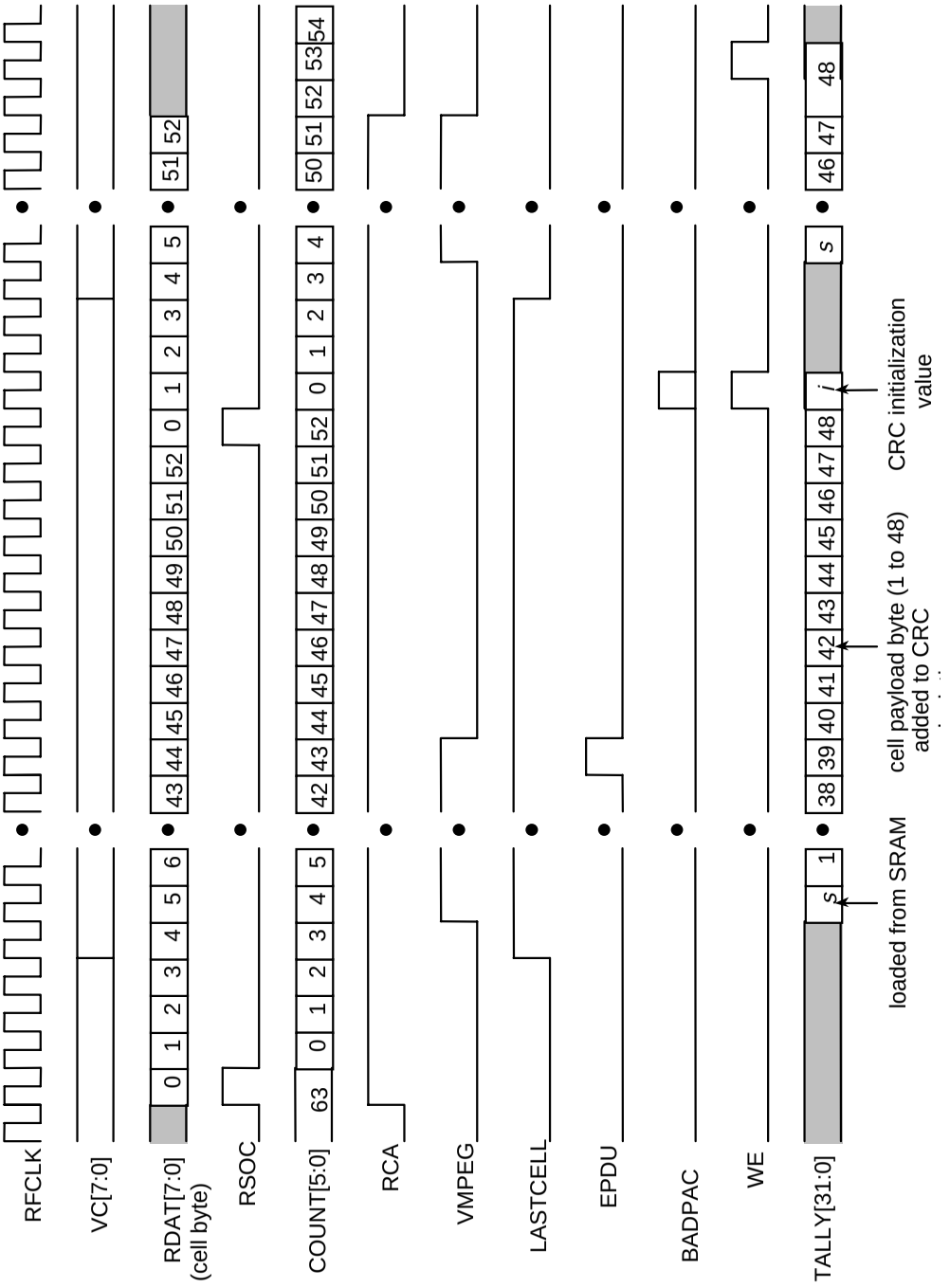
[Note that this description lacks full CRC calculation details for the function f_{CRC}(TALLY, RDAT).]

This block makes the CRC calculation that determines the validity of each AAL5 PDU (MPEG packet). It operates as follows (TALLY is intermediate CRC value):

```
TALLY     = SRAM output if (COUNT = 3)  [using VC as
address]
          =  fCRC(TALLY, RDAT) if (COUNT • 4) • (COUNT • 51)
          = TALLY   if (COUNT = 52) • not(LASTCELL)
          = CRC init. value   if (COUNT = 52) • LASTCELL
WE        = (COUNT = 52)
```

BADPAC = (COUNT = 52) • LASTCELL • (TALLY ≠ expected CRC total)

Figure 2 - Functional Timing of S/UNI-LITE to MPEG Circuitry



1.4 Interface Timing

Figure 2 shows the functional timing of events in the circuitry being described. AC timing details for the S/UNI-LITE are available in the specification for that device. AC timing for the rest of the circuitry depends on the components chosen.

1.5 Disclaimer

The information contained in this document is believed to be correct; however it has not been verified in real operation.

1.6 References

1. PMC-Sierra, Inc., PM5346 S/UNI-LITE Data Sheet, Issue 3, May, 1994.

NOTES

NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

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