PM7545
S/UNI-PDH-EVBD

REFERENCE DESIGN FOR S/UNI-PDH

Preliminary Information

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OVERVIEW

The PM7545 S/UNI-PDH EVBD is a versatile board used to perform functional testing of the S/UNI-PDH PM7345 chip (PDH). The board allows for complete functional testing of the S/UNI-PDH device at DS3 and E3 rates of 44.736 Mbit/s and 34.368 Mbit/s, as well as at DS1 and E1 rates of 1.544 Mbit/s and 2.048 Mbit/s. The board can be used with the SATURN COMPLIANT INTERFACE FOR ATM PHYSICAL LAYER INTERCONNECT EVALUATION MOTHER BOARD (SCI-PHY EVMB), or it can be used stand alone with reduced functionality. The S/UNI-PDH EVBD is normally configured, monitored, and powered through two 96 pin DIN connectors that mate directly to the SCI-PHY EVMB. There is a power connector and fuse for the application of +5V and ground directly to the S/UNI-PDH EVBD.

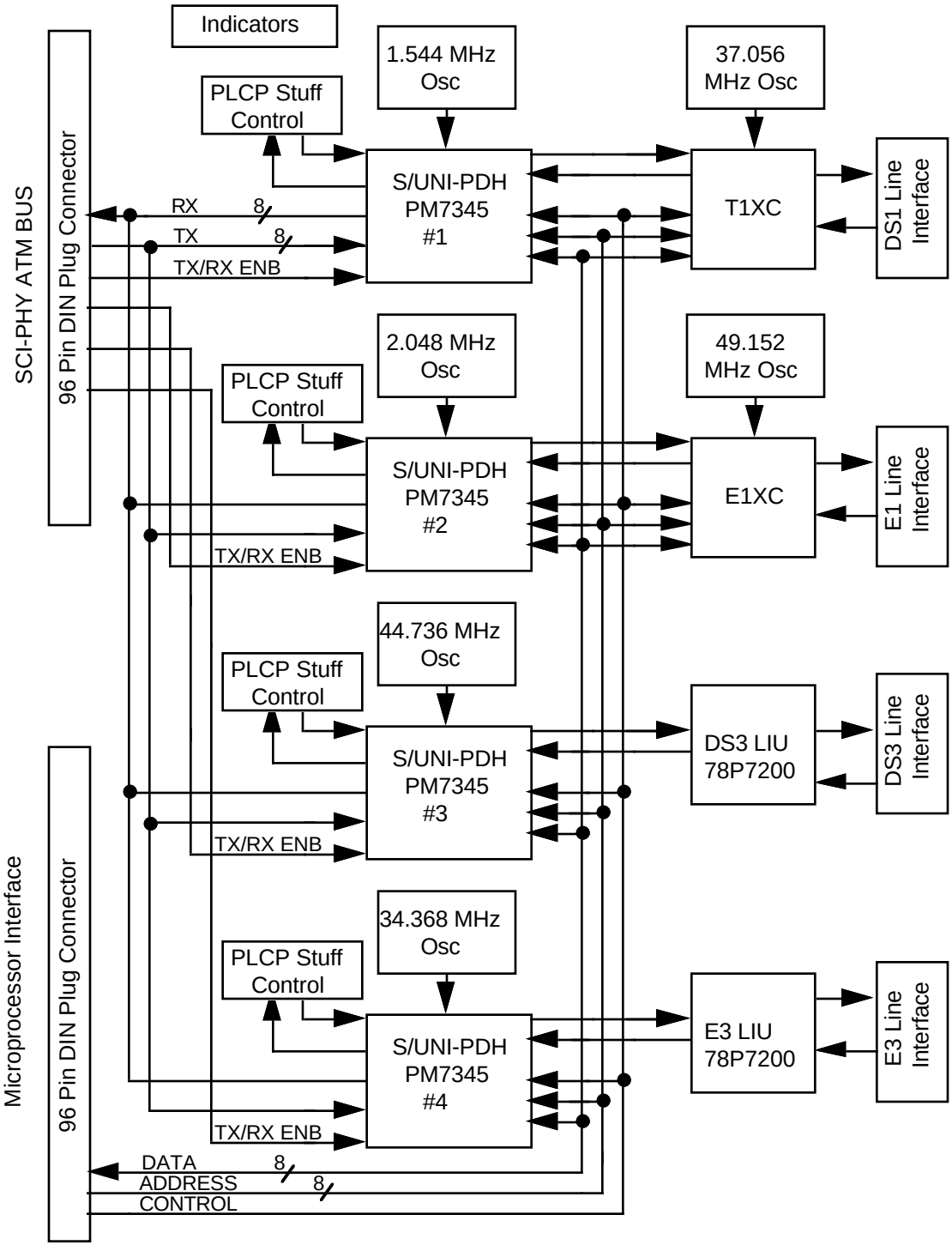
There are four PM7345 S/UNI-PDH devices on the S/UNI-PDH EVBD. One PM7345 is configured for operation at DS1, another one at E1, one at DS3, and the last one at E3. The rate that each S/UNI-PDH works at is fixed by the board design. The DS1 format S/UNI-PDH utilizes the PMC PM4341 T1XC T1 framer and transceiver. The DS3/E3 format S/UNI-PDHs utilize the internal PDH T3/E3 framer and the external Silicon Systems SSI78P7200 DS3/E3 LIU. The E1 format S/UNI-PDH utilizes the PMC PM6341 E1XC E1 framer and transceiver. The E3 format S/UNI-PDH can also be put into a special Loopback mode whereby parallel ATM bus receive signals are looped back into the transmit side. The rest of the S/UNI-PDH devices will not function in this mode. Line side connections use BNC and Bantam connectors. One of the 96 pin DIN connectors is a generic microcontroller port. The second 96 pin DIN connector contains signals necessary to implement ATM cell transfer.

All four S/UNI-PDH PM7345 devices have microprocessor interfaces that are accessible through the DIN connector. Control of the T1XC, E1XC, and 78P7200 devices is accomplished via the same connector. Twenty four general purpose parallel input/output (PIO) lines are also accessible through the same connector. PIO lines are used to control and monitor various signals on the S/UNI-PDH EVBD. Headers are provided for PLCP and DS3/E3 overhead insertion and extraction. Headers are also provided for HDLC signals and other pertinent control/status signals.

Each S/UNI-PDH PM7345 is independently configurable and has its own LIU. All four PM7345 share data signals on the ATM bus side and are individually selectable under microprocessor control.

FUNCTIONAL DESCRIPTION

Fig 1. Block Diagram



SCI-PHY Interface

The SCI-PHY interface provides a standard connection to the S/UNI-PDH ATM drop side according the SCI-PHY specification. The 96 pin DIN SCI-PHY connector contains parallel ATM receive and transmit signals along with the required FIFO control signals and clocks. The PDH devices on the S/UNI-PDH EVBD utilize 8 bit parallel transmit and receive ATM transfers. The SCI-PHY interface contains signals that support multiple physical layer devices. Since there are four S/UNI-PDH PM7345 on the EVBD, the SCI-PHY interface will be supporting its maximum number of physical layer devices. Also included in the SCI-PHY connector is a +5V supply. The SCI-PHY interface was designed to be electrically compatible with the SCI-PHY EVMB.

Microprocessor interface

The Microprocessor interface is a generic microprocessor interface. The interface contains data, address, and control lines compatible with the SCI-PHY EVMB microprocessor interface and is available on a 96 pin DIN connector. These signals are directly connected to the microprocessor ports on the four S/UNI-PDH PM7345 devices, the T1XC, and the E1XC. Six chip select lines are use to control the programmable devices on the board. In addition, this interface contains 24 parallel input/output (PIO) lines, 16 of which are used by the S/UNI-PDH EVBD. The mother board's PIO lines come from an undedicated 8255 PIO on that board. PIO lines are used to provide control over each PM7345's 8 kHz reference for PLCP stuff control (C13/CADD). PIO lines are used to control the two 78P7200 devices. PIO input lines are used to monitor low received line signal level on the 78P7200 LIUs. PIO inputs also monitor Loss of Frame signals from the PM7345s.

Indicators

There are five LEDs provided for visual status. One LED lights when a source of five volts is provided to the S/UNI-PDH EVBD. The other four LEDs light up when Loss of Cell Delineation (LCD) occurs for the individual S/UNI-PDH PM7345 chips.

PM7345 S/UNI-PDH

The PM7345 devices are the heart of the S/UNI-PDH EVBD. They are ATM physical layer processors with integrated DS3 and E3 framing. PLCP sublayer DS1, DS3, E1, and E3 processing is supported as is ATM cell delineation. All traffic goes through the PM7345s. Each PM7345 is setup through the microprocessor interface. All the internal registers are accessed through this interface.

When a PM7345 is configured for DS3 transmission, the overhead bits are inserted and extracted on an external serial interface. The DS3 overhead interface signals are brought out to a header. When PLCP framing is enabled, the PLCP overhead octets are inserted and extracted on an external serial interface that is also brought out to headers. All ATM data is passed through the parallel SCI-PHY data bus.

Because there are four physical layer devices sharing the ATM parallel data buses, device select signals on the SCI-PHY DIN connector are utilized to select a particular PM7345 in the transmit and receive directions. S/UNI-PDH device 4 can be put into a special Loopback mode using jumpers on the board. This will allow Loopback testing on the ATM parallel bus side. All other S/UNI-PDH devices do not function in this mode.

When a PM7345 is configured for DS1 or E1 transmission sublayer processing, a unipolar signal with the appropriate clock and framing is provided and expected.

For a complete description of the PM7345, refer to the PM7345 data sheet.

On Board Oscillators

Each S/UNI-PDH PM7345 device requires an oscillator feeding its TICLK pin . This clock source is used to generate the transmit clock for line side transmissions. S/UNI-PDH device 1 uses a 1.544 MHz oscillator for DS1 transmissions. S/UNI-PDH device 2 uses a 2.048 MHz oscillator for E1 transmissions. S/UNI-PDH device 3 uses a 44.736 MHz oscillator for DS3 transmissions. S/UNI-PDH device 4 uses a 34.368 MHz oscillator for E3 transmissions. The T1XC device uses a 37.056 MHz oscillator on pin XCLK for internal timing generation. The E1XC device uses a 49.152 MHz oscillator on pin XCLK for internal timing generation.

PLCP Stuff Control

The PM7345 S/UNI-PDH devices provide stuffing control for T3 PLCP (nibble stuffing) and E3 PLCP (byte stuffing) frame formats via the C13/CADD pin. The PLCP Stuff Control block allows this pin to be controlled by one of two reference sources to produce a nominal 125 microsecond PLCP frame rate. The source is either the result of a phase comparison between the transmit PLCP frame rate and receive PLCP frame rate (loop time operation) or the result of a phase comparison between the transmit PLCP frame rate and a generated 8 KHz clock. The 8 KHz clock is generated using the onboard 1.544 MHz crystal oscillator and 22V10 PALs.

T1XC

The PM4341 T1XC is a full featured T1 transceiver with an integrated framer and line analog circuitry. A 37.056 MHz oscillator is used by its internal digital PLL for clock and data recovery. All internal registers for configuration, control, and status monitoring are accessible through its microprocessor interface. The analog line interface is brought out to Bantam connectors. Headers are provided for the digital transmit and receive interface as well as the facility data link (FDL) interface. Also note that the T1XC is connected on the digital signal side to PM7345 S/UNI-PDH device 1.

For a complete description of the T1XC, refer to the PM4341 datasheet**.**

E1XC

The PM6341 E1XC is a full featured E1 transceiver with an integrated framer and line analog circuitry. A 49.152 MHz oscillator is used by its internal digital PLL for clock and data recovery. All internal registers for configuration, control, and status monitoring are accessible through its microprocessor interface. The analog line interface is brought out to Bantam connectors. Headers are provided for the digital transmit and receive interface as well as the facility data link (FDL) interface. Also note that the E1XC is connected on the digital signal side to PM7345 S/UNI-PDH device 2.

For a complete description of the E1XC, refer to the PM6341 datasheet

DS3 LIU

A Silicon Systems 78P7200 DS3 line interface unit (LIU) is used to convert the digital B3ZS-encoded AMI encoded data to its analog equivalent and to convert analog B3ZS-encoded AMI to its digital equivalent. The LIU has 3 main control inputs for controlling the transmitter. If the received signal falls below the required threshold, a status signal, LOWSIGB, is asserted. The transmitter control and LOWSIGB signals are accessible via PIO lines. These lines would be under microprocessor control if the SCI-PHY EVMB was connected to the S/UNI-PDH EVBD. Also note that the 78P7200 DS3 LIU is connected on the digital signal side to PM7345 S/UNI-PDH device 3.

For a complete description of the 78P7200, refer to the datasheets in Silicon Systems Communication Products databook.

E3 LIU

A Silicon Systems 78P7200 E3 line interface unit (LIU) is used to convert the digital HDB3-encoded AMI encoded data to its analog equivalent and to convert analog HDB3-encoded AMI to its digital equivalent. The LIU has 3 main control inputs for controlling the transmitter. If the received signal falls below the required threshold, a status signal, LOWSIGB, is asserted. The transmitter control and LOWSIGB signals are accessible via PIO lines. These lines would be under microprocessor control if the SCI-PHY EVMB were connected to the S/UNI-PDH EVBD. Also note that the 78P7200 E3 LIU is connected on the digital signal side to PM7345 S/UNI-PDH device 4.

For a complete description of the 78P7200, refer to the datasheets in Silicon Systems Communication Products databook.

DS1 Line Interface

The S/UNI-PDH EVBD provides for the standard DS1 100 ohm analog interface. Two Bantam connectors are provided.

E1 Line Interface

The S/UNI-PDH EVBD provides for the standard E1 120 ohm analog interface. Two Bantam connectors are provided.

DS3 Line Interface

The S/UNI-PDH EVBD provides for the standard DS3 75 ohm analog interface. Two BNC connectors are provided.

E3 Line Interface

The S/UNI-PDH EVBD provides for the standard E3 75 ohm analog interface. Two BNC connectors are provided.

S/UNI-PDH EVBD CONNECTOR SIGNAL DESCRIPTIONS

Daughterboard Microprocessor Connector

The Daughterboard Microprocessor Connector Interface is made up of a 96 pin DIN plug connector designed to mate with a corresponding connector on the SCI-PHY mother board. The connector consists of signals appropriate to read and write the registers of the S/UNI-PDH EVBD. It also provides the necessary power and ground. CMOS signal levels are used on this interface.

Signal Name	Type	Pin	Function
PIO1A[0]	I	A1	Connected to C13REF1. This signal selects between the 1.544 MHz crystal (divided by 193) or RPOHFP1 as the onboard source of the C13/CADD pin on S/UNI-PDH device 1.
PIO1A[1]	I	A2	Connected to C13REF2. This signal selects between the 1.544 MHz crystal (divided by 193) or RPOHFP2 as the onboard source of the C13/CADD pin on S/UNI-PDH device 2.
PIO1A[2]	I	A3	Connected to C13REF3. This signal selects between the 1.544 MHz crystal (divided by 193) or RPOHFP3 as the onboard source of the C13/CADD pin on S/UNI-PDH device 3.
PIO1A[3]	I	A4	Connected to C13REF4. This signal selects between the 1.544 MHz crystal (divided by 193) or RPOHFP4 as the onboard source of the C13/CADD pin on S/UNI-PDH device 4.
PIO1A[4]	I	A5	Connected to C13SEL1. This signals controls which 8 kHz reference signal goes to the C13/CADD pin on S/UNI-PDH device 1
PIO1A[5]	I	A6	Connected to C13SEL2. This signals controls which 8 kHz reference signal goes to the C13/CADD pin on S/UNI-PDH device 2.
PIO1A[6]	I	A7	Connected to C13SEL3. This signals controls which 8 kHz reference signal goes to the C13/CADD pin on S/UNI-PDH device 3.
PIO1A[7]	I	A8	Connected to C13SEL4. This signals controls which 8 kHz reference signal goes to the C13/CADD pin on S/UNI-PDH device 4.
PIO1B[0]	O	A9	Connected to LOF1. Loss of frame for S/UNI-PDH device 1.
PIO1B[1]	O	A10	Connected to LOF2. Loss of frame for S/UNI-PDH device 2.

PIO1B[2]	O	A11	Connected to LOF3. Loss of frame for S/UNI-PDH device 3
PIO1B[3]	O	A12	Connected to LOF4. Loss of frame for S/UNI-PDH device 4.
PIO1B[4]	O	A13	Not used
PIO1B[5]	O	A14	Not used
PIO1B[6]	O	A15	Connected to DS3LOWSIG. Low receive line level for DS3 78P7200 LIU.
PIO1B[7]	O	A16	Connected to E3LOWSIG. Low receive line level for E3 78P7200 LIU.
PIO1C[0]	I	A17	Connected to DS3LBO. Controls line buildout function on DS3 78P7200 LIU.
PIO1C[1]	I	A18	Connected to DS3OPT1. Controls transmitter output power on DS3 78P7200 LIU.
PIO1C[2]	I	A19	Connected to DS3OPT2. Controls transmitter enable on DS3 78P7200 LIU.
PIO1C[3]	I	A20	Not used
PIO1C[4]	I	A21	Connected to E3LBO. Controls line build out function on E3 78P7200 LIU.
PIO1C[5]	I	A22	Connected to E3OPT1. Controls transmitter output power on E3 78P7200 LIU.
PIO1C[6]	I	A23	Connected to E3OPT2. Controls transmitter enable on E3 78P7200 LIU.
PIO1C[7]	I	A24	Not used
CSB0	I	A25	Active low chip select for S/UNI-PDH device 1. Active address range C000H - C0FFH.
CSB1	I	A26	Active low chip select for S/UNI-PDH device 2. Active address range C100H - C1FFH.
CSB2	I	A27	Active low chip select for S/UNI-PDH device 3. Active address range C200H - C2FFH.
CSB3	I	A28	Active low chip select for S/UNI-PDH device 4. Active address range C300H - C3FFH.
CSB4	I	A29	Active low chip select for T1XC. Active address range C400H - C4FFH.
CSB5	I	A30	Active low chip select for E1XC. Active address range C500H - C5FFH.
CSB6	NC	A31	Not used
CSB7	NC	A32	Not used.
GND	P	B1 to B26	Ground.
PWR+5V	P	B27 to B32	+5V power.

RST	NC	C1	Not Connected
RSTB	I	C2	Active low hardware reset connected to RSTB line of S/UNI-PDH devices, T1XC, and E1XC.
WRB	I	C3	Active low write strobe to S/UNI-PDH devices, T1XC, and E1XC.
RDB	I	C4	Active low read strobe to S/UNI-PDH devices, T1XC, and E1XC.
ALE	I	C5	Address latch enable. When high, identifies that address is valid on D[7:0]. Connected to the four S/UNI-PDH devices, T1XC, and E1XC.
HC11_IRQB	O	C6	Maskable 68HC11 interrupt. Connected to the four S/UNI-PDH devices, the T1XC, and the E1XC interrupt pins (INTB).
HC11_ XIRQB	NC	C7	Not used
PIO_RSTB	NC	C8	Not used
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O I/O I/O I/O I/O I/O I/O I/O	C9 C10 C11 C12 C13 C14 C15 C16	Eight bit microprocessor data bus. Connected to the four S/UNI-PDH devices, T1XC, and the E1XC data lines.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10] A[11] A[12] A[13] A[14] A[15]	I I I I I I I I NC NC NC NC NC NC NC NC	C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32	Sixteen bit microprocessor address bus. Lower eight bits are connected to the S/UNI-PDH devices, T1XC, and E1XC address lines. Higher address lines are unconnected.

Daughterboard SCI-PHY Connector Interface

The Daughterboard SCI-PHY connector is the parallel ATM drop side interface made up of a 96 pin DIN plug connector and is designed to mate with a corresponding connector on the SCI-PHY mother board. It consists of signals required by the SCI-PHY interface. Please refer to the PMC-940212, SATURN COMPLIANT INTERFACE FOR ATM DEVICES document for interface timing details. CMOS signal levels are used on this interface.

Signal Name	Type	Pin	Function
TDAT[0]	I	A1	Transmit Data. TDAT[7:0] is used to transfer ATM cells to an ATM PHY daughterboard. TDAT[15:8] are not connected.
TDAT[1]	I	A2	
TDAT[2]	I	A3	
TDAT[3]	I	A4	
TDAT[4]	I	A5	
TDAT[5]	I	A6	
TDAT[6]	I	A7	
TDAT[7]	I	A8	
TDAT[8]	NC	A9	
TDAT[9]	NC	A10	
TDAT[10]	NC	A11	
TDAT[11]	NC	A12	
TDAT[12]	NC	A13	
TDAT[13]	NC	A14	
TDAT[14]	NC	A15	
TDAT[15]	NC	A16	
RDAT[0]	O	A17	Receive Data. RDAT[8:0] is used to transfer ATM cells from an ATM PHY daughterboard. RDAT[15:8] are not connected.
RDAT[1]	O	A18	
RDAT[2]	O	A19	
RDAT[3]	O	A20	
RDAT[4]	O	A21	
RDAT[5]	O	A22	
RDAT[6]	O	A23	
RDAT[7]	O	A24	
RDAT[8]	NC	A25	
RDAT[9]	NC	A26	
RDAT[10]	NC	A27	
RDAT[11]	NC	A28	
RDAT[12]	NC	A29	
RDAT[13]	NC	A30	
RDAT[14]	NC	A31	
RDAT[15]	NC	A32	

GND	P	B1 to B23	Ground.
PWR-2V	NC	B24	Not Connected.
PWR-4.5V	NC	B25 to B28	Not Connected.
PWR+5V	P	B29 to B32	+5V power.
TFCLK	I	C1	Supplies S/UNI-PDH devices with a TFCLK signal up to 25 MHz.
GND	P	C2	Ground.
TSOC	I	C3	Transmit Start Of Cell. TSOC marks the start of cell on the TDAT bus. TSOC drives all S/UNI-PDH devices' TSOC input.
TXPRTY[0]	I	C4	Transmit Parity. TXPRTY[0] drives all S/UNI-PDH devices' TXPRTY input.
TXPRTY[1]	NC	C5	Not connected
TCA1	O	C6	Transmit cell available. Connected to S/UNI-PDH device 1 TCA output.
TCA2	O	C7	Transmit cell available. Connected to S/UNI-PDH device 2 TCA output.
TCA3	O	C8	Transmit cell available. Connected to S/UNI-PDH device 3 TCA output.
TCA4	O	C9	Transmit cell available. Connected S/UNI-PDH device 4 TCA output.
TWREN1B	I	C10	The Transmit Write Enable. TWREN1B drives the TWRENB signal of S/UNI-PDH device 1.
TWREN2B	I	C11	The Transmit Write Enable. TWREN2B drives the TWRENB signal of S/UNI-PDH device 2.
TWREN3B	I	C12	The Transmit Write Enable. TWREN3B drives the TWRENB signal of S/UNI-PDH device 3.
TWREN4B	I	C13	The Transmit Write Enable. TWREN4B drives the TWRENB signal of S/UNI-PDH device 4.
PD2_MISO	NC	C14	Not connected
PD3_MOSI	NC	C15	Not connected
GND	P	C16	Ground.
RFCLK	I	C17	Receive FIFO clock. RFCLK is used to synchronize data transfer transactions from the ATM PHY daughterboard. RFCLK supplies a 25 MHz clock and is connected to all S/UNI-PDH devices' RFCLK input.
GND	P	C18	Ground.

RSOC	O	C19	Receive Start Of Cell. RSOC marks the start of cell on the RDAT bus. When RSOC is high, the first word of the cell structure should be present on the RDAT bus. RSOC is sampled on the rising edge of RFCLK and is considered valid only when RRDENB is simultaneously asserted. RSOC is connected to each S/UNI-PDH devices' RSOC output.
RXPRTY[0]	O	C20	Receive parity. RXPRTY[0] should indicate the parity of the RDAT[7:0] bus. RXPRTY[0] is connected to all S/UNI-PDH devices' RXPRTY output.
RXPRTY[1]	NC	C21	Not Connected
RCA1	O	C22	Receive Cell Available. RCA1 is used by an ATM physical layer device to indicate when it can provide a full cell. RCA1 is connected to the S/UNI-PDH device 1 RCA output.
RCA2	O	C23	Receive Cell Available. RCA2 is used by an ATM physical layer device to indicate when it can provide a full cell. RCA2 is connected to the S/UNI-PDH device 2 RCA output.
RCA3	O	C24	Receive Cell Available. RCA3 is used by an ATM physical layer device to indicate when it can provide a full cell. RCA3 is connected to the S/UNI-PDH device 3 RCA output.
RCA4	O	C25	Receive Cell Available. RCA4 is used by an ATM physical layer device to indicate when it can provide a full cell. RCA4 is connected to the S/UNI-PDH device 4 RCA output.
RRDEN1B	I	C26	The Receive Read Enable. RRDEN1B is connected to S/UNI-PDH device 1 RRDENB input.
RRDEN2B	I	C27	The Receive Read Enable. RRDEN2B is connected to S/UNI-PDH device 2 RRDENB input.
RRDEN3B	I	C28	The Receive Read Enable. RRDEN3B is connected to S/UNI-PDH device 3 RRDENB input.
RRDEN4B	I	C29	The Receive Read Enable. RRDEN4B is connected to S/UNI-PDH device 4 RRDENB input.
PD4_SCLK	NC	C30	Not connected
PD5_SS	NC	C31	Not connected
BUS8	NC	C32	Not connected

Line Interface Signals

The S/UNI-PDH EVBD contains four S/UNI-PDH devices that operate with four different line interface formats. These input and output signals are transformer isolated.

Signal+	Signal-	Description
TXDS1P	TXDS1N	DS1 balanced TX outputs.
RXDS1P	RXDS1N	DS1 balanced RX inputs.
TXE1P	TXE1N	E1 balanced TX outputs.
RXE1P	RXE1N	E1 balanced RX inputs.
TXDS3P	TXDS3N	DS3 unbalanced TX outputs.
RXDS3N	RXDS3N	DS3 unbalanced RX inputs.
TXE3P	TXE3N	E3 unbalanced TX outputs.
RXE3P	RXE3N	E3 unbalanced RX inputs.

Header Descriptions

Several jumper terminals are used as test headers to test and monitor certain S/UNI-PDH EVBD signal lines. CMOS signal levels are used for all inputs and outputs.

Header J4 (page 2 of schematics)

Header J4 is a 5 row by 2 column header whose function is to monitor signals common to the four S/UNI-PDH devices. The selection of operating modes is given in the OPERATION section. The signals on the header are described in the next table.

Signal	PIN #	Description
TFCLK	1	ATM Transmit FIFO clock. Clock for transferring ATM parallel data into the S/UNI-PDH devices.
+5V	2	Power
RFCLK	3	ATM Receive FIFO clock. Clock for transferring ATM parallel data out of the S/UNI-PDH devices.
+5V	4	Power
TSOC	5	Transmit start of Cell. TSOC marks the start of cell on the TDAT data bus.
GND	6	Ground
RSOC	7	Receive start of cell. RSOC marks the start of cell on the RDAT data bus.
GND	8	Ground
IRQB	9	Maskable interrupt to the controlling microprocessor via the microprocessor interface.
GND	10	Ground

Headers J13, J12, J9, J20 (pages 3, 4, 5, 6 of schematics)

Headers J13, J12, J9, J20 are 8 row by 2 column headers. These headers are described together because they serve identical functions for each S/UNI-PDH device. They are used to monitor HDLC signals as well as TICLK and LCD for the four S/UNI-PDH devices. They are also used to bring an external source of 8 kHz signal via EXTC13 for C13/CADD generation, and to control the TSEN input for each S/UNI-PDH device. J13 services S/UNI-PDH device 1, J12 is for device 2, J9 is for device 3, and J20 is for device 4. The signals on the headers are described in the next table. Note that each signal has an * at the end of its name. When referring to a specific signal on the header for a S/UNI-PDH device, just replace the * with the S/UNI-PDH device number (1 to 4).

Signal	PIN #	Description
GND	1	Ground
TDLSIG*	2	HDLC transmit data input to S/UNI-PDH.
GND	3	Ground
TDLCLK*	4	HDLC transmit data clock.
GND	5	Ground
TSEN*	6	Tristate enable for RDAT bus, RXPRTY, and RSOC pins. When TSEN is a logic 0 RDAT bus , RXPRTY, and RSOC are always active and are forced to digital logic values.
GND	7	Ground
RDLCLK*	8	HDLC receive data clock.
GND	9	Ground
RDLSIG*	10	HDLC receive data output from S/UNI-PDH.
GND	11	Ground
EXTC13*	12	External source for 8 kHz signal for C13/CADD generation.
GND	13	Ground
TICLK*	14	TICLK is the S/UNI-PDH transmission system baud clock.
GND	15	Ground
LCD*	16	Loss of Cell Delineation indication. LCD transitions to a logic 1 when an out of cell delineation is found.

Headers J11, J10, J7, J14 (pages 3, 4, 5, 6 of schematics)

Headers J11, J10, J7, J14 are 20 pin headers. These headers are described together because they serve identical functions for each S/UNI-PDH device. They are used to monitor PLCP as well as overhead stuff signals for the four S/UNI-PDH devices. They are also used to bring external PLCP and overhead stuff signals to each S/UNI-PDH device. These headers are also used to monitor LOF, OOF, TCELL, RCELL, TCA, and RCA for each S/UNI-PDH device. J11 services S/UNI-PDH device 1, J10 is for device 2, J7 is for device 3, and J14 is for device 4.The signals on the header are described in the next table. Note that each signal has an * at the end of its name. When refering to a specific signal on the header for a S/UNI-PDH device, just replace the * with the S/UNI-PDH device number (1 to 4).

Signal	PIN #	Description
XTOHCLK*	1	Buffered transmit overhead clock. XTOH*, XTOHINS*, are sampled on the rising edge of XTOHCLK*
XTOHFP*	2	Buffered transmit overhead frame position. XTOHFP* is updated on the falling edge of XTOHCLK*.
XTOHINS*	3	Buffered transmit overhead insertion. Controls insertion of overhead bit into XTOH* stream.
XTOH*	4	Buffered transmit overhead data. Contains overhead bits that are inserted into DS3, E3 transmit streams.
XTPOHCLK*	5	Buffered transmit PLCP overhead clock. XTPOH*, and XTPOHINS* are sampled on the rising edge of XTPOHCLK*.
XTPOHFP*	6	Buffered transmit PLCP overhead frame position. XTPOHFP* is updated on the falling edge of XTPOHCLK*.
XTPOHINS*	7	Buffered transmit PLCP overhead insertion. Controls insertion of PLCP overhead bits into XTPOH* stream.
XTPOH*	8	Buffered transmit PLCP overhead data. Contains PLCP overhead bits that are inserted into the transmit PLCP frame.
TCELL*	9	Transmit cell indication. TCELL* Pulses once for every ATM cell transmitted.
TCA*	10	Transmit cell available. TCA* is a logic 1 when the cell based transmit FIFO is empty. It is a logic 0 when the FIFO contains cells.
RCELL*	11	Receive cell indication. RCELL* pulses once for every ATM cell received.
RCA*	12	Receive cell available. RCA* is a logic 1 when the cell based received FIFO contains at least one cell. It is logic 0 when the FIFO is empty (or nearly empty).

LOF*	13	PLCP Loss of frame. LOF* is asserted to a logic 1 while the PLCP receiver is in a loss of frame state.
OOF*	14	PLCP Out of frame. OOF* is asserted to a logic 1 while the PLCP receiver is in a loss of frame state.
XRPOHFP*	15	Buffered receive PLCP overhead frame position. XRPOHFP* is updated on the falling edge of XRPOHCLK*.
XRPOHCLK*	16	Buffered receive PLCP overhead clock. XRPOHFP* and XRPOH* are updated on the falling edge of XRPOHCLK*.
XRPOH*	17	Buffered receive PLCP overhead data. Contains PLCP overhead bits that are extracted from the receive PLCP frame.
XROHFP*	18	Buffered receive overhead frame position. XROHFP* is updated on the falling edge of XROHCLK*.
XROHCLK*	19	Buffered receive overhead clock. XROH*, and XROHFP*, are updated on the falling edge of XROHCLK*
XROH*	20	Buffered receive overhead data. Contains overhead bits that are extracted from DS3, E3 receive streams.

Headers J16, J17, J19 (page 6 of schematics)

Headers J16, J17, J19 are 14 pin headers. These headers are used to put S/UNI-PDH device 4 into either normal ATM bus mode or ATM Loopback mode. A 14 row by 2 column jumper block is used to short across headers J16 and J19 for normal ATM bus mode. A jumper block is used to short headers J17 and J16 for ATM Loopback mode. The following table describes signals on J16. J16 signals connect directly to inputs on S/UNI-PDH device 4 TDAT bus side.

Signal	PIN #	Description
TFCLK4	1	ATM Transmit FIFO clock. Clock for transferring ATM parallel data into S/UNI-PDH devices 4.
RFCLK4	2	ATM Receive FIFO clock. Clock for transferring ATM parallel data out of S/UNI-PDH device 4.
TDAT4(0)	3	Parallel ATM transmit data bus bit 0.
TDAT4(1)	4	Parallel ATM transmit data bus bit 1.
TDAT4(2)	5	Parallel ATM transmit data bus bit 2.
TDAT4(3)	6	Parallel ATM transmit data bus bit 3.
TDAT4(4)	7	Parallel ATM transmit data bus bit 4.
TDAT4(5)	8	Parallel ATM transmit data bus bit 5.
TDAT4(6)	9	Parallel ATM transmit data bus bit 6.
TDAT4(7)	10	Parallel ATM transmit data bus bit 7.
TSOC4	11	Transmit start of cell. Marks start of cell on TDAT4 bus.
TXPRTY4	12	Transmit parity. Indicates parity on TDAT4 bus.
TWREN4B4	13	Transmit write enable. Used to enable write TDAT bus data to S/UNI-PDH device 4 only.
RRDEN4B4	14	Receive Read output enable. Enables read data onto RDAT bus for S/UNI-PDH device 4 only.

The following table describes signals on J17. J17 signals are connected to J16 inputs on S/UNI-PDH device 4 TDAT bus side in Loopback mode with shorting jumpers.

Signal	PIN #	Description
NC	1	Not connected. This pin is left open for external TFCLK source to be connected in Loopback mode.
NC	2	Not connected. This pin is left open for external source of RFCLK to be connected in Loopback mode.
RDAT(0)	3	Parallel ATM receive data bus bit 0. Connected to TDAT4(0) in Loopback mode.
RDAT(1)	4	Parallel ATM receive data bus bit 1. Connected to TDAT4(1) in Loopback mode.
RDAT(2)	5	Parallel ATM receive data bus bit 2. Connected to TDAT4(2) in Loopback mode.
RDAT(3)	6	Parallel ATM receive data bus bit 3. Connected to TDAT4(3) in Loopback mode.
RDAT(4)	7	Parallel ATM receive data bus bit 4. Connected to TDAT4(4) in Loopback mode.
RDAT(5)	8	Parallel ATM receive data bus bit 5. Connected to TDAT4(5) in Loopback mode.
RDAT(6)	9	Parallel ATM receive data bus bit 6. Connected to TDAT4(6) in Loopback mode.
RDAT(7)	10	Parallel ATM receive data bus bit 7. Connected to TDAT4(7) in Loopback mode.
RSOC	11	Receive start of cell. Marks start of cell on RDAT bus. This signal is connected to TSOC4 in Loopback mode.
RXPRTY	12	Receive parity. Indicates parity on RDAT bus. This signal is connected to TXPRTY4 in Loopback mode.
BRCA4	13	Inverted Receive Cell Available. Indicates when a cell is available for output on the RDAT bus. Connected to TWREN4B4 in Loopback mode.
BTCA4	14	Inverted Transmit Cell Available. Indicates when transmit cell FIFO is empty. Connected to RRDEN4B4 in Loopback mode.

The following table describes signals on J19. J19 signals are normally connected to J16 inputs on S/UNI-PDH device 4 TDAT bus side with shorting jumpers.

Signal	PIN #	Description
TFCLK	1	ATM Transmit FIFO clock. Clock for transferring ATM parallel data into S/UNI-PDH device 4 from SCI-PHY connector.
RFCLK	2	ATM Receive FIFO clock. Clock for transferring ATM parallel data out of S/UNI-PDH device 4 to SCI-PHY connector.
TDAT(0)	3	Parallel ATM transmit data bus bit 0 from SCI-PHY connector.
TDAT(1)	4	Parallel ATM transmit data bus bit 1 from SCI-PHY connector.
TDAT(2)	5	Parallel ATM transmit data bus bit 2 from SCI-PHY connector.
TDAT(3)	6	Parallel ATM transmit data bus bit 3 from SCI-PHY connector.
TDAT(4)	7	Parallel ATM transmit data bus bit 4 from SCI-PHY connector.
TDAT(5)	8	Parallel ATM transmit data bus bit 5 from SCI-PHY connector.
TDAT(6)	9	Parallel ATM transmit data bus bit 6 from SCI-PHY connector.
TDAT(7)	10	Parallel ATM transmit data bus bit 7 from SCI-PHY connector.
TSOC	11	Transmit start of cell. Marks start of cell on TDAT bus.
TXPRTY	12	Transmit parity. Indicates parity on TDAT bus from SCI-PHY connector.
TWREN4B	13	Transmit write enable. Used to enable a write of TDAT bus data to S/UNI-PDH device 4 from SCI-PHY connector.
RRDEN4B	14	Receive Read output enable. Enables a read of data onto RDAT bus on the SCI-PHY connector from S/UNI-PDH device 4.

Headers J21 (page 7 of schematics)

Headers J21 is a 17 pin header. This header is a used to test and monitor signals connected to the PM4341 T1XC T1 framer transceiver. The following table describes signals on J21.

Signal	PIN #	Description
GND	1	Ground
T1BRFPI	2	Backplane frame pulse input. This signal is used to frame align the received data to the system backplane. It is pulled up with 10 kohms.
T1BRCLK	3	Backplane Receive clock. This input can be fed with a 1.544 MHz clock. It is pulled up with 10 kohms.
T1RDLCLK	4	Receive data link clock. This output is the clock for the HDLC receiver T1RDLSIG signal.
T1RDLSIG	5	Receive data link signal. This output is the HDLC receiver data signal.
T1RDN	6	Receive Digital Negative Line Pulse. This input can receive the negative phase NRZ or RZ line receive data stream. It is pulled up with 10 kohms.
T1RDP	7	Receive Digital Positive Line Pulse. This input can receive the positive phase NRZ or RZ line receive data stream. It is pulled up with 10 kohms.
T1BRSIG	8	Backplane Receive Signalling. The T1BRSIG output contains extracted signalling bits for each channel in the receive frame.
T1BRPCM	9	Backplane Receive PCM. This output contains the recovered receive line data stream.
T1BRFPO	10	Backplane Frame Pulse Output. This output indicates the frame alignment of the T1BRPCM data stream.
T1RCLKI	11	Receive Line Clock Input. This input can be an externally recovered 1.544 MHz clock used to sample the T1RDP and T1RDN inputs. It is pulled up with 10 kohms.
T1TDLSIG	12	Transmit Data Link Signal. HDLC transmit data is input to this pin to be inserted in the line transmit stream. It is pulled up with 10 kohms.
T1TDLCLK	13	Transmit Data Link Clock. This input provides clocking for the T1TDLSIG signal.
T1TDN	14	Transmit Digital Negative Line Pulse. This output represents the negative phase line transmit data stream with RZ or NRZ CMOS levels.
T1TDP	15	Transmit Digital Positive Line Pulse. This output represents the positive phase line transmit data stream with RZ or NRZ CMOS levels.

T1TCLKO	16	Transmit Clock Output. The T1TDP, and T1TDN outputs can be clocked on the rising or falling edge of T1TCLKO.
T1TCLKI	17	Transmit Clock Input.This input can be used to generate the TCLKO signal. It is pulled up with 10 kohms.

Headers J15 (page 8 of schematics)

Headers J15 is a 17 pin header. This header is a used to test and monitor signals connected to the PM6341 E1XC E1 framer transceiver. The following table describes signals on J15.

Signal	PIN #	Description
GND	1	Ground
E1BRFPI	2	Backplane Frame Pulse Input. This signal is used to frame align the received data to the system backplane. It is pulled up with 10 kohms.
E1BRCLK	3	Backplane Receive Clock. This input can be fed with a 2.048 MHz clock. It is pulled up with 10 kohms.
RFP	4	Receive Frame Pulse. This output indicates frame alignment of the RDPCM data stream.
E1RDLCLK	5	Receive Data Link Clock. This is the output clock for the HDLC receiver E1RDLSIG signal.
E1RDLSIG	6	Receive Data Link Signal. This is the HDLC receiver data signal output.
RDPCM_RPCM	7	Recovered Decoded PCM. This output is the recovered receive PCM data stream.
E1RDN	8	Receive Digital Negative Line Pulse. This input can receive the negative phase NRZ or RZ line receive data stream. It is pulled up with 10 kohms.
E1RDP	9	Receive Digital Positive Line Pulse. This input can receive the positive phase NRZ or RZ line receive data stream. It is pulled up with 10 kohms.
E1BRSIG	10	Backplane Receive Signalling. The E1BRSIG output contains extracted signalling bits for each channel in the receive frame.
E1RCLKI	11	Receive Line Clock Input. This input could be an externally recovered 2.048 MHz clock used to sample the E1RDP and E1RDN inputs. It is pulled up with 10 kohms.
E1TDLSIG	12	Transmit Data Link Signal. HDLC transmit data is input to this pin to be inserted in the line transmit stream. It is pulled up with 10 kohms.
E1TDLCLK	13	Transmit Data Link Clock. This input provides clocking for the E1TDLSIG signal.
E1TDN	14	Transmit Digital Negative Line Pulse. This output represents the negative phase line transmit data stream with RZ or NRZ CMOS levels.

E1TDP	15	Transmit Digital Positive Line Pulse. This output represents the positive phase line transmit data stream with RZ or NRZ CMOS levels.
E1TCLKO	16	Transmit Clock Output. The E1TDP, and E1TDN outputs can be clocked on the rising or falling edge of E1TCLKO.
E1TCLKI	17	Transmit Clock Input.This input can be used to generate the TCLKO signal. It is pulled up with 10 kohms.

Power Connector

A supply of +5V and ground is normally provided by the SCI-PHY EVBD via the 96 pin DIN connectors when the SCI-PHY EVBD is attached to the S/UNI-PDH EVBD. When the S/UNI-PDH EVBD is used in Loopback mode, a 2 position barrier strip power connector, J25 (on schematic page 10), is provided to supply +5V and ground to the board. The +5V connection is fused with a 3 Amp quick blow fuse (F1). J25 connections are listed in the next table.

Signal	PIN #	Description
GND	1	Ground
+5V	2	Power

OPERATION

The S/UNI-PDH EVBD has been designed to work with the SCI-PHY evaluation mother board, or in a Loopback mode with reduced functionality.

Operation with SCI-PHY Motherboard

During operation with the SCI-PHY mother board, TDAT[7:0], RDAT[7:0], the control lines, and clocks come from the SCI-PHY 96 pin DIN connector. Microprocessor control and data bus signals are provided from the SCI-PHY motherboard via the Microprocessor Interface 96 pin DIN connector. Each S/UNI-PDH device on the S/UNI-PDH EVBD has an independent line interface but all S/UNI-PDH devices are common to the ATM parallel data buses. Since all four S/UNI-PDH devices are common to the ATM parallel data buses, access to a particular S/UNI-PDH device is controlled by read and write enable signals emanating from the SCI-PHY motherboard. This is done under control by the microprocessor on the SCI-PHY motherboard. In order that the S/UNI-PDH EVBD operates properly in its normal operating mode, headers J16 and J19 must have their adjacent pins jumpered together with a 2 row by 14 column shorting jumper block.

Operation in Loopback Mode

The S/UNI-PDH EVBD can be operated in a Loopback mode with reduced functionality. Only S/UNI-PDH device 4, which is configured for operation at the E3 line rate, can be operated in Loopback mode. The rest of the S/UNI-PDH devices will not be able to function during Loopback mode. In Loopback mode the receive parallel RDAT ATM data bus is looped back to the transmit parallel TDAT4 bus input on S/UNI-PDH device 4. RSOC is looped back to TSOC4. RXPRTY is looped back to TXPRTY4. RCA4 is inverted and looped back to TWREN4B4. TCA4 is inverted and looped back to RRDEN4B4.

To put the S/UNI-PDH board into Loopback mode one must jumper together adjacent pins on headers J16 and J17 (page 6 on schematics) with a 2 row by 14 column shorting jumper block. Off board clock sources for TFCLK4 and RFCLK4 must be provided on pins 1 and 2 of header J17 for Loopback mode to work on S/UNI-PDH device 4. If the SCI-PHY motherboard is not mated with the S/UNI-PDH EVBD, Pins 1 and 2, 3 and 4, 5 and 6 on header J4 (page 2 on schematics) must be shorted with 2 position shorting jumpers to prevent floating CMOS inputs on the rest of the S/UNI-PDH devices on the board.

ELECTRICAL SPECIFICATIONS

SCI-PHY ATM and Microprocessor Interface

Both the SCI-PHY ATM and Microprocessor interfaces use 96 pin DIN plug connectors. These interfaces provide support for the ATM drop side as well as the microprocessor interface. See SATURN COMPLIANT INTERFACE FOR ATM PHYSICAL LAYER INTERCONNECT EVALUATION MOTHERBOARD ENGINEERING DOCUMENT for further details on this interface.

CMOS level voltages are used by all signals on these connectors.

Line Interface Signals

The transmit and receive line interface signals are transformer isolated. The termination impedance and connector type for each signal is given in the following table.

Signal+	Signal-	Impedance	Connector	Description
TXDS1P	TXDS1N	100 ohm	Bantam	DS1 balanced TX outputs.
RXDS1P	RXDS1N	100 ohm	Bantam	DS1 balanced RX inputs.
TXE1P	TXE1N	120 ohm	Bantam	E1 balanced TX outputs.
RXE1P	RXE1N	120 ohm	Bantam	E1 balanced RX inputs.
TXDS3P	TXDS3N	75 ohm	BNC Coax	DS3 unbalanced TX outputs.
RXDS3N	RXDS3N	75 ohm	BNC Coax	DS3 unbalanced RX inputs.
TXE3P	TXE3N	75 ohm	BNC Coax	E3 unbalanced TX outputs.
RXE3P	RXE3N	75 ohm	BNC Coax	E3 unbalanced RX inputs.

S/UNI-PDH EVBD Power

The S/UNI-PDH EVBD requires a single supply of +5 Volts D.C. at x.xx Amps. This can be provided through several pins on the Microprocessor interface 96 pin DIN connector, or, by J25, a two position barrier strip connector. The +5V supply via pin 1 on J25 is fused for 3 Amps, quick blow. The S/UNI-PDH EVBD draws its power from the SCI-PHY EVMB when attached to it. Fusing in this case is provided on the SCI-PHY board.

STOCK LIST

Item	Part	Description	Reference	Qty
1	PDH	PM7345 S/UNI-PDH	U1,U7,U9,U12	4
2	PM4341	PM4341 T1XC	U20	1
3	PM6341	PM6341 E1XC	U21	1
4	78P7200	78P7200 PLCC 28 pin	U18,U19	2
5	PE64952	Transformers PE64952	T1,T2	2
6	PE65663	Transformer PE65663	T3	1
7	OSC	Oscillator 49.152 MHz Osc TTL	Y2	1
8	OSC	Oscillator 44.736 MHz Osc TTL	Y5	1
9	OSC	Oscillator 37.056 MHz Osc TTL	Y1	1
10	OSC	Oscillator 34.368 MHz Osc TTL	Y6	1
11	OSC	Oscillator 2.048 MHz Osc TTL	Y4	1
12	OSC	Oscillator 1.544 MHz TTL	Y3	1
13	74HCT541	74HCT541	U2,U3,U4,U5,U6, U8,U10,U11	8
14	HDR5X2	Header - Dual row breakable header strip, tin plate, male, 0.1" spacing, 50 contacts total, INDUS 923866 - CUT INTO LENGTHS OF 5 CONTACT PAIRS EACH.	J4	1
15	HDR8X2	Header - Dual row breakable header strip, tin plate, male, 0.1" spacing, 50 contacts total, INDUS 923866 - CUT INTO LENGTHS OF 8 CONTACT PAIRS EACH	J9,J12,J13,J20	4
16	HDR14	Header - Single row breakable header strip, tin plate, male, 0.1" spacing, 36 contacts total INDUS 929647-01-36 - CUT INTO LENGTHS OF 14 contacts each	J16,J17,J19	3

17	HDR17	Header - Single row breakable header strip, tin plate, male, 0.1" spacing, 36 contacts total, INDUS 929647-01-36 - CUT INTO LENGTHS OF 17 CONTACTS EACH	J15,J21	2
18	HDR20	Header - Single row breakable header strip, tin plate, male, 0.1" spacing, 36 contacts total, INDUS 929647-01-36 - CUT INTO LENGTHS OF 20 CONTACTS EACH.	J7,J10,J11,J14	4
19	RSIP9	resistor 10 pin 9 resistor 4.7K ohms 5% (4.7kx9+1)	RN1,RN2,RN3	3
20	RESISTOR	resistor 75 ohm 1%	R28,R53,R54	3
21	RESISTOR	resistor 422 ohm 1%	R51	1
22	RESISTOR	resistor 5.23Kohm 1%	R40	1
23	RESISTOR	resistor 6.81Kohm 1%	R37	1
24	RESISTOR	resistor 301 ohm 1%	R50	1
25	RESISTOR	resistor 604 ohm 1%	R52	1
26	RESISTOR	resistor 6.04 Kohm 1%	R35,R45	2
27	RESISTOR	resistor 100 Kohm 1%	R41,R48	2
28	RESISTOR	resistor 316 Kohm 1%	R21,R27	2
29	RESISTOR	resistor 1.1 Kohm 1%	R2,R5	2
30	RESISTOR	resistor 1 ohm 1%	R6,R22,R23,R31, R38,R42,R44, R46,R55,R56	10
31	RESISTOR	resistor 9.09 K ohm 1%	R16	1
32	RESISTOR	resistor 412 ohm 1%	R20	1
33	CAPACITOR	cap 22 pF ceramic Cog	C32	1
34	CAPACITOR	cap 10 pF ceramic "100" NPO	C23,C97	2
35	CAPACITOR	cap 2.7 pF ceramic 50V	C20,C98	2
36	CAPACITOR	cap 0.22 microFarad elec. tant.	C18,C22	2
37	CAPACITOR	cap 0.022 microFarad ceramic "223" X7R	C19,C30	2
38	CAPACITOR	cap 10 microFarad elec. 10V	C46,C99	2
39	CAPACITOR	cap 0.047 microFarad ceramic "473" X7R	C15,C17	2

40	CAPACITOR	cap 0.1 microFarad ceramic "104" X7R	C1,C3-C8,C12, C13,C16,C25-C29,C31,C33-C45,C47-C96	79
41	CAPACITOR	cap 0.01 microFarad ceramic	C24	1
42		PCB 4 layer, one +5V plane, one GND plane,two signal planes,		1
43	DIN96	R/A PCB connector 3x32 pins	J1,J2	2
44	BANTAM	Bantam PCB Jack + cover (PC834)	J18,J22,J23,J24	4
45	BNC	BNC PCB R/A mount 75 ohm	J3,J5,J6,J8	4
46	INDUCTOR	Inductor 4.7 microHenry	L1,L2,L3,L4,L6, L7,L8,L9	8
47	INDUCTOR	Inductor 0.47 microHenry	L5	1
48	LED	LED Green	D5	1
49	LED	LED Red	D1,D2,D3,D4	4
50	RESISTOR	resistor 330 ohm 1/4W 5%	R9,R15,R24,R32, R57	5
51	22V10PLCC	PAL 22V10 -25	U13,U15,U16, U17	4
52	74F04BLK	74F04 SOIC	U14	1
53	PE65664	Transformers PE65664	T4,T5,T6	3
54	RESISTOR	resistor 120 ohm 5%	R26,R30,R34, R49	4
55	RESISTOR	resistor 22.1 ohm 1%	R47	1
56	RESISTOR	resistor 47 ohm 5%	R39	1
57	RESISTOR	resistor 4.53 kohm 1%	R7	1
58	RESISTOR	resistor 4.7 kohm 5%	R3,R4,R8,R10, R11,R12,R13, R14,R17,R18, R19,R25,R29, R33,R36,R43	16
59	RESISTOR	resistor 523 ohm 1%	R1	1

60	CAPACITOR	cap 0.001 µF ceramic "101" NPO	C2,C11	2
61	CAPACITOR	cap 0.47 µF elec. tant. surface mount	C9,C10	2
62	CAPACITOR	cap 0.68 µF ceramic monolithic X7R thru hole	C14,C21	2
63	RSIP9	resistor 10 pin 9 resistor10K ohms 5% (4.7kx9+1)	RN4,RN5	2
64	POWER2	PW 2 Power Connector - Barrier Strip 2 pos. PC mount	J25	1
65	FUSE	Fuse - 3A - PICO II Very Fast Acting Pico Fuse	F1	1
66		Socket-PLCC-28 pin surface mount		6
67		Adhesive Mount Rubber Feet		4
68		Spacer 4-40 nylon hex 1/4'	H1	
69		Screw 4-40 1/4 nylon	H2	
70	CAPACITOR	Cap 3.3pF ceramic chip	possible substitute for C20, C98	

REFERENCES

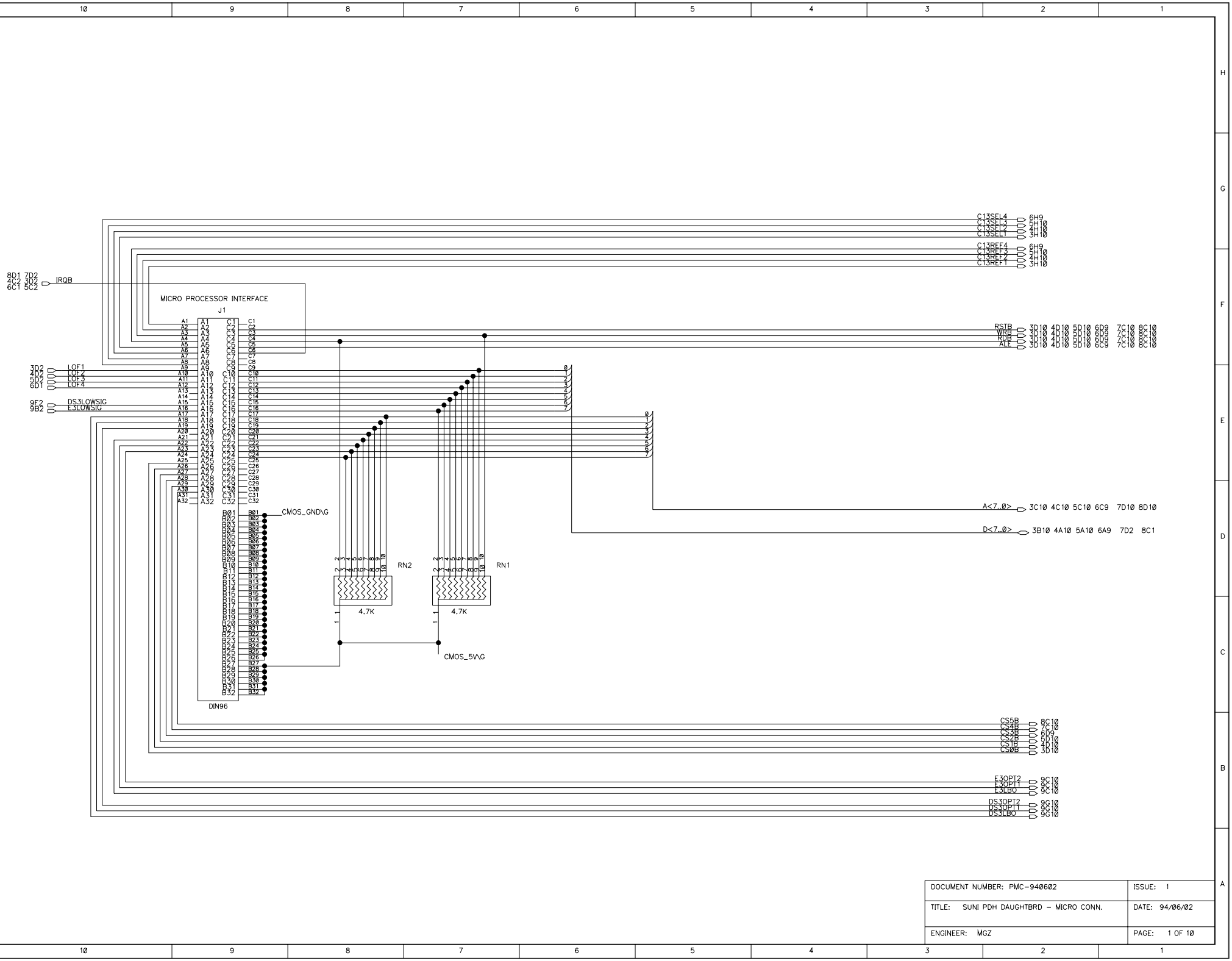
- PMC-940212, ATM_SCI_PHY, "SATURN COMPLIANT INTERFACE FOR ATM DEVICES", February 1994, Issue 1
- PMC-940324, SATURN COMPLIANT INTERFACE FOR ATM PHYSICAL LAYER INTERCONNECT EVALUATION MOTHERBOARD (SCI-PHY EVMB) ENGINEERING DOCUMENT.
- PMC-931011, "SATURN USER-NETWORK INTERFACE FOR ATM PLESIOCHRONOUS DIGITAL HIERARCHY", April 1994
- PM4341A T1XC DATABOOK, "T1 FRAMER TRANSCEIVER".
- PM6341A E1XC DATABOOK, "E1 FRAMER TRANSCEIVER".
- 78P7200 LIU DATASHEET, "COMMUNICATION PRODUCTS DATABOOK", SILICON SYSTEMS, 1994.

APPENDIX 1: COMPONENT PLACEMENT DIAGRAM

APPENDIX 2: SUGGESTED REVISIONS

1) The placement of J16 and J17 should be swapped.

APPENDIX 3: SCHEMATICS



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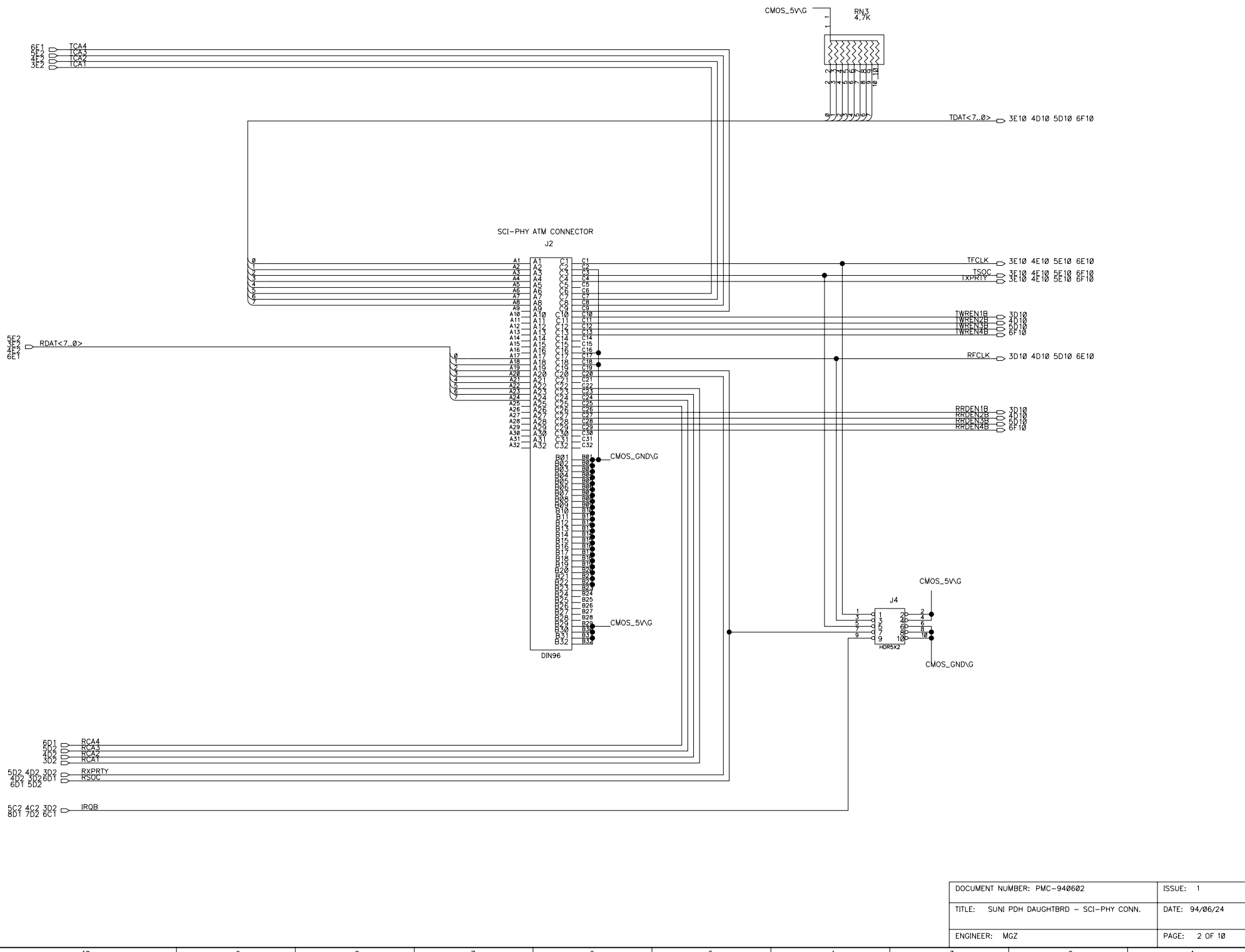

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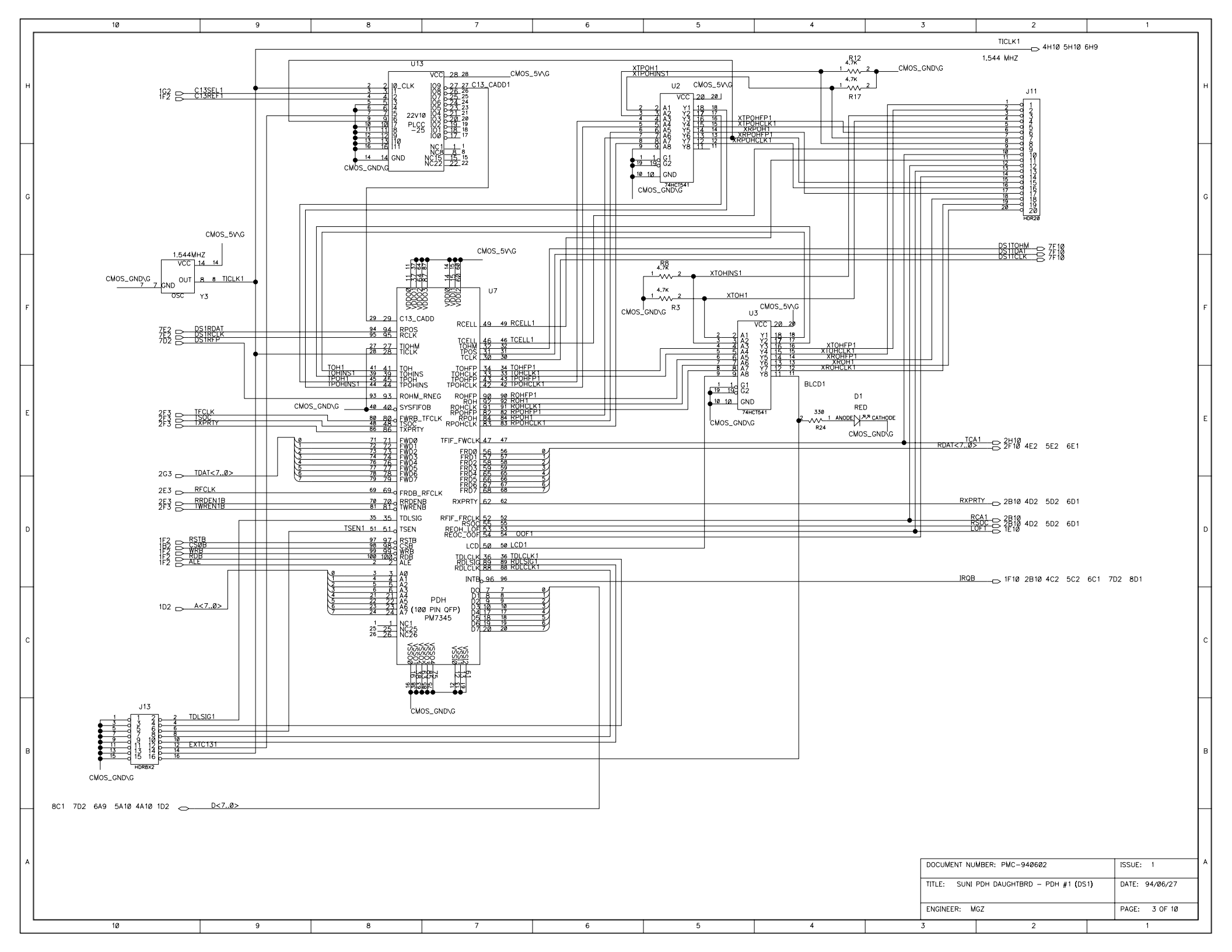

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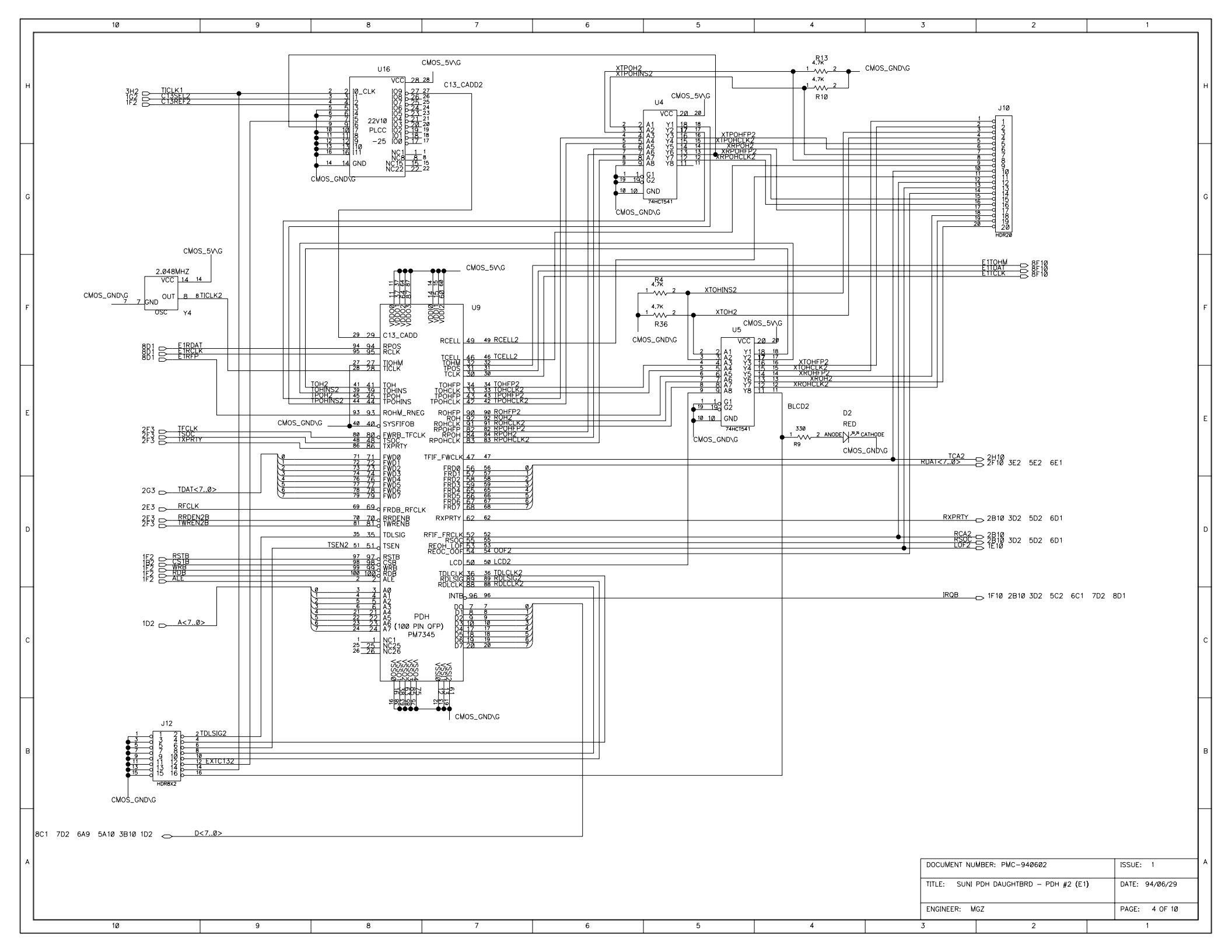

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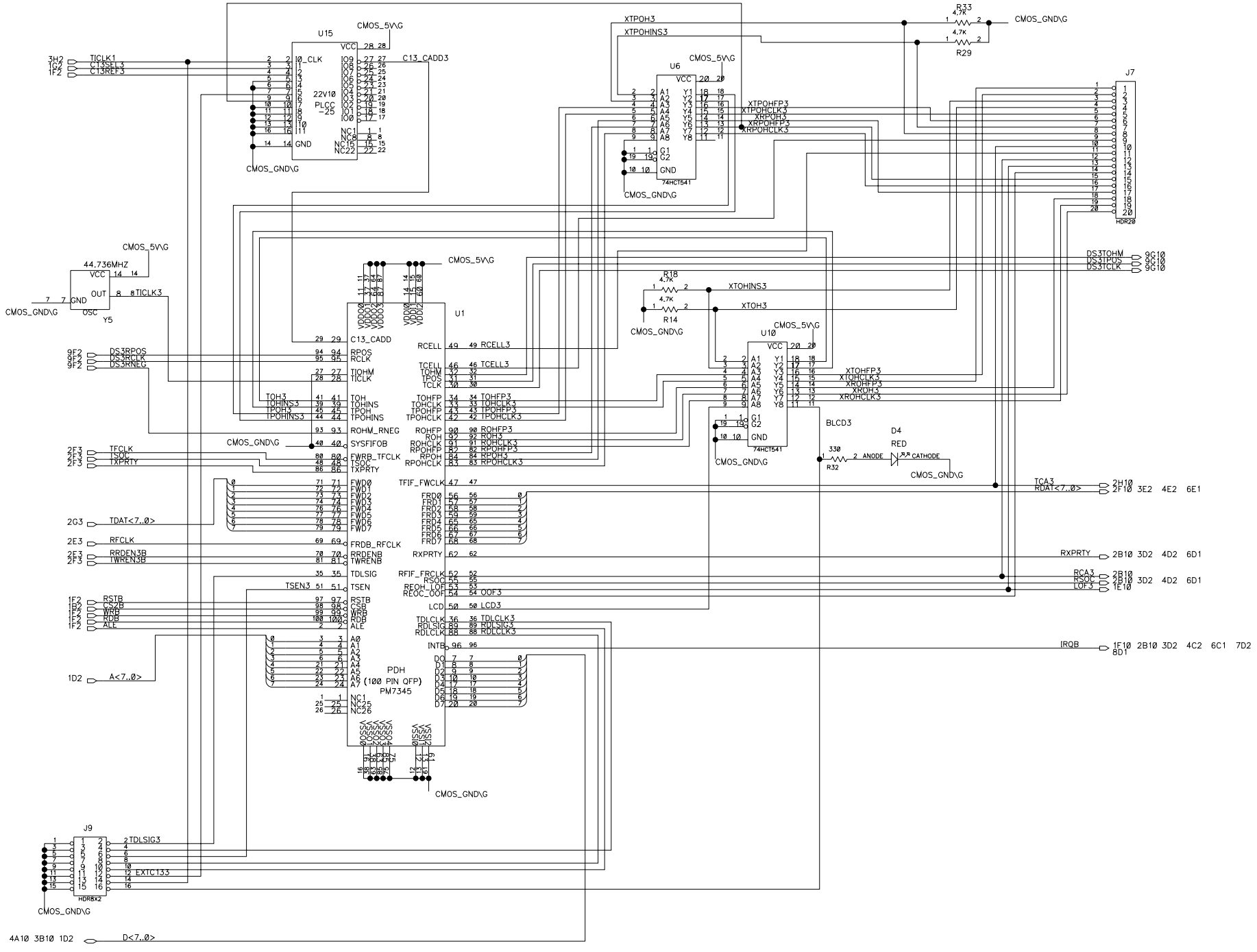
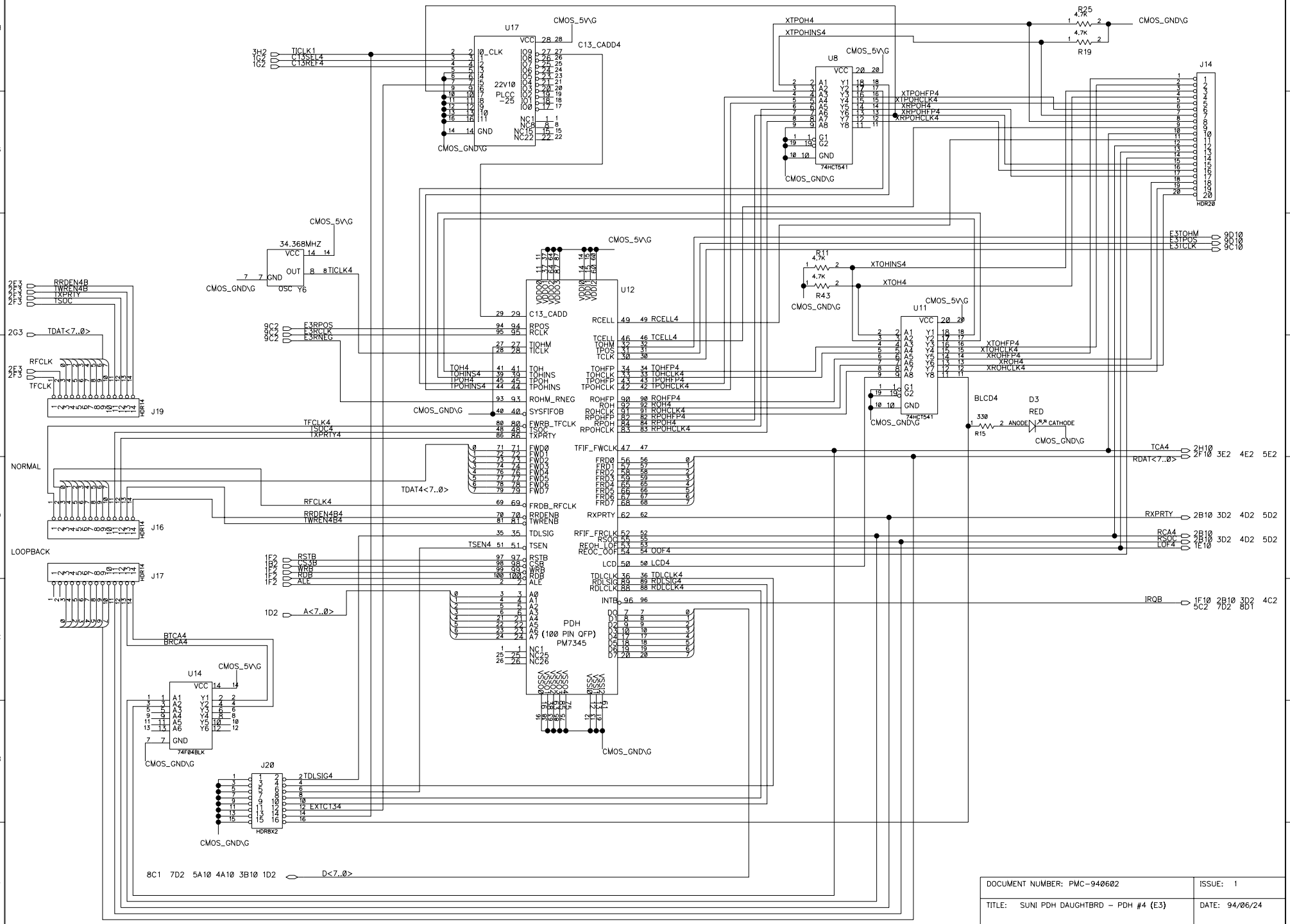
TITLE: SUNI PDH DAUGHTBRD - PDH #2 (E1)	DATE: 94/06/29
ENGINEER: MGZ	PAGE: 4 OF 10



DOCUMENT NUMBER: PMC-940602	ISSUE: 1
TITLE: SUNI PDH DAUGHTBRD - PDH #3 (DS3)	DATE: 94/06/27
ENGINEER: MGZ	PAGE: 5 OF 10


U17
U12
U11
U8
U14
J14
J19
J16
J17
J20
J18
PDH
PM7345
(100 PIN QFP)
74HCT541
74F84BLK
HDR20
HDR14
HDR8X2
CMOS_5V\G
CMOS_GND\G
34.368MHZ
TICLK1
C13SEL4
C13REF4
C13_CADD4
XTPOH4
XTPOHINS4
XTPOHFP4
XTPOHCLK4
XRPOH4
XRPOHFP4
XRPOHCLK4
R25
R19
R11
R43
R15
BLCD4
D3
RED
ANODE
CATHODE
E3TOHM
E3TPOS
E3TCLK
RRDEN4B
TWREN4B
TXPRTY
TSOC
TDAT<7..0>
RFCLK
TFCLK
NORMAL
LOOPBACK
E3RPOS
E3RCLK
E3RNEG
TFCLK4
TSOC4
TXPRTY4
RFCLK4
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TDAT4<7..0>
A<7..0>
D<7..0>
BTCA4
BRCA4
TCA4
RDAT<7..0>
RXPRTY
RCA4
RSOC
LOF4
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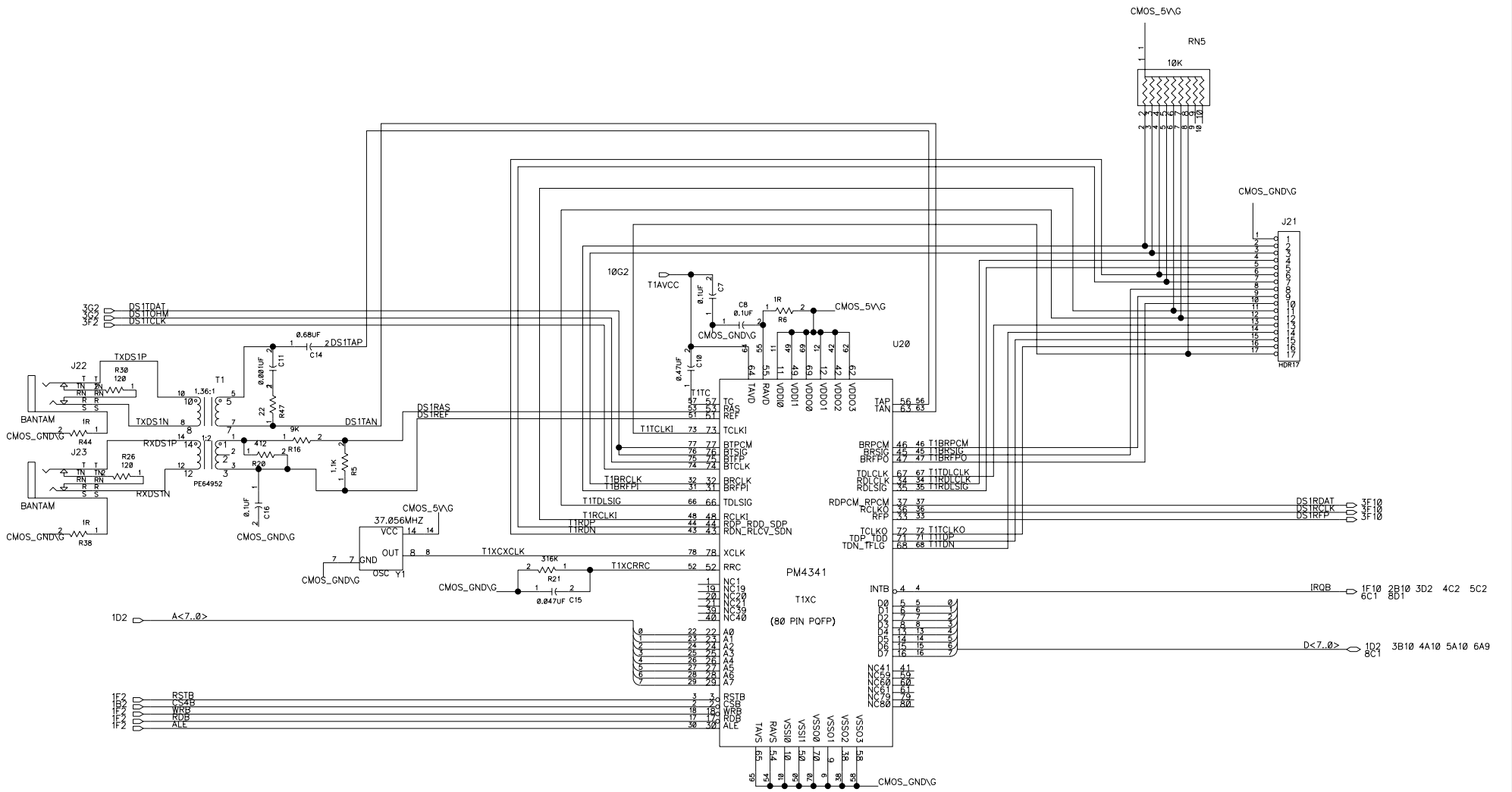
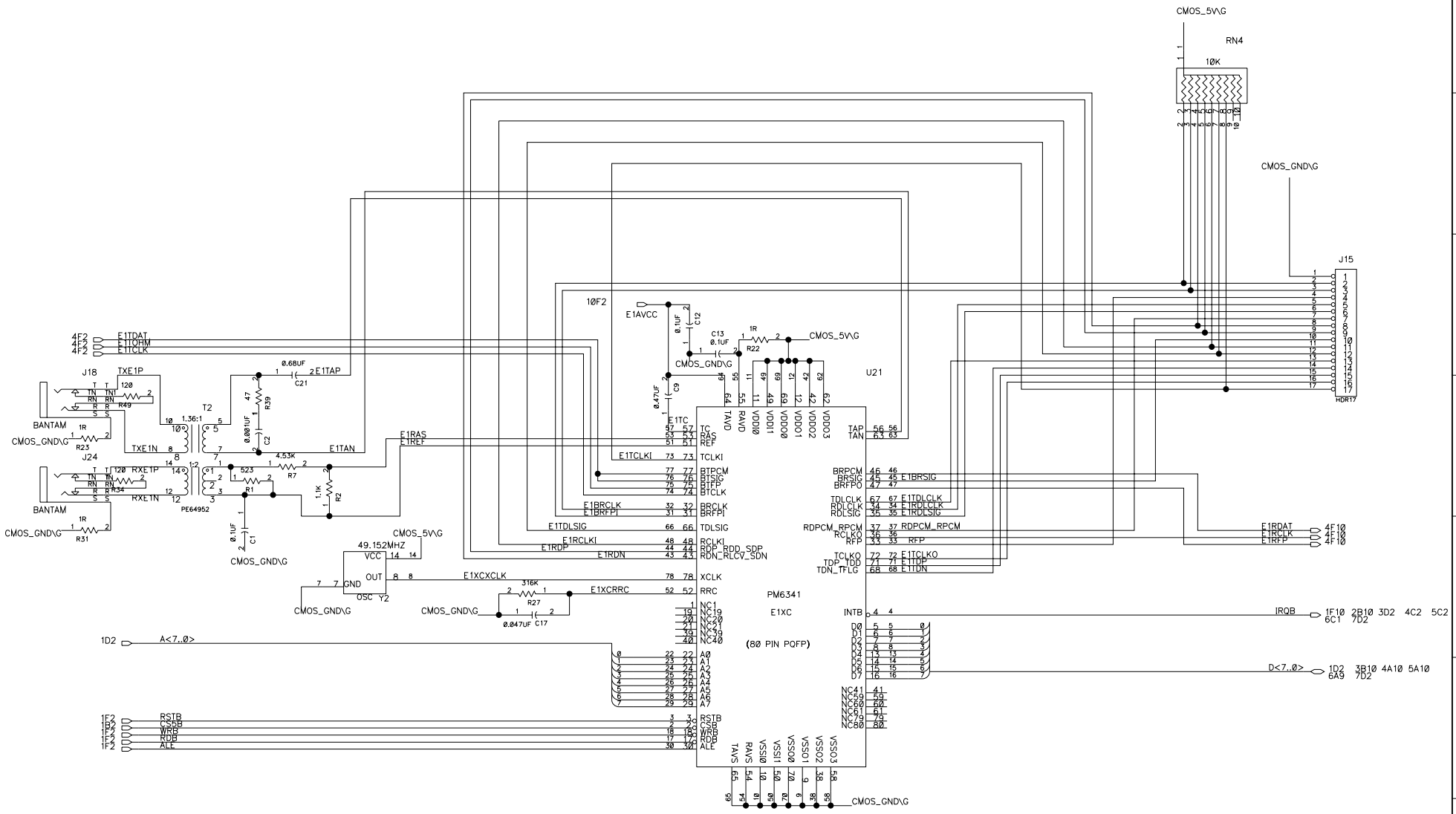
WRB
RDB
ALE
LCD4
TDLSIG4
EXTC134
8C1 7D2 5A10 4A10 3B10 1D2
DOCUMENT NUMBER: PMC-940602
ISSUE: 1
TITLE: SUNI PDH DAUGHTBRD - PDH #4 (E3)
DATE: 94/06/24
ENGINEER: MGZ
PAGE: 6 OF 10



DOCUMENT NUMBER: PMC-940602	ISSUE: 1
TITLE: SUNI PDH DAUGHTBRD - T1XC	DATE: 94/06/29
ENGINEER: MGZ	PAGE: 7 OF 10



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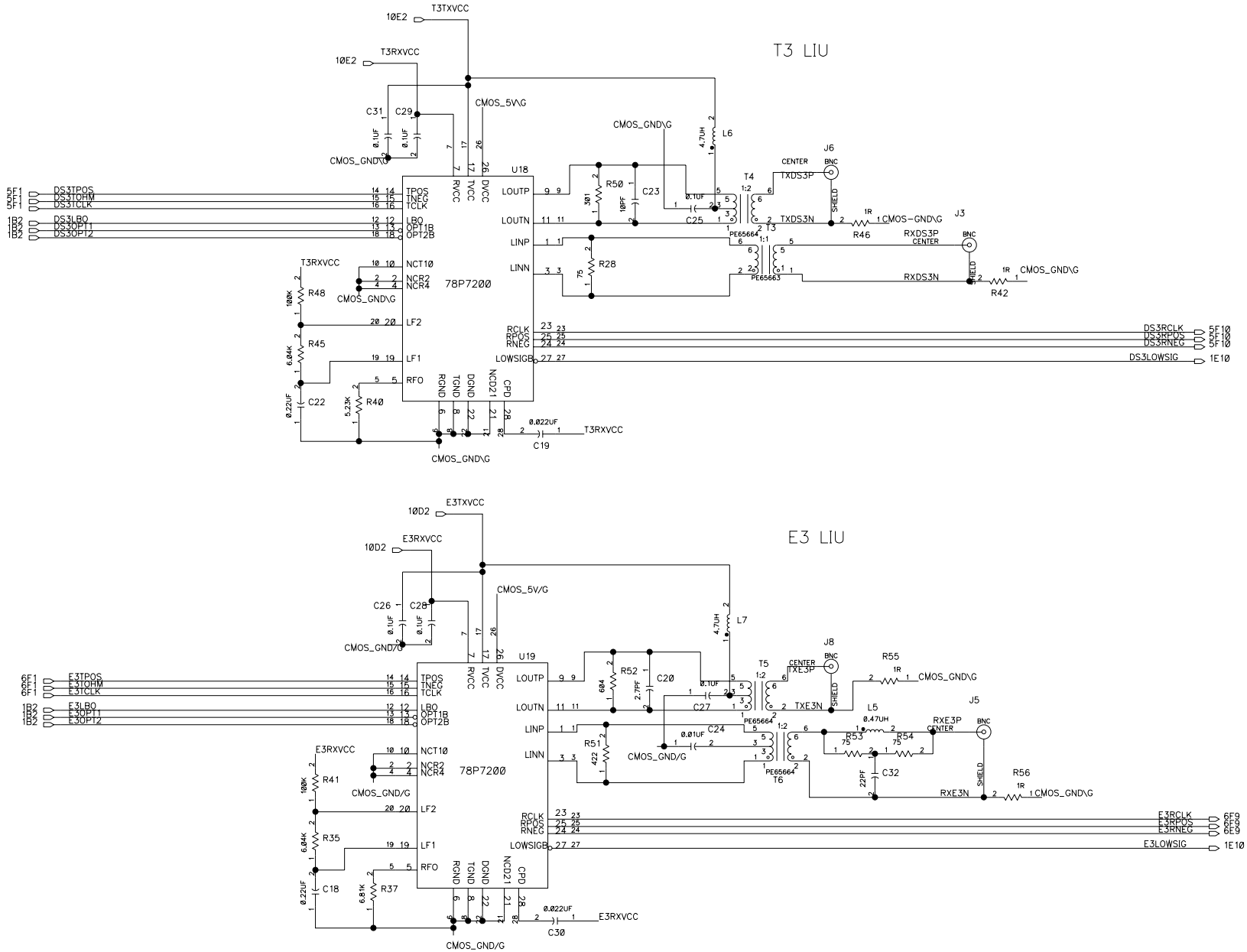
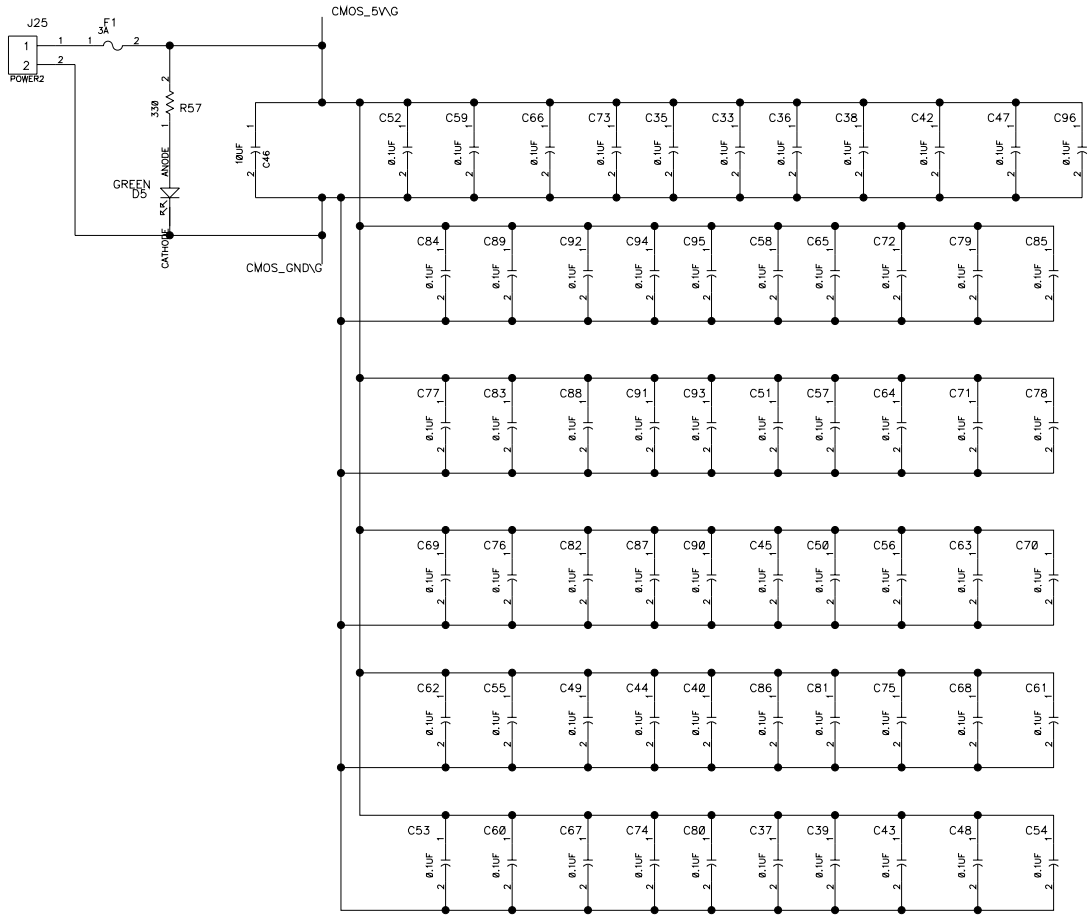
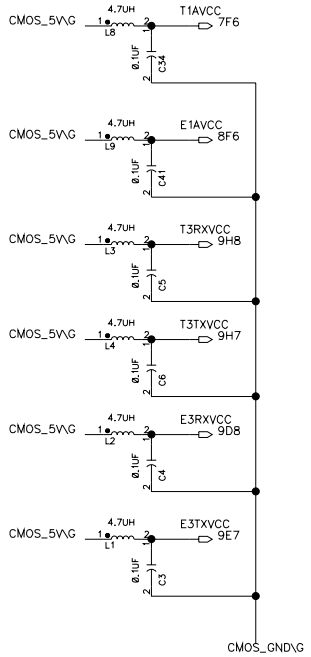
TITLE: SUNI PDH DAUGHTBRD – E1XC	DATE: 94/06/29
ENGINEER: MGZ	PAGE: 8 OF 10



DOCUMENT NUMBER: PMC-940602	ISSUE: 1
TITLE: SUNI PDH DAUGHTBRD - T3 AND E3	DATE: 94/06/27
ENGINEER: MGZ	PAGE: 9 OF 10



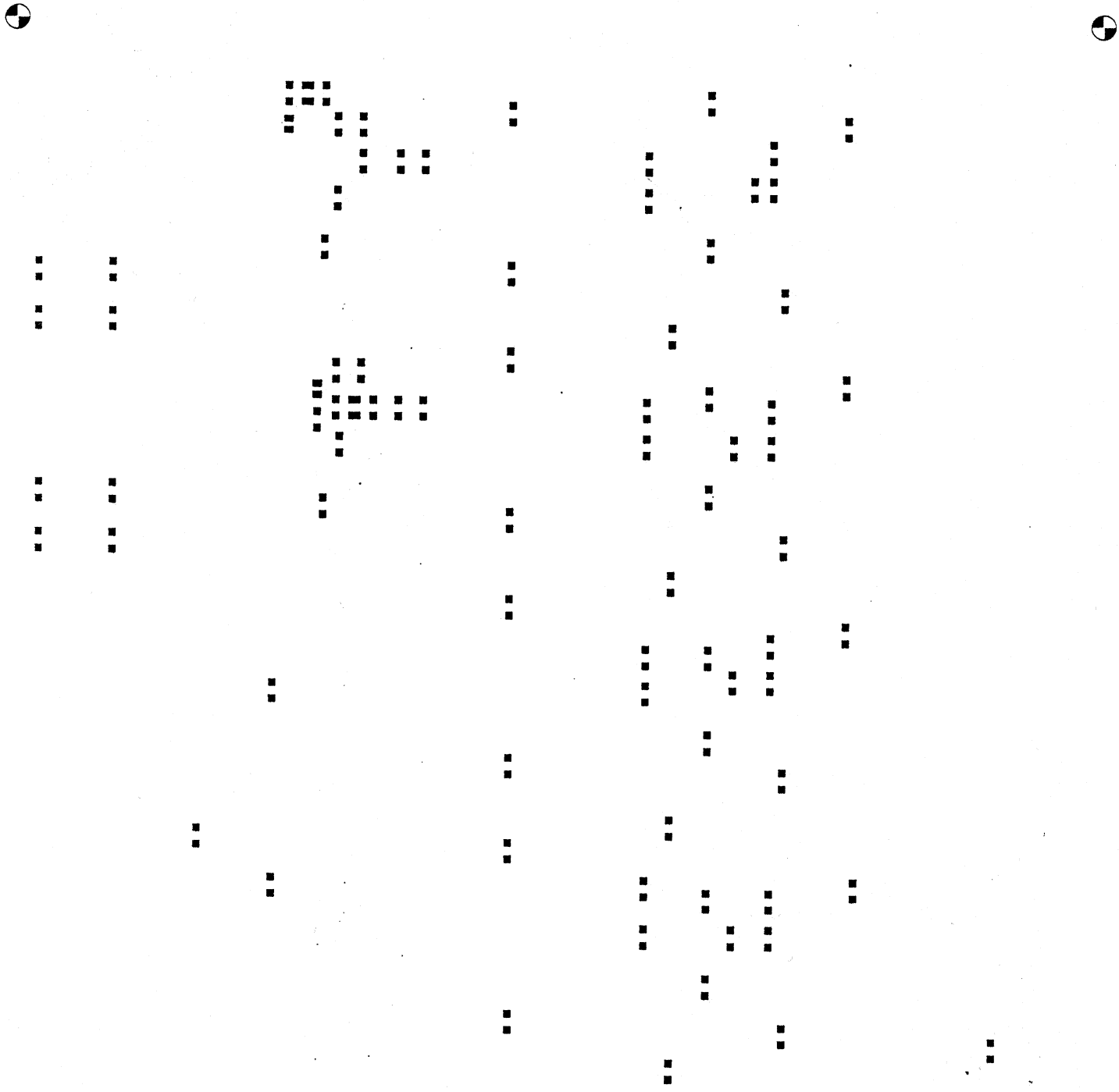


DOCUMENT NUMBER: PMC-940602	ISSUE: 1
TITLE: SUNI PDH DAUGHTBRD - PWR / DECOUP	DATE: 94/06/29
ENGINEER: MGZ	PAGE: 10 OF 10

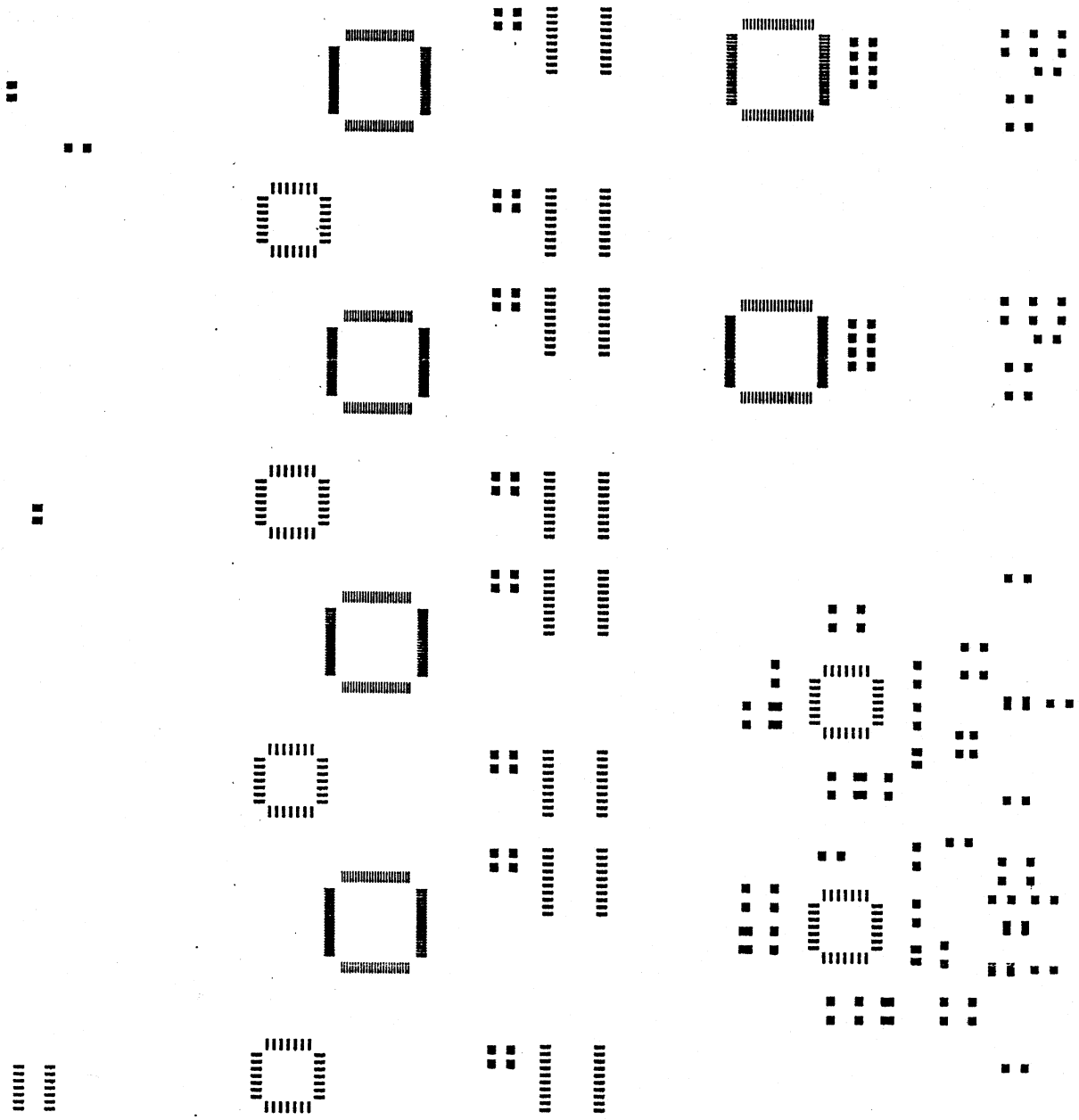
APPENDIX 4: EXAMPLE FORTH WORDS

TBD;

APPENDIX 5: EXAMPLE BOARD LAYOUT



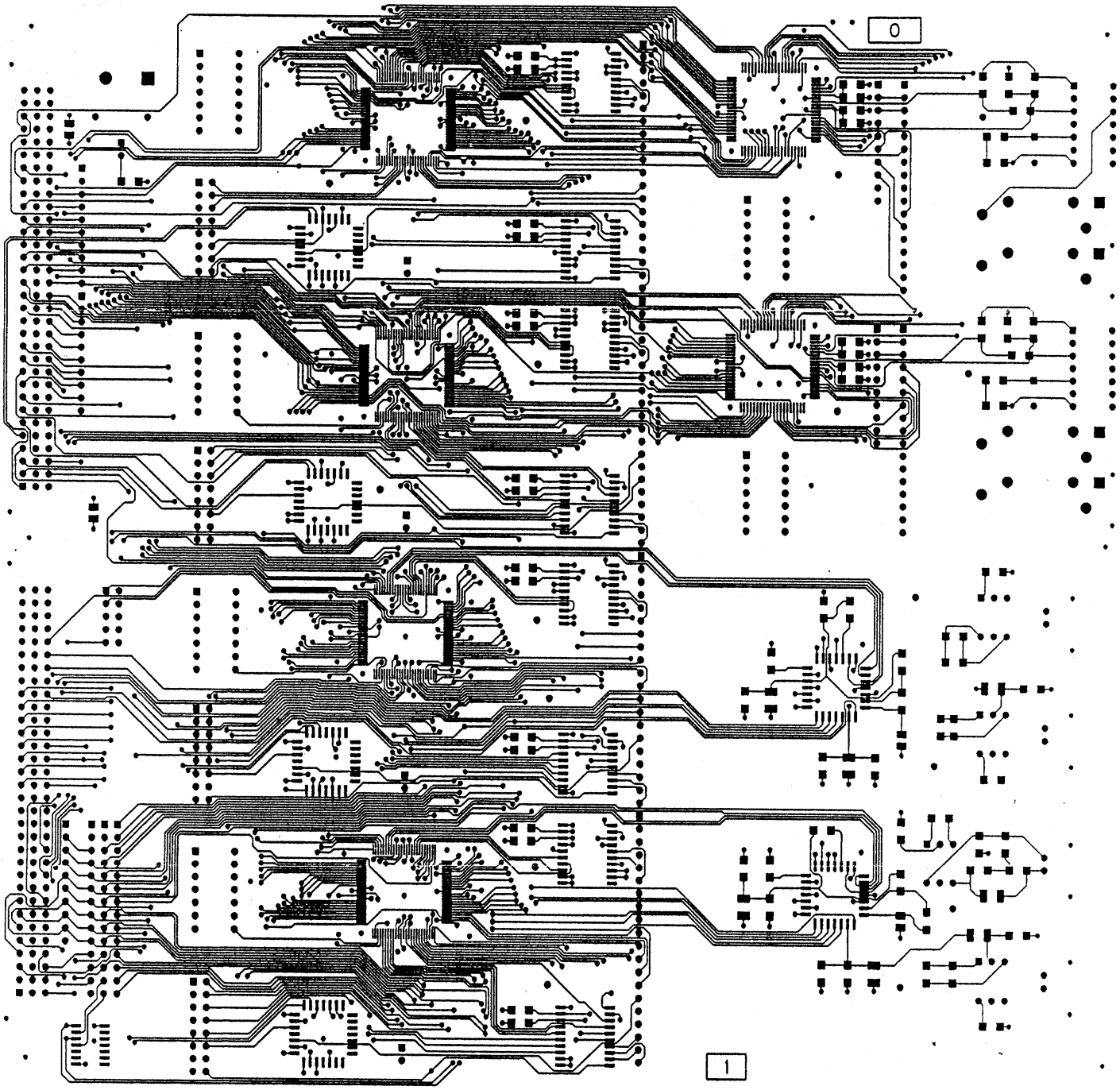
PMC SUNI-PDH EVALUATION BOARD
(PS) PASTE MASK (SOLDER SIDE) REV 0 94-07-15



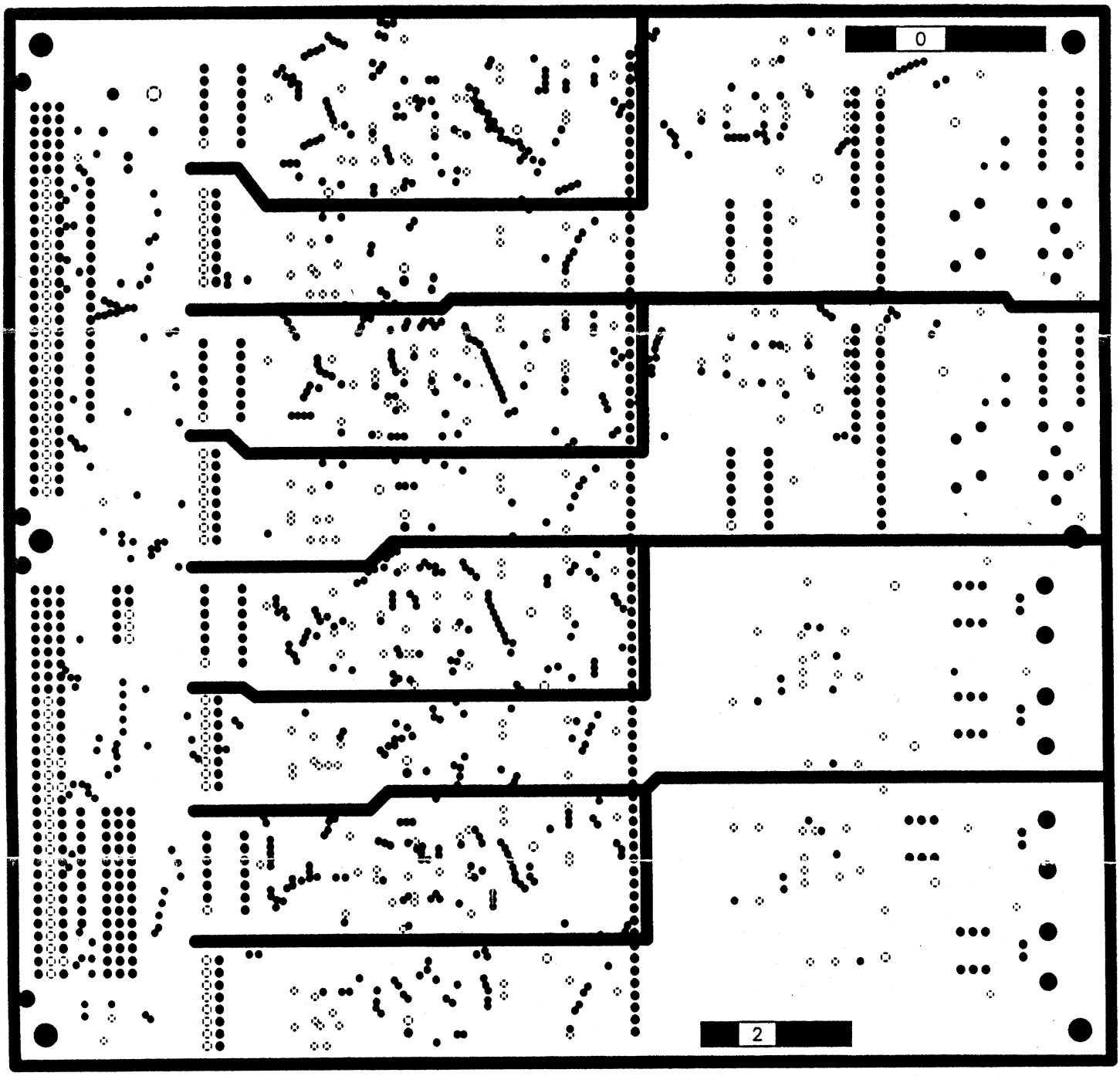
PMC SUNI-PDH EVALUATION BOARD
(PC) PASTE MASK (COMPONENT SIDE) REV 0 94-07-15

(cc) CMOS_SV PLANE REV 0 89-10-12
PMC SUNI-PDH EVALUATION BOARD
3
0

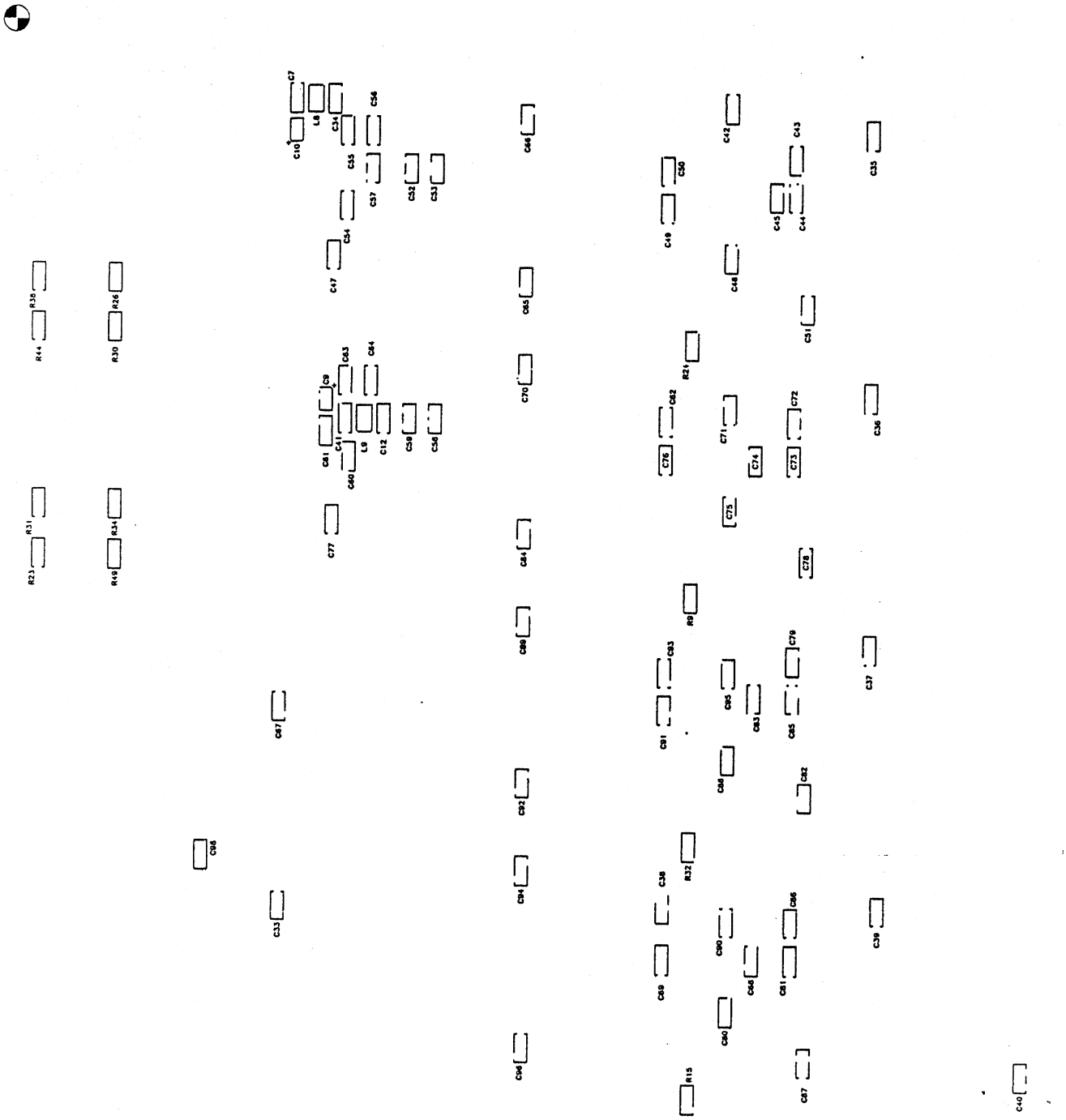
(c+) SOLDER SIDE REV 0 94-07-12
PMC SUNI-PDH EVALUATION BOARD



PMC SUNI-PDH EVALUATION BOARD
(C1) COMPONENT SIDE REV 0 94-07-15



PMC SUNI-PDH EVALUATION BOARD
(C2) GROUND PLANE REV 0 94-07-15



PMC SUNI-PDH EVALUATION BOARD
(MS) MARKING MASTER (SOLDER SIDE) REV 0 94-07-15

NOTES

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