ISSUE 4

SATURN USER NETWORK INTERFACE FOR ATM PLESIOCHRONOUS DIGITAL HIERARCHY

PM7345



S/UNI-PDH

SATURN USER NETWORK INTERFACE FOR ATM PLESIOCHRONOUS DIGITAL HIERARCHY

ERRATA

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1 FOURTH ISSUE OF THE S/UNI-PDH ERRATA

This document is the errata notice for Issue 6 of the SUNI-PDH datasheet (PMC-931011R6). This issue, Issue 4, of the SUNI-PDH errata notice supersedes all prior editions & prior versions of errata notices.

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2 ISSUE 4 ERRATA

PAGE	ERROR	DESCRIPTION/CORRECTION
20, 21	When using the PM7345-RI in synchronous mode, without handshaking between the RCA and RRDENB signals (i.e. RRDENB always asserted), there is a small probability that the assertion of RCA signal will be offset by one clock cycle for a given cell transfer.	When using the PM7345-RI in synchronous mode - ensure handshaking is provided between RCA and RRDENB. This means that RRDENB must be deasserted when not transferring cell data. One simple method of achieving this is to tie RCA to RRDENB through an inverter. Note that for this solution to function correctly, RCA must be set to its default mode - which does not provide the 4 byte advanced indication of FIFO empty. RPOS/RDAT RNEG/ROHM RCLK RRDENB RFCLK RSOC FRDATA[7:0] RCA TICLK TIC
22, 23	Tristate operation of RSOC and FRDATA[0:7] in synchronous FIFO mode when in device reset state.	When the PM7345-RI package is configured for synchronous FIFO operation (SYFIFIB=0) with TSEN asserted, and RSTB asserted, both RSOC and FRDATA[0:7] will drive valid logic levels. Both RSOC and FRDATA[0:7] become tristate upon the first rising edge of RFCLK following deassertion of RSTB.
		For more information please reference PMC-960621-"Avoiding Bus Contention on the S/UNI-PDH UTOPIA Interface".

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