# ATM Layer Cell Routing Control, Monitoring, and Policing 200 Mbit/s

## FEATURES

- Monolithic single-chip device that handles ATM switch ingress VPI/VCI address translation, cell appending, cell rate policing, counting, and OAM requirements for 65,536 Virtual Circuits (VCs).
- Instantaneous transfer rate of 200 Mbits supports a cell transfer rate of 0.355 x 106 cells/s.
- 8-bit PHY interface using direct addressing for up to four PHYs (UTOPIA Level 1) and Multi-PHY addressing for up to 32 PHYs (UTOPIA Level 2).
- 8-bit SCI-PHY™+ (53 - 64 byte extended ATM cell with prepend/ postpend) interface at output to switch fabric.
- Software compatibility with PM7322 RCMP-800.
- Compatible with wide range of switching fabrics and traffic management architectures, including per-VC or per-PHY queuing.
- Provides identification/tagging of RM cells to support adjunct processing applications such as Virtual Source/ Virtual Destination (VS/VD) Available Bit Rate (ABR) service.
- Extremely flexible CAM-type cell identification that uses arbitrary VPI/ VCI values and/or appended bytes for identification.
- Drops on command al low priority (CLP=1) cells to relieve switch congestion.
- Includes16-bit FIFO-buffered microprocessor bus interface for cell extraction and insertion (including OAM), VC table access, control and status monitoring, and configuration of the IC.
- Supports DMA access for cell extraction and insertion.
- Low power, 0.6 micron, +5 V CMOS technology.
- 240 Plastic Quad Flat Pack (PQFP).

### POLICING

- Policing performed for adherence to: Peak Cell Rate (PCR), Sustained Cell Rate (SCR), and burst tolerance (BT). Violating cells can be noted, dropped, or have CLP bits set to1.

- Policing done according to the Virtual Scheduling Algorithm (equivalent to Continuous-State Leaky Bucket Algorithm).
- Two instantiations of policing per VC.

### CELL COUNTING

- Per-VC counts maintained for low priority cells, high priority cells, cells discarded due to policing/congestion, and cells with a reduced priority.
- Per-device counts maintained include: total cells input, total cells output, OAM cells, cells discarded due to congestion, corrupted OAM cells, and unassigned/invalid VPI/VCIs.
- Per-VC performance monitoring counts maintained include: lost cells, misinserted cells, BIP-16 errors, and Severely Errored Cell Blocks (SECB).

### OAM HANDLING AND PERFORMANCE MONITORING

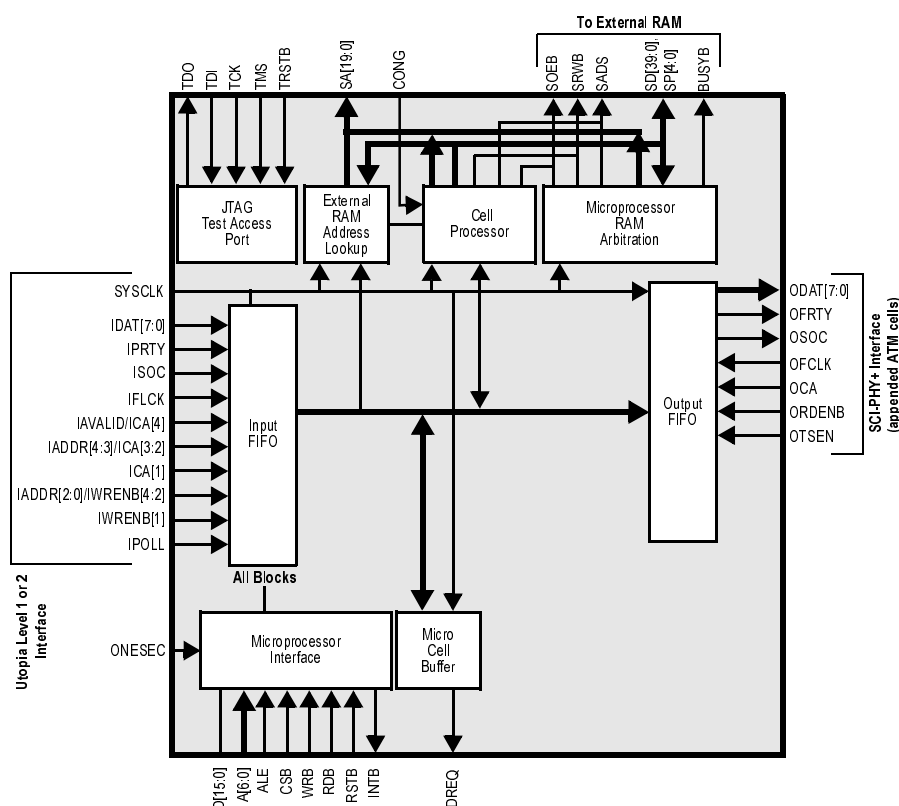- VC OAM performance monitoring per ITU Recommendation I.610,

Bellcore TR-1248 and Bellcore GR-1113- CORE.
- Automatic OAM handling includes: reception and generation of AIS and RDI cells.
- OAM cell identification/tagging provided to enable direct extraction by egress device, eliminating delays through switch core.
- Incoming OAM cells are terminated, passed to device output or microprocessor.
- Outgoing OAM cells sourced from automatic OAM generating circuitry, device input, or microprocessor.
- Generates backward reporting cells.

## APPLICATIONS

- ATM Access Switches and Multiplexers
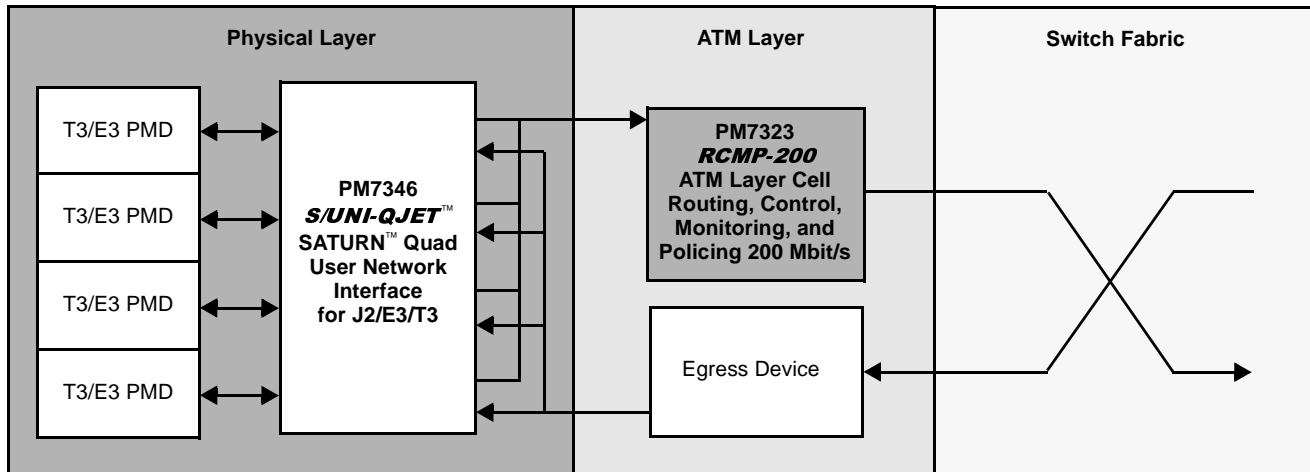- ATM Enterprise and Edge Switches

## BLOCK DIAGRAM

## TYPICAL APPLICATIONS

### MULTI-PHY T3/E3 (45/34 Mbit/s) SWITCH PORT



### MULTI-PHY T1/E1 (1.5/2.0 Mbit/s) SWITCH PORT