PM7322

3.3V SRAM INTERFACE FOR RCMP-800

Issue 1: October 7, 1996

TABLE OF CONTENTS

REFERENCE

[1] PMC-940904, "PM7322 RCMP-800 Datasheet", Issue 5, PMC-Sierra Inc.

[2] App. Note 1, "Zero Delay Bus Switches", Pericom Databook.

[3] AN-966, "Using the Bus Switch as a 5V to 3V Translator", National Semiconductor

INTRODUCTION

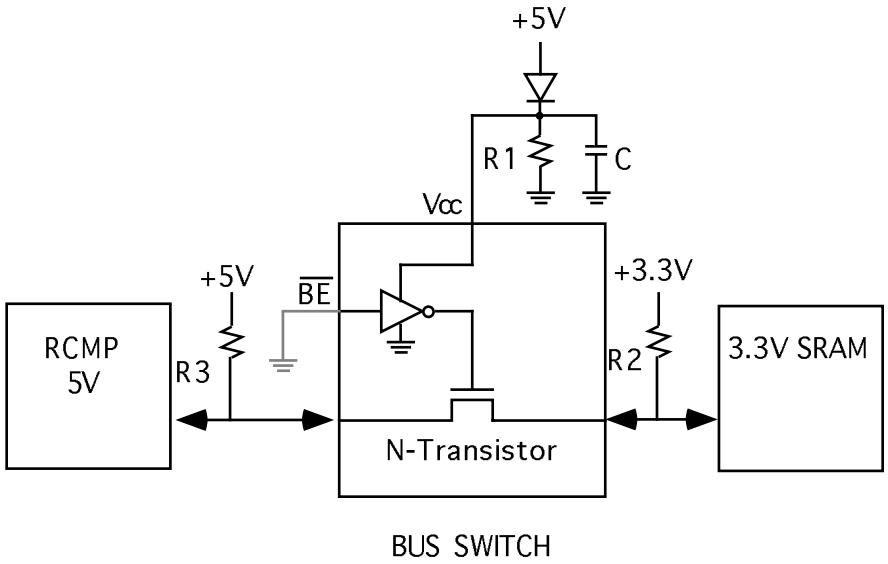
The choice of Synchronous SRAM's to be used with the RCMP-800 (which will be referred to as simply RCMP[1]) is important from both a technical and cost perspective. Currently, 3.3V Synchronous SRAM's are becoming more common, as mainly driven by demand in the PC market. In general, 3.3V SRAM's dissipate lower power, and have lower costs due to higher levels of integration. However, the majority of these 3.3V SRAM's are not 5V I/O tolerant. In order for the 5V RCMP to take advantage of these 3.3V SRAM's, simple level-translation logic can be used to overcome this 5V tolerance problem.

This appnote illustrates how the RCMP can be interfaced to 3.3V Synchronous SRAM's, using very low-power, close to zero-delay bus switches.

CIRCUIT DESCRIPTION

Fig.1 shows 5V-to-3.3V interface between the 5V RCMP and 3.3V SRAM's. It illustrates how any signal, uni-directional or bi-directional, can be connected between the 5V circuitry (the RCMP) and the 3.3V circuitry (the SRAM). For the RCMP SRAM interface, the relevant signals are the address, data, control (address strobe, write strobe, output enable) and clock.

Fig. 1 5V-to-3.3V Level-Translation Interface



[1]Note that this appnote applies equally to PM7323, the RCMP-200.

The bus switch shown is simply a N-transistor with its gate controlled by the byte-enable (BE, active-low) input. The byte-enable is tied low in this application, which causes the gate of the transistor to be high. The transistor will turn on if either the drain or the source is one threshold voltage (V_T) below the gate. The source and drain act as the I/O ports of this level translator. When the transistor is turned on, the switch becomes a very low series resistance, typically about 5 ohms, which in effect connects the input directly to the output. The switch acts as a level translator by clamping the signal level at the I/O's to at most one V_T below the V_{CC}. By changing the V_{CC}, the user can therefore control the maximum voltage seen at the I/O's. Since the switch becomes effectively only a resistor, there is close-to-zero delay (max. 250ps) incurred. Also, typical power dissipation is extremely low, about 0.1mA, or 0.2uA for low-power versions. The switch is inherently bidirectional since the transistor is symmetric.

As shown in Fig. 1, V_{CC} is limited to about 4.3V by the diode from the 5V supply. A diode that can maintain a constant voltage drop, such as the IN4001, would be suitable. R1 provides the forward biasing current for the diode, in order to maintain a constant voltage drop across the diode. A typical value for R1 is 2.2K ohm. The bypass capacitor, C, provides decoupling for the reduced V_{CC}. A typical value for C is 0.01uF. Also, optionally, R2 can be used to pull-up the signal on the 3.3V side, to ensure that the high voltage level will be close to 3.3V. Similarly, R3 can be used to pull-up the signal on the 5V side to give a 5V high voltage level. Typical value for R2 and R3 is 1K ohm.

Table 1 shows a list of vendors offering a variety of these bus switches[2]. The most common version is the dual 5-bit bus switch, the 3384, which all four vendors offer. Pericom and Quality Semiconductor have the largest selection of bus switches, tailored for many applications. The parameters that distinguish these bus switches are: power dissipation, configuration, package, and on-resistance. In particular, there are 25-ohm on-resistance versions that provide series resistance to help reduce reflections, which can be applicable to clock signals. Also, the variety of packages allow the user to optimize the board area, or to maintain footprint compatibility with devices such as 74XXX245.

[2]All of the listed vendors have Internet web pages available.

Table 1 Bus Switch Vendors

Vendor	Part Number	Configuration	ICCQ (Typ.)	Package
Cypress	CYBUS3384	Dual 5-bit	0.1mA	24 DIP/SOIC/QSOP
	CYBUS3L384	Dual 5-bit	0.2uA	24 DIP/SOIC/QSOP
National Semi.	74LVX3L384	Dual 5-bit	0.2uA	24 DIP/SOIC/QSOP
Pericom	PI5C3384	Dual 5-bit	0.2uA	24 DIP/SOIC/QSOP
(25 ohm)	PI5C32384	Dual 5-bit	0.2uA	24 DIP/SOIC/QSOP/TSSOP
	PI5C32X384	Dual 10-bit	0.2uA	48 TSSOP
(Flow-Through Pinout)	PI5C3861	Single 10-bit	0.2uA	24 SOIC/QSOP
	PI5C16861	Dual 10-bit	0.2uA	48 SSOP/TSSOP
Quality Semi.	QS3384	Dual 5-bit	1.5mA(max)	24 PDIP/SOIC/QSOP/HQSOP
	QS3L384	Dual 5-bit	0.2uA	24 PDIP/SOIC/QSOP
(25 ohm)	QS32384	Dual 5-bit	1.5mA(max)	24 PDIP/SOIC/QSOP/HQSOP
	QS32X384	Dual 10-bit	3mA(max)	48 QVSOP
(Flow-Through Pinout)	QS3861	Single 10-bit	3uA	24 SOIC/QSOP

For the RCMP SRAM interface, the total number of signals that needs to be level-translated will be: 20 bits address, 45 bits of data, 3 control signals and a clock, which is equal to 69 bits. In this case, 3 of the dual 10-bit switches and 1 of the single 10-bit switches can be used to provide this interface.

SUMMARY

This appnote shows how the RCMP can be interfaced to 3.3V SRAM's using very simple bus switches. These switches incur almost zero delay, and dissipate very little power. Also, the board area needed can be minimized with the small packages available.

NOTES

Contact us for applications support:

FAX: (604) 415-6206

PHONE: (604) 415-6000

Email: apps@pmc-sierra.bc.ca

Website: http://www.pmc-sierra.com

PMC-961022P1 Issue date: October 7, 1996

Printed in Canada