PM5350

S/UNI-® 155-ULTRA

S/UNI-ULTRA REFERENCE DESIGN

RELEASED

ISSUE 3: JULY 1999

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	March 1997	Creation of Document
2	November 1997	Incorporated changes for rev 2 of board.
3	July 1999	Incorporated changes to reflect new recommendations and included Errata fixes such as the RAVD2 power pin ramp up of the data sheet errata issue 2 of PMC-990107.

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1 OVERVIEW

The PM5350 S/UNI-ULTRA finds its application at either end of the terminal to switch or switch to switch links in a local area network (LAN). The S/UNI-ULTRA is capable of directly interfacing with a UTP-5 cable, or a fiber optics transceiver with a PECL interface. This reference design provides an example of a Peripheral Component Interconnect (PCI) Bus based Category 5 Unshielded Twisted Pair (UTP-5) or optical Asynchronous Transfer Mode (ATM) network interface card (NIC) using the PM5350 S/UNI-ULTRA.

This reference design consists of the physical layer device (S/UNI-ULTRA) and a segmentation and reassembly (SAR) device (LASAR-155). It provides a PCI bus based local ATM network UTP-5 or optics interface using SONET/SDH framing at 155.52 Mbit/s and ATM Adaptation Layer 5 (AAL5). The board is configured, monitored, and powered via a 5 Volt/32bit PCI connector compliant with the PCI SIG Specification Rev. 2.0. It employs an 8-pin 8-position Modular Jack (RJ45) to connect to the UTP-5 cables. It also contains a footprint to substitute a 9X2 optical transceiver in place of the RJ45. An on-board oscillator is provided as a reference for the S/UNI-ULTRA's integrated clock and data recovery unit on the receive side, and the clock synthesis unit on the transmit side.

A typical host for the S/UNI-ULTRA Reference Design card would be a PC with a PCI bus and software driver for configuring and monitoring the S/UNI-ULTRA and the SAR device.

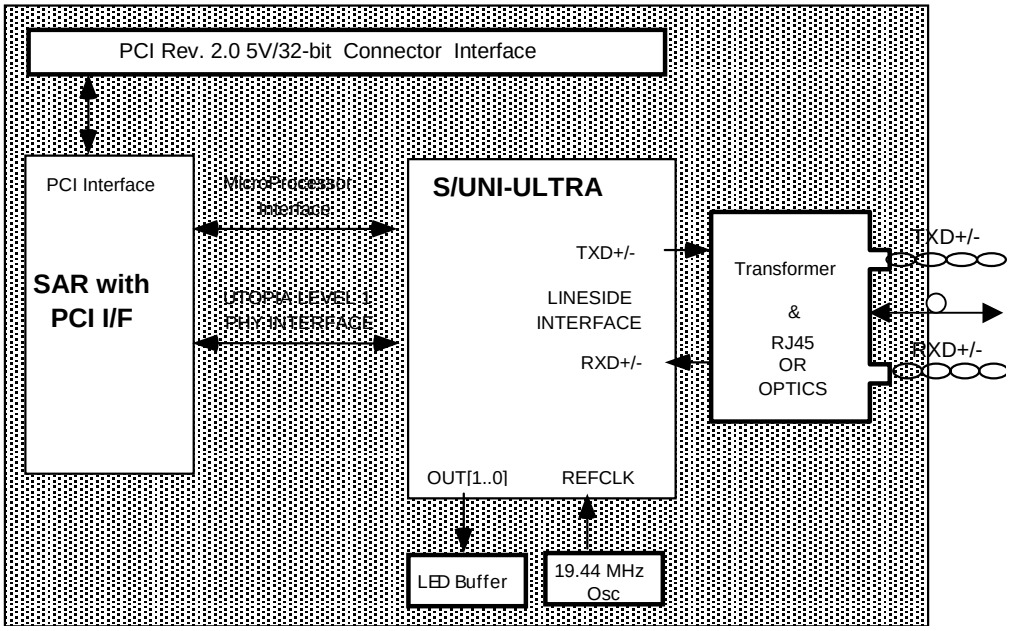
2 FUNCTIONS AND IMPLEMENTATION

The following sections provide a functional description of the components on board.

2.1 Block Diagram

The reference design consists of the S/UNI-ULTRA as the physical layer device and the PM7375 LASAR-155 (with its internal physical layer circuitry bypassed) as the SAR processor with AAL5 capabilities. A dual footprint for either an optical or a UTP-5 module is provided. In the case of UTP-5, an 8-pin 8-position RJ45 modular jack is used to connect to the UTP-5 cables, while the transformer couples signals between the RJ45 connector and the S/UNI-ULTRA. In the case of an optical link, a 9X2-footprint is provided for an optical module in place of the RJ45 connector and the transformer and all its associated terminations are not required. In addition, an on-board oscillator provides a local timing reference for both transmit and receive sections of the S/UNI-ULTRA. The functional blocks of the S/UNI-ULTRA Reference Design board are shown below:

Figure 1 - Block Diagram



In the receive direction of a UTP-5 link, the S/UNI-ULTRA will equalize the received signal, extract the digital content, process the SONET/SDH frames, and pass the extracted ATM cells to the LASAR-155 via a UTOPIA Level 1 interface. This

functionality is repeated for an optical interface, however, the equalization is not required in this case. The LASAR-155 provides the necessary cell processing and AAL5 packet reassembly before relaying the packets back to the PCI host for further processing. The reverse occurs in the transmit direction. Packets from the PCI host are processed by the LASAR-155 and the resulting AAL5 packets are segmented and mapped into ATM cells which are then written into S/UNI-ULTRA's transmit cell buffer via the UTOPIA Level 1 interface. Cells in the transmit cell buffer are then mapped into SONET/SDH frames which are output as a bit steam via the S/UNI-ULTRA's TXD+/- current drivers.

2.2 S/UNI-ULTRA (U2)

The PM5350 S/UNI-ULTRA Saturn User Network Interface is a monolithic integrated circuit that implements the SONET/SDH processing and ATM mapping functions of a 155 Mbit/s or 51 Mbit/s (in PECL mode only) ATM User Network Interface. It is fully compliant with both SONET and SDH requirements and ATM Forum UNI specifications.

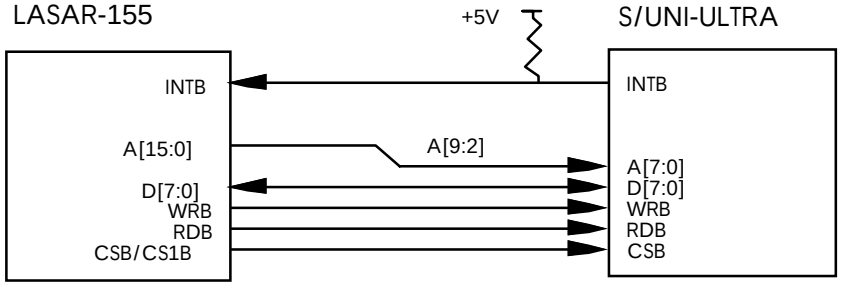
The S/UNI-ULTRA is capable of directly interfacing with a UTP-5 cable, or a fiber optics transceiver with a PECL interface. This reference design demonstrates the S/UNI-ULTRA's application in a ATM user network interface card with a UTP-5 or an optics interface card; which is compliant with the ATM Forum's PMD Interface Specifications for 155 Mb/sec.

For a detailed description of the S/UNI-ULTRA, refer to its datasheet.

2.2.1 Microprocessor Interface

The registers of the S/UNI-ULTRA are mapped into the host address space via the SAR's PCI configuration registers. This interface is configured as follows:

Figure 2 - Microprocessor Interface.

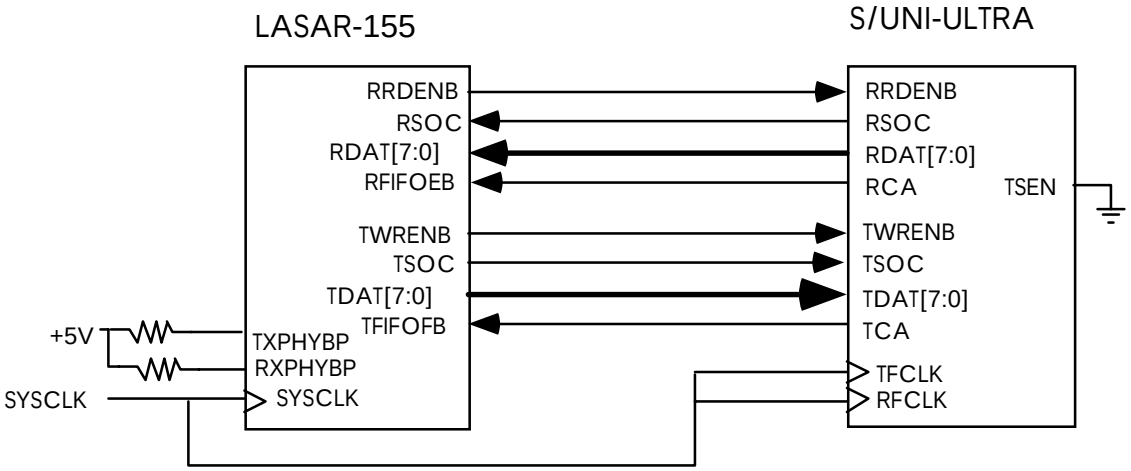


Access within this address space by a PCI host is translated by the SAR into its local bus signals which include a 8-bit address bus (A[9:2]), 8-bit data bus (D[7:0]), chip select (CSB), read (RDB), and write (WRB).

2.2.2 UTOPIA Level 1 Interface

The S/UNI-ULTRA provides a UTOPIA Level 1 drop side interface to communicate with higher level devices. In this case its 8-bit UTOPIA Level 1 interface with cell-based hand-shaking is used to communicate with the LASAR-155.

Figure 3 - UTOPIA Level 1 Interface



The FIFO clocks (TFCLK and RFCLK) of the S/UNI-ULTRA come from the PCICLKO (a buffered version of the PCI bus clock) output of the LASAR-155. The same output drives the SYSCLK input of the LASAR-155. Note that the receive and transmit FIFO interfaces of the S/UNI-ULTRA do not have to be synchronous. The same clock source is used in this application for both the transmit and receive FIFO interfaces. The rate of the clock in this application is 33 MHz.

The receive FIFO interface consists of the RRDENB, RSOC, RDAT[7:0], RXPRTY, RCA and RFCLK signals. RCA indicates whether or not a complete cell is available in the receive FIFO. RRDENB (active low) enables or disables cell data transfer out of the receive FIFO using the RDAT[7:0]. RSOC marks the start of a cell. The receive data parity output, RXPRTY, of the S/UNI-ULTRA is not used in this application.

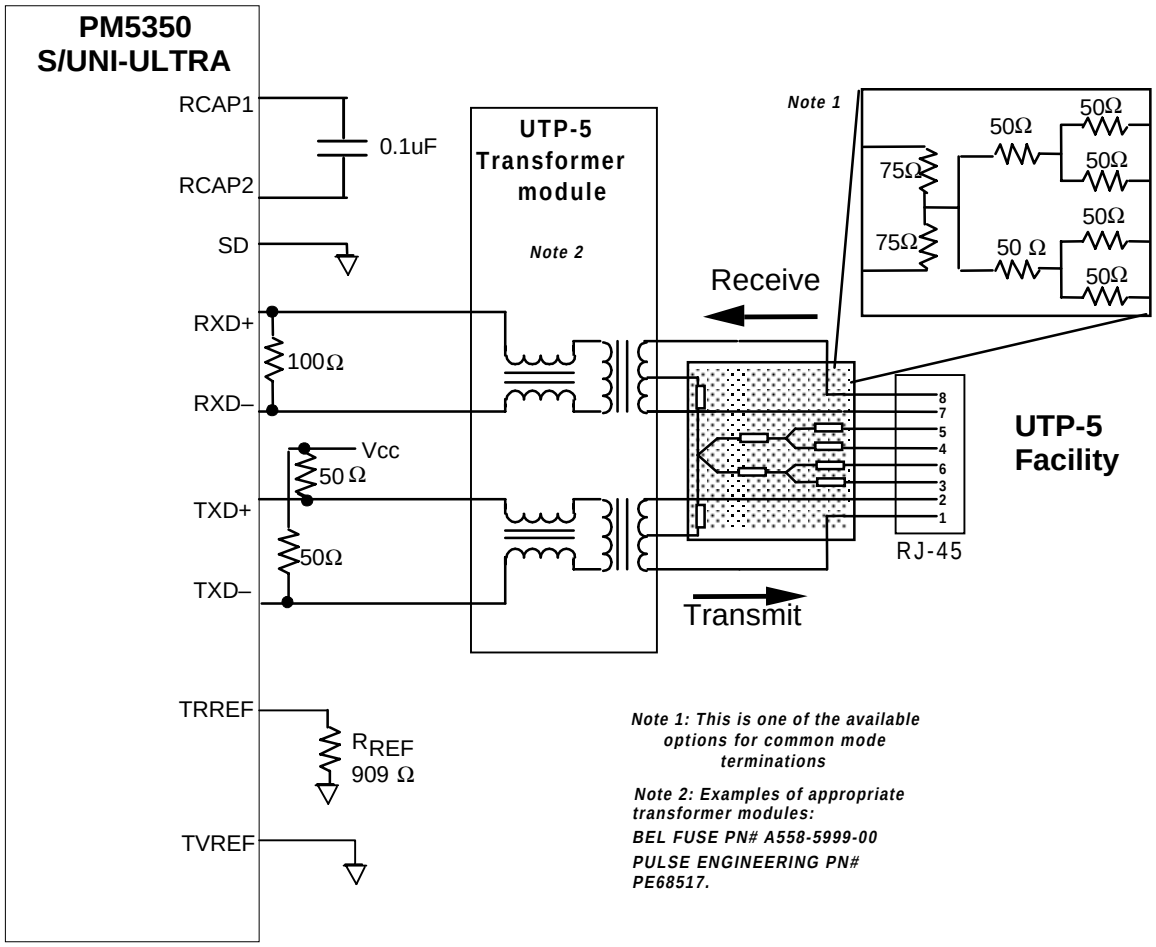
The transmit FIFO interface consists of TWRENB, TSOC, TDAT[7:0], TXPRTY, TCA, and TFCLK signals. TCA indicates whether or not the transmit FIFO can accept a complete cell. TWRENB (active low) enables or disables cell data transfer

into the transmit FIFO. TSOC marks the start of a cell. The transmit data parity input, TXPRTY, of the S/UNI-ULTRA is not used in this application.

2.3 S/UNI-ULTRA UTP-5 Line Side Interface

The UTP-5 line side interface consists of the transformer, the RJ45 connector, S/UNI-ULTRA's transmit and receive data pins, an external reference capacitor, a reference resistor, as well as a voltage reference.

Figure 4 - UTP-5 Terminations



The transformer couples signals to and from the UTP-5 cables. On the transmit side, outgoing NRZ data is coupled from the S/UNI-ULTRA's TXD+/- differential current outputs to the 8-pin 8-position RJ45 modular jack via a 1:1 turns ratio transformer. On the receive side, another 1:1 transformer couples data from the

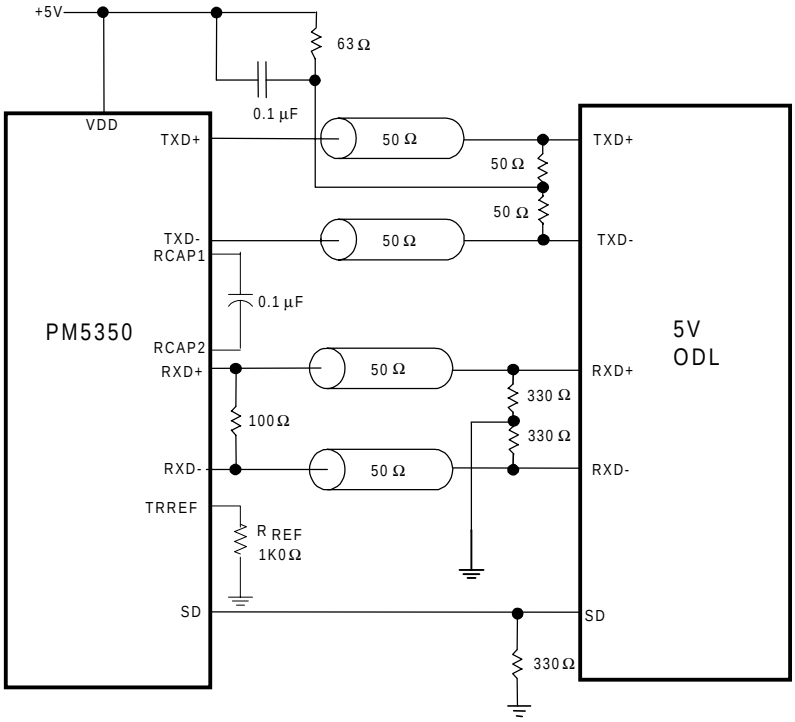
UTP-5 cables to the S/UNI-ULTRA's receiver. The receiver then performs equalization and recovers data.

Two pairs of the 4-pair UTP-5 cable are used to carry data while the unused pairs are terminated via a resistor network to a common mode termination point. The center-taps of the transformers are also terminated to the same point.

Note: Always put a 0.1uF ceramic capacitor across pins RCAP1 and RCAP2.

The S/UNI-ULTRA is also capable of interfacing with an optics module that provides a PECL electrical interface. In this type of application some external components are required to ensure proper operation of the device. The figure below illustrates the recommended circuit.

Figure 5 - PECL Transmit Terminations For ODL's



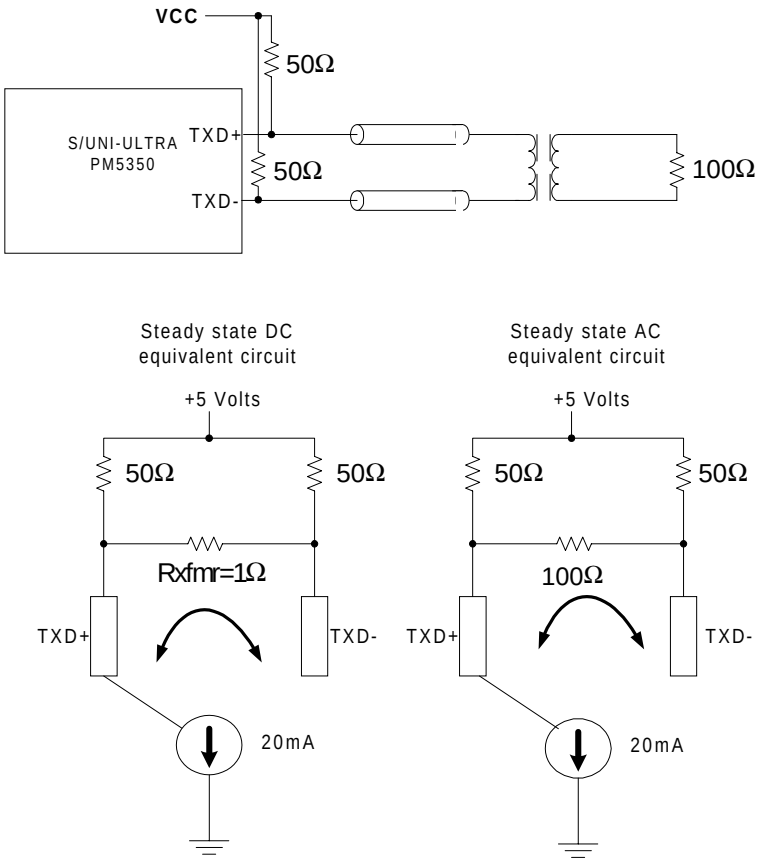
2.3.1 TXD+/-.

2.3.1.1 UTP-5 Termination.

TXD+/- are current sinking outputs that require source termination to the supply rail. Since the UTP-5 cables are 100 Ohm differential pairs, each of the TXD+/- outputs is terminated via a 50 Ohm resistors to its power supply (TAVD3).

The PECLSEL (pin 40) of the S/UNI-ULTRA is connected to digital ground to enable the RXD+/- pins for UTP-5 mode of operation. The TXD+/- steady state analysis is shown below.

Figure 6 - TXD Outputs for UTP-5 Connection Analysis



Note that the above diagram shows that the TXD+/- outputs are set up to sink 20 mA of current. External resistor RREF, connected to TRREF pin, is used to set the output current. Please refer to the External Components section of the data sheet, for correct RREF values.

When a logic 0 is produced, TXD+ sinks 20mA of current, and TXD- virtually shuts off; when a logic 1 is produced, TXD- sinks 20mA of current while TXD+ virtually shuts off.

DC wise, the winding resistance of the transformer is less than 1 Ohm, virtually a short circuit. Since a constant 20mA is being sunk by either TXD+ or TXD-, the DC common-mode voltage at the output can be calculated (Vcc = 5 Volts):

Vcc - 20 mA * 25 Ohm = 4.5 Volts

The 25 Ohm resistance is the result of the two 50 Ohm resistors in parallel (because the DC resistance of the transformer is very small). **Note that this common-mode voltage is set for UTP-5 mode of operation.**

AC wise, the 1:1 transformer and a far end 100 Ohm termination create a virtual 100 Ohm termination resistor between the TXD+/- outputs. When a logic 0 is produced, TXD- sinks 0 mA of current, while 20 mA of current flows though a resistor network of 50 Ohms in parallel with 150 Ohms (100 Ohm in series with 50 Ohm). For UTP-5 interfaces the voltage at TXD+ is calculated (Vcc = 5 Volts):

$$\text{Vcc} - 20\,\text{mA} * (50\ \text{Ohm} / / \ 150\ \text{Ohm}) = 5 - 0.02 * (\frac{50 * 150}{50 + 150}) = 4.25\text{V}$$

In a UTP-5 application, the voltage at TXD- is calculated by first finding the current through the 150 Ohm branch and then subtracting the voltage drop across the 50 Ohm resistor from Vcc:

$$\text{Current through 150 Ohm branch} = 20\text{mA} - \frac{5\text{V} - 4.25\text{V}}{50\,\text{Ohm}} = 5\text{mA}$$

$$\text{Voltage at TXD}- = 5 - 0.005 * 50 = 4.75\text{V}$$

Therefore, for a logic 0, the voltage of TXD+ will be 4.25 V while that of TXD- will be 4.75 V. For a logic 1, TXD+ will be at 4.75 Volts and TXD- will be at 4.25 Volts. The differential voltage between TXD+/- for logic 1 or 0 is 500 mV, and the peak-to-peak voltage is 1 Volt.

Footprints for additional output filtering capacitors are added in this design. In the event that fast edge cause excessive emission, these capacitors can be populated to reduce the edge rate. Care must be taken when additional filtering is used so that the output rise/fall time still meets the ATM Forum Specification to ensure interoperability.

Furthermore, since TXD+/- terminate via 50 Ohm resistors to TAVD3, output filtering capacitors should also terminate to TAVD3. The 50 termination resistors and filtering capacitors (if any) should be placed as close to the TXD+/- pins as possible.

2.3.1.2 PECL Termination.

In the case of optical interfaces, the PECL electrical interface of the optics module is terminated as shown in figure 5.

2.3.2 RXD+/-

2.3.2.1 UTP-5 Termination.

A 100 Ohm termination resistor is placed across the RXD+/- to terminate the received signal as the UTP-5 cables are 100 Ohm differential. In UTP-5 mode (with PECLSEL pin pulled low for UTP-5 operation) RXD+/- will self-bias to a typical value of Vcc/2. Note that this level is device and process dependent and can vary. The transformer AC couples the received signal from the cable to these two inputs. The received signals are then passed through the adaptive circuitry in the S/UNI-ULTRA before their digital content is extracted.

2.3.2.2 PECL Termination.

For PECL interfaces, this termination is shown in figure 6.

2.3.3 Signal Detect (SD)

The signal detect input is not used in the UTP-5 mode. Instead, an internal signal detect is generated and used by the S/UNI-ULTRA's circuitry. This internal signal detect is NOT available externally.

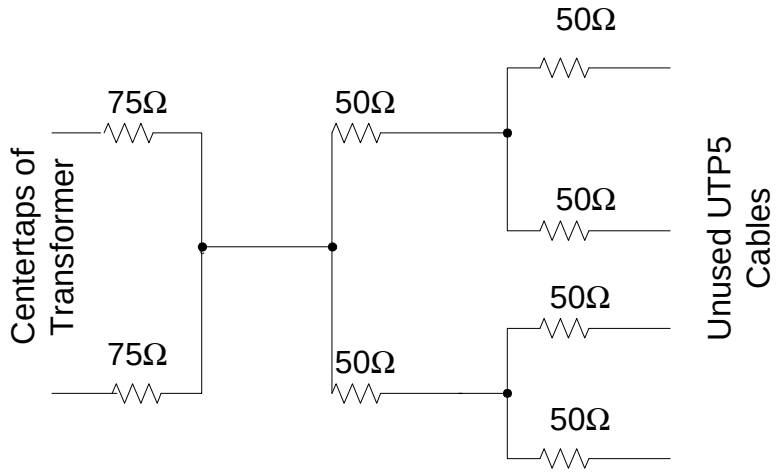
The SD pin is tied to the analog ground in UTP-5 mode to prevent noise pick up.

In interfacing to the PECL optical module, the SD input must be terminated identical to the RXD+/- inputs.

2.3.4 UTP-5 Common-mode Termination

The unused pairs of the RJ45 cable as well as the center taps of the transformer on the line side are terminated to a common-mode termination plane. The following is one of the common-mode termination schemes (note that this termination scheme may be patented). Other schemes (as suggested in the ATM Forum specification) may also be used.

Figure 7 - Unused RJ45 Connector Termination



The intended common-mode impedance is 75 Ohm. Since the UTP-5 cables are used as 50 Ohm differential pairs, a 50 Ohm resistor is added in series with each cable. Each pair of the 50 Ohm resistors are then tied together to a third 50 Ohm series resistor which is then tied to the common-mode termination plane. This scheme allows the differential impedance seen between each cable pair to be 100 Ohms and the DC common-mode impedance between each cable pair to be 50//50 + 50 = 75 Ohm.

This scheme terminates any common-mode and differential noise picked up by the unused cables, so that it will not "bounce" back and forth on the cable and radiate. Furthermore, the common-mode termination is also provided for the transformer center tap so that the common-mode noise on the signal lines is terminated.

The common-mode plane is connected to the chassis ground via two high voltage capacitors that are designed to tolerate fast transients. Direct connection from the common-mode plane to chassis ground is an electrical hazard as the common-mode voltage on the cable from a different system can differ from the chassis ground level.

2.4 SAR (U3)

The segmentation and reassembly device (SAR) used is a PM7375 LASAR-155 device which provides the following features:

- Implements the ATM Physical Layer according to the ATM Forum User Network Interface Specification and ITU-TS Recommendation I.432, and the ATM Adaptation Layer Type 5 (AAL-5) for Broadband ISDN according to ITU-TS Recommendation I.363.

- Directly supports a 32-bit PCI compliant bus interface for configuration, monitoring and transfer of packet data, with an on-chip DMA controller with scatter/gather capabilities.

- Contains an on-chip 96 cell receive buffer to accommodate up to 270 µs of PCI Bus latency.

- Supports simultaneous segmentation and re-assembly of 128 virtual circuits (VCs) in both transmit and receive directions.

- Deploys leaky bucket peak cell rate enforcement using 8 programmable peak queues coupled with sub peak control on a per VC basis; provides sustainable cell rate enforcement using the programmable peak cell rate queues and per VC token bucket averaging; and provides aggregate peak cell rate enforcement.

- Provides a SCI PHY and UTOPIA Level 1 compliant interface for connection to external ATM PHY layer devices.

The hardware configuration of the LASAR-155 is as follows:

- Bypass the transmit and receive PHY portion and use SCI-PHY/UTOPIA Level 1 interface by tying RXPHYBP (pin 152) and TXPHYBP (pin 92) low.

- Bypass the external expansion ROM by tying ROMP (pin 132) low.

- Enable PCI Host to access LASAR-155 registers by tying MPENB (pin 153) high. This setting also puts the LASAR-155 in master mode in which its address and data pins can be used to control an external device (such as the S/UNI-ULTRA). In the master mode, D[7:0] are used as I/O's, and A[15:0] are used as outputs.

- The analog portion of the LASAR-155 is shut down to conserve power. To do so, RAVD[4:1], TAVD[3:1], and TXVDD pins are connected via resistors to ground. In addition, all inputs on the analog side (ALOS+/-, RRCLK+/-, RXD+/-, TRCLK+/-, and LF+/-) are connected via resistors to ground. All analog outputs (TXD+/-, and LFO) are left unconnected.

- All the PCI bus signals are connected directly to the designated pins on the 5V/32-bit PCI connector.

- A buffered version of PCI clock is used for the LASAR-155's Adaptation Layer timing. This is done by connecting PCICLKO (pin 196) to SYSCLK (pin 81). The same PCICLKO is connected to the S/UNI-ULTRA's drop side FIFO clock inputs (RFCLK and TFCLK). The frequency of this clock is 33 MHz.

- The physical layer functions of the LASAR-155 is disabled by connecting the RXPHYBP (pin 152) and TXPHYBP (pin 92) to +5 Volts via pull-up resistors.

Detailed description of the interface between the LASAR-155 and the S/UNI-ULTRA is provided in earlier sections.

2.5 Power and Ground Connections

The S/UNI-ULTRA Reference Design card is powered through a 5V 32bit PCI edge connector. Only the 5V and GND supplies are required by the card. Solder bridges are provided to allow direct connection from the common-mode termination plane to chassis ground (it is advised to use high-voltage capacitors to AC couple the common-mode plane to chassis ground as the common-mode voltage on the cable from a different system can differ from the chassis ground level). The S/UNI-ULTRA's Vcc and the LASAR-155's Vcc comes directly from the PCI connector. Some solder bridges (marked as SB) are placed between the S/UNI-ULTRA and the LASAR, effectively forming a partial cut. These are experimental and can be closed to remove the isolation between the LASAR and the S/UNI-ULTRA.

The common-mode termination plane is AC coupled to chassis ground via two high voltage capacitors. These capacitors protect against high voltage spikes received on UTP-5 cables.

2.6 Oscillator (Y1)

The 19.44 MHz TTL/CMOS oscillator provides a local reference to the clock and data recovery circuitry of the S/UNI-ULTRA on the receive side, and clock synthesis circuitry on the transmit side. The output of the oscillator is connected to the digital REFCLK input of the S/UNI-ULTRA.

On the receive side, the 19.44MHz clock input is used by the clock recovery unit (CRU) as a reference in the following fashion:

- Initially (after power up or under loss of signal condition) the phase-locked-loop (PLL) of the CRU locks to the REFCLK.

- When the frequency of the recovered clock is within the specified range (488 ppm) of the REFCLK, the PPL attempts to lock onto the data.

- Once in data lock, in STS-3c/STM-1 mode, the PLL will continue to compare a divided by 8 version of the recovered clock to the REFCLK, and will switch back to lock onto the REFCLK if the frequency difference is greater than 488 ppm. The PLL will also switch to the REFCLK when no data transition occurs in 80 bit periods.

On the transmit side, S/UNI-ULTRA synthesizes its line rate clock (155.52 MHz) either from the 19.44 MHz REFCLK in non-loop-timed mode or bypasses the clock synthesis unit and uses the recovered clock directly in loop-timed mode.

The following is a summary of how REFCLK is used by the transmitter:

- In loop-timed mode: The transmitter timing is derived from the output of the CRU, while the internal transmit clock synthesis unit (CSU) is bypassed. When the CRU is in data lock, the recovered clock is then the output of the CRU. If the CRU loses data lock (i.e. no data transition for 80 bit periods or the divided version of the recovered clock differs from the REFCLK by more than 488 ppm), it will switch to lock onto the REFCLK and output a line rate clock that is synchronous to the REFCLK.

- In non-loop-timed mode: The S/UNI-ULTRA's transmitter will always use its CSU to synthesize the line rate clock from the REFCLK.

As a result, the on-board oscillator is always necessary regardless of whether the S/UNI-ULTRA is in loop-timed or non-loop-timed mode. Furthermore, the ATM Forum specification requires the transmit clock to be +/- 100 ppm for an ATM user device and +/- 20 ppm for an ATM network device.

2.7 Bandgap Reference and RREF Resistor

It is recommended that the internal bandgap reference be used (see figure 4). When using the internal bandgap reference, the RREF should be 1.30K Ohm. in PECL mode (Optical I/F). In UTP-5 mode, RREF should typically be 909 ohms. For more detail on RREF resistor, please see section “External Components” in the PM5350 data sheet, document number pmc-960924.

3 STANDARD COMPLIANCE

The S/UNI-ULTRA Reference Design is designed to the following specifications:

- The ATM Forum ATM Physical Medium Dependent Interface Specification for 155 Mb/s over Twisted Pair Cable (AF-PHY-0015.000) Version 1.0
- ANSI/TIA/EIA-568-A Building Telecommunications Wiring Standards

Note 1: The phrase "ATM Forum specification" refers to the "AF-PHY-0053.000 ATM Forum ATM Physical Medium Dependent Interface Specification for 155 Mb/s over Twisted Pair Cable" specification.

The ATM Forum specification is a system level specification. The following sections highlight the factors that would impact each requirement.

3.1 Transmission Requirements

3.1.1 Line Rates and Bit Timing

The ATM Forum specification requires the following:

1. ATM Forum UNI Specification 3.1 STS-3c frame format
2. Encoded line rate of 155.52 MBaud +/- 20 ppm for ATM network device
3. Ability for ATM user device derive its transmit clock from received line signal
4. Provision for the ATM user device to use a free-running transmit clock that operates at 155.52 MHz +/- 100 ppm

S/UNI-ULTRA meets requirement 1 by providing an ATM Forum UNI 3.1 compliant STS-3c frame format.

Requirement 2 applies to an ATM network device (i.e., an ATM LAN switch with a UTP-5 interface) which provides timing reference to all connected ATM user devices. The S/UNI-ULTRA can synthesize a 155.52 MHz transmit clock by multiplying a 19.44 MHz reference clock input by 8, and the accuracy of this synthesized clock is dependent on the accuracy of the reference oscillator. Therefore, when using S/UNI-ULTRA as an ATM network device, a 19.44 MHz +/-20 ppm or better oscillator should be used to meet this requirement.

Requirements 3 and 4 apply to this reference design which is configured as an ATM user device. The S/UNI-ULTRA can be set up (via its internal registers) in "loop-timed" mode in which its transmitter uses the clock output of the clock and data

recovery unit (CRU) on the receive side. When there is good incoming data, the CRU will lock onto data, recover the clock, and output the line rate clock to the transmitter. The transmitter will then output data using the recovered clock as required by requirement 3. Upon loss of signal, the CRU will switch to lock onto the REFCLK input and output a line-rate clock to the transmitter. In that case, the transmitter's accuracy is essentially dependent on the REFCLK accuracy. To meet requirement 4, a 19.44 MHz +/-100 ppm or better on-board oscillator should be used.

3.1.2 Line Code

As required, the S/UNI-ULTRA will output and receive binary Non-Return to Zero (NRZ) bit steams.

3.1.3 Bit Error Rate

Bit errors can be caused by signal level, noise and jitter. With the recommended layout and components, a S/UNI-ULTRA design should operate with a bit error rate of less than 10^{-10} when connected to a ATM Forum Specification compliant device via the channel reference model defined in the ATM Forum Specification.

3.2 UTP-5 Active Output Interface (AOI)

3.2.1 Load

The ATM Forum requires the load to be 100 Ohm UTP or 150 Ohm STP cables. The S/UNI-ULTRA is configured to drive 100 Ohm (differential) UTP-5 cables in this application note.

3.2.2 Differential Output Voltage

The required output voltage across a 100 Ohm test load is 1 Volt +/- 6%. The S/UNI-ULTRA's transmitter output accuracy depends directly on the precision of the voltage reference, reference resistor RREF as well as the insertion loss of the transformer and RJ45 modular jack. Resistor RREF, allows the output amplitude to be adjusted to compensate for this insertion loss. For a detailed description on how to adjust output amplitude, refer to section 2.3 and the External Component section of the data sheet

Using the recommended magnetics, voltage reference, and reference resistor, this requirement can be met.

3.2.3 Waveform Overshoot

The waveform overshoot and undershoot are caused primarily by impedance mismatch. With proper source termination, matched transmission line, and load termination, the over/undershoot seen at the 100 Ohm test load should be less than 10% which is the ATM Forum requirement for UTP-5 applications.

3.2.4 Return Loss

Return loss is a measure of impedance mismatch at a junction and applies to the UTP-5 mode of operation. It is determined by applying a balanced differential signal to the junction and measuring the reflection back. Return loss is impacted by the RJ45 modular jack, the transformer, and the transmission lines connected to the TXD+/- outputs of the S/UNI-ULTRA. Any discontinuity in this path will affect return loss. With the recommended transformer, RJ45, and layout, the S/UNI-ULTRA design should meet the return loss requirement which is summarized in the following table:

Return Loss	Frequency Range
> 16 dB	2 MHz - 30 MHz
> 16 dB - 20*log(f/30 MHz)	30 MHz - 60 MHz
> 10 dB	60 MHz - 100 MHz

3.2.5 Rise/Fall Times

The ATM Forum allowed rise/fall time at the transformer output is between 1.5 ns and 3.5 ns. The overall rise/fall time of a system is approximated by taking the square-root of the sum of the square of each device's rise/fall time. In the transmit path, the most significant factors affecting the overall system rise/fall time are the S/UNI-ULTRA's TXD+/- outputs and the transformer. For example, if the S/UNI-ULTRA has an output rise/fall time of approximately 2.0ns, using a transformer with a rise/fall time of 2.0 ns, the overall rise/fall time of the system is:

$$T_{\text{rise total}} = \sqrt{T_{\text{rise ultra}}^2 + T_{\text{rise transformer}}^2}$$
$$= \sqrt{2.0^2 + 2.0^2} = 2.83 \text{ ns}$$

Should emission due to fast data edges become a problem, additional capacitance on the TXD+/- outputs can be used to increase the rise/fall time. Ideally, the slowest possible rise time that the specification allows is the most desirable because faster edges produce greater emission.

3.2.6 Duty Cycle Distortion

Duty cycle distortion is caused by:

- asymmetry in the two branches of the differential pair
- asymmetry in rise and fall time

Asymmetry in the differential pair is caused by routing one trace longer than the other trace of the pair or routing the two traces with different characteristics impedance and the asymmetry in the transformer.

The S/UNI-ULTRA's TXD+/- output duty cycle is very close to 50/50. Therefore, using the recommended magnetics and layout, this requirement can be meet.

3.2.7 Jitter

Transmit jitter can be caused by:

- output duty cycle distortion
- jitter on transmitter clock
- board level noise

As indicated earlier, the transformer and the S/UNI-ULTRA's TXD+/- will always have small amount of inherent duty cycle distortion. This duty cycle distortion is very small and should only consume a small amount of system jitter budget. Additional duty cycle distortion can be limited by balancing both branches of the TXD+/- path (such as routing the signals with equal lengths).

In loop-time mode, in which the S/UNI-ULTRA's transmitter timing is derived from the received data, the jitter on the transmitter clock can be caused by noise on the S/UNI-ULTRA's receive side as well as on the TXD+/- outputs' power supply. Careful layout and decoupling can reduce this jitter.

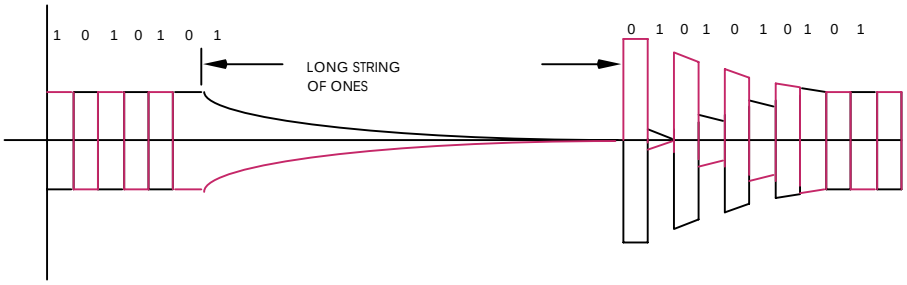
In non-loop-timed mode, the jitter on the transmitter clock is caused by noise on the transmit side (especially the transmit clock synthesis circuitry) and the intrinsic jitter of the reference oscillator. Again, a careful layout and a clean reference oscillator go a long way in reducing this jitter.

3.2.8 UTP-5 Baseline Wander

Baseline wander is the decay of output voltage due to the high-pass nature of the transformer. DC or near DC contents of the signal are blocked (or greatly

attenuated), causing the output voltage to drop towards the average DC level. All AC coupled systems exhibit this phenomenon.

The following diagram illustrates the effects of baseline wander:



As the diagram indicates, long string of ones will cause the voltage across the two output terminals of the transmit to converge to a common-mode level (on the receive side, it is set by the S/UNI-ULTRA's RXD+/- self-bias voltage). In the worst case, the voltage difference will diminish, causing the receiver not being able to distinguish between 0's and 1's.

The above diagram also indicates that, after a long string of no transitions, the baselines of the positive and negative signals are so far apart that when transitions do occur, initially the consecutive 0's and 1's amplitude will be different. This abrupt change in 0's and 1's amplitude will cause the equalizer not equalize properly and introduce bit errors. Although it is arguable that, in an ATM network where scrambling occurs at the cell and SONET frame levels, 100 bits of consecutive one's and zeros will occur, baseline wander should still be taken into consideration because it can still be caused by a data pattern that has many more 1's than 0's or vice versa.

Therefore, to achieve maximum 10% decay over 100 bits of logical one (or logical zero) as required, the transformer must have an OCL of at least 350 nH. The recommended transformers all meet the 350 nH OCL requirement.

3.3 UTP-5 Active Input Interface

3.3.1 Differential Input Signals

The ATM Forum Specification requires the receiver to interpret a positive voltage on the RXD+ pin with respect to the RXD- pin as a logical ONE, and the reverse as a logical ZERO. The S/UNI-ULTRA interprets the received signals as required.

3.3.2 Differential Return Loss

The parameters for differential return loss for the **AII** are the same as those of the AOI. The differential return loss is a measurement of impedance mismatch on the receive side. Differential return loss is affected by any discontinuity in the receive path which includes the RJ45 connector, the receive side of the transformer, the traces connected to the S/UNI-ULTRA's RXD+/- inputs and the termination resistor. Minimizing discontinuity in the receive path will minimize the return loss.

3.3.3 Common-mode Rejection

Common-mode noise can "leak" across the transformer as common-mode as well differential signals. The common-mode choke of the transformer will provide the bulk of the common-mode rejection. Using the recommended magnetics, the common-mode or differential noise reaching the RXD+/- inputs is insignificant.

3.3.4 Input Jitter Tolerance

The ATM Forum specification requires the input jitter tolerance of the receive to be 3.5 ns. The receiver jitter tolerance depends on the board layout, the symmetry of the receive transformer's rise/fall time, as well as the S/UNI-ULTRA's clock and data recovery unit's (CRU) ability to recover data.

The asymmetry in the rise/fall time of the receive transformer can create duty cycle distortion which is seen as jitter by the receiver of the S/UNI-ULTRA. Furthermore, the S/UNI-ULTRA's equalization and baseline wander correction circuitry does not provide jitter attenuation. Noise introduced in these portions of the circuitry will in fact add jitter to the equalized signal before it reaches the CRU.

Therefore, it is essential to provide a quiet analog power supply with adequate external decoupling to these circuitry and a transformer with clean duty cycle. With good power supply decoupling on the analog receive section and the recommended magnetics, a S/UNI-ULTRA design will meet this requirement.

3.4 Electromagnetic Susceptibility & Impulse Noise

3.4.1 Electromagnetic Susceptibility

Annex B of the ATM Forum Specification requires the PMD/PHY implementation to pass a 3/m field electromagnetic susceptibility test (IEC 801-3, Level 2). Using the recommended magnetics, this requirement can be met. In an optical interface the

requirements are easier to pass since the transformer and the RJ45 connector are not present.

3.4.2 Impulse (Fast Transient) Noise

Annex B of the ATM Forum AF-PHY-0015-000 specification requires the PMD/PHY implementation to be able to recover from a 500 V of impulse noise without operator intervention. The test condition and characteristics of the impulse noise are defined in the IEC 1000-4-4 standard. The IEC level 2 impulse noise on I/O signal is a 500 V impulse with 5 ns rise time. This requirement arises from the fact that UTP-5 cables installed inside a building sometimes have to run adjacent to power lines. The switching current on the power lines (due to motors starting or stopping) can induce voltage spikes on these unshielded cables. If unattenuated, the voltage spike reaching the input of a CMOS device can cause latch-up conditions and damage the device. This problem does not apply to optical links.

Typically, on slower speed data lines (such as telephone wires), transient surge suppressers are used to either attenuate transients or divert transients away from sensitive loads. The problem arises when capacitance of most transient surge suppressers (other than gas discharge tubes) alters the signal integrity. With stringent requirements by the ATM Forum on the transmitter output amplitude and rise time, it is not feasible to attach transient suppressers to each RJ45 cables. Because UTP-5 cables are tightly twisted together, fast transients will typically couple onto the UTP-5 cable as common-mode noise which will be rejected by a transformer with common-mode chokes before they can cause any damages. Furthermore, high voltage capacitors (500 V or higher rating) with values around 0.1 uF can be used to divert the common-mode fast transients to chassis ground.

3.5 Copper Link Characteristics

The ATM Forum specification requires copper link characteristics and installation to conform to EIA/TIA-568-A cabling specification. The details of the EIA/TIA-568-A specifications are beyond the scope of this document.

3.6 UTP-5 Emission Standard Compliance

To meet emission standards such as FCC Class B or CISPR, layout and component selection are critical. Compliance tests results on rev 1 of this reference design (also available on the Web) from an independent test lab attached in the appendix show that the rev 1 S/UNI-ULTRA Reference Design meets the following specifications:

- EN55022:1994 Radiated Emissions 30MHz - 1000MHz Class B

- EN55022:1994 Conducted Emissions 150KHz - 30MHz Class B
- IEC1000-4-2 Electrostatic Discharge Level B
- IEC1000-4-3 RF Electromagnetic Fields Level A
- IEC1000-4-4 Fast Transient/Burst Level B

These tests have not been verified on this revision (rev 2) of the reference design. However, these results are not expected to be any different in this revision of the board and will be documented, when the measurements are completed, in the next issue of this document.

3.7 Summary

The following table provides a summary of ATM Forum requirements and the components that may affect them.

ATM Forum Requirements		Related Components
General		
	Line Rates and Bit Timing	S/UNI-ULTRA
	Line Code	S/UNI-ULTRA
	Bit Error Rate	all components, layout
Active Output Interface		
	Differential Output Voltage	transformer, RJ45, S/UNI-ULTRA txd+/- outputs, the bandgap reference, TRREF resistor value,
	Waveform Overshoot	transformer, RJ45, impedance of signal traces connected to the S/UNI-ULTRA TXD+/- outputs
	Return Loss	transformer, RJ45, impedance of signal traces connected to the S/UNI-ULTRA TXD+/- outputs
	Rise/Fall Times	transformer, capacitive loading of the TXD+/- outputs
	Duty Cycle Distortion	S/UNI-ULTRA's TXD+/- outputs and the signal traces connected to the TXD+/- outputs, transformer
	Jitter	on-board reference oscillator of the S/UNI-ULTRA, duty cycle of S/UNI-ULTRA's TXD+/- outputs, board level noise
	Baseline Wander	transformer OCL
Active Input Interface		

	Differential Input Signal Polarity	S/UNI-ULTRA
	Differential Return Loss	transformer, RJ45, impedance of the RXD+/- signal traces, termination resistor between RXD+/-
	Common-mode Rejection	transformer, S/UNI-ULTRA's common-mode rejection on RXD+/- inputs
	Input Jitter Tolerance	transformer, board level noise
Copper Link Characteristics		UTP-5 cable & patch cords, RJ45 connector, patch panels, transition connectors, cross-connect fields, and telecommunication outlets
Electromagnetic Susceptibility		transformer and common-mode termination
Impulse (Fast Transients)		transformer & layout of the common-mode termination plane

4 LAYOUT DESCRIPTIONS

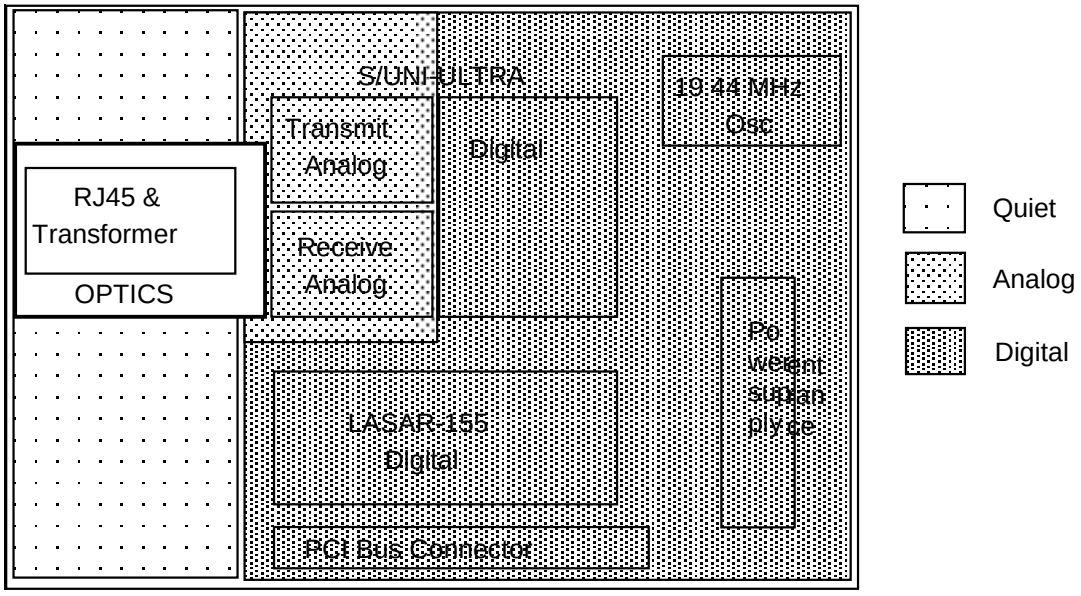
4.1 Component Placement

The overall placement strategies of the components are:

- Place the analog circuitry away from the digital circuitry.
- Keep analog transmit side components separate from the analog receive side components.
- Place the RJ45 and the transformer further away from any active circuitry (analog or digital).
- Keep the transformer as close to the RJ45 as possible so that the common-mode noise riding on the traces coming from the RJ45 will be suppressed by the transformer before it can radiate.

The overall placement is as follows:

Figure 8 - Main Component Placement Diagram



The RJ45 and transformer are placed as far away from all of the analog and digital circuitry as possible to prevent noise coupling. This is not required when using an optical module in the case of an optical interface. The analog circuitry is placed further away from the power supply entrance than the digital circuitry. With

adequate bypassing and decoupling on the digital side the digital Vcc and ground noise will not propagate to the analog section. The separation of the analog and digital areas shown in the diagram are due to these reasons alone, not because they are physically separate. Local decoupling capacitors are also placed near all analog and digital power supply pins.

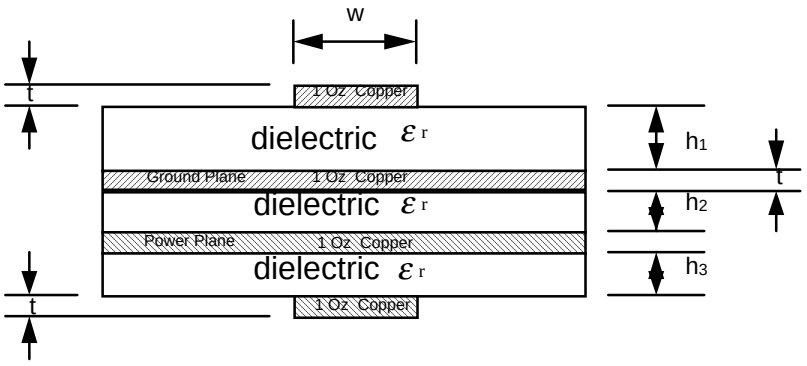
In addition, the following rules are used:

- The LASAR-155 device is placed such that all the PCI interface traces are within the specified length limits of the PCI Rev. 2.0 Specification, while being as close to the S/UNI-ULTRA as possible.
- The oscillator (Y1) is placed in a quiet digital section as noise on its power supply will cause jitter on the output, and the oscillator itself generates noise that may affect sensitive analog circuits. The pin-out of the S/UNI-ULTRA facilitates this placement by locating the REFCLK input on the digital side and powering the input via the digital supply as well.
- All source termination resistors are placed near the outputs and load termination resistors are placed near the inputs. In particular, the source termination resistors for the TXD+/- outputs of the S/UNI-ULTRA are placed near these outputs.
- All pull down resistors are placed near the output pins.
- All decoupling capacitors are placed near the power supply pins. All bypassing capacitors on the analog side are placed near the ferrite beads. The bulk decoupling capacitors are placed near the power entrance.

4.2 Layer Stacking and Transmission Line Impedance Control

The S/UNI-ULTRA Reference Design card has four layers: (from the top down) layer 1 and 4 for signals, layer 2 for ground, and layer 3 for power. The dimension of the card conforms to the 5V PCI Raw Short Card, with custom mounting hole locations. The layer configurations are shown below:

Figure 9 - PCB Cross Section



where

ε_r = relative dielectric constant, nominally 5.0 for G-10 fibre-glass epoxy

t = thickness of the copper, fixed according to the weight of copper selected. For 1 oz copper, the thickness is 1.4 mil. This thickness can be ignored if w is great enough.

h1, h2, h3 = thickness of dielectric.

w = width of copper

The PCB related parameters are shown in the following table:

Parameters	Nominal
Board Thickness (mil)	62 (including copper thickness)
dielectric thickness between layers 1 and 2 (mil) (h1)	10
dielectric thickness between layers 2 and 3 (mil) (h2)	33
dielectric thickness between layers 3 and 4 (mil) (h3)	10
Relative dielectric constant	4.2

To reduce signal degradation due to reflection and radiation, the traces that carry high speed signals should be treated as micro strip transmission lines with controlled impedance and matched resistive termination. The trace impedance is calculated using the formula:

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

Parameter	Data
ε_r	4.2
h1 (mil)	10
t (mil) (2 Oz copper)	2.88
Zo (Ohm)	50
W (mil)	16

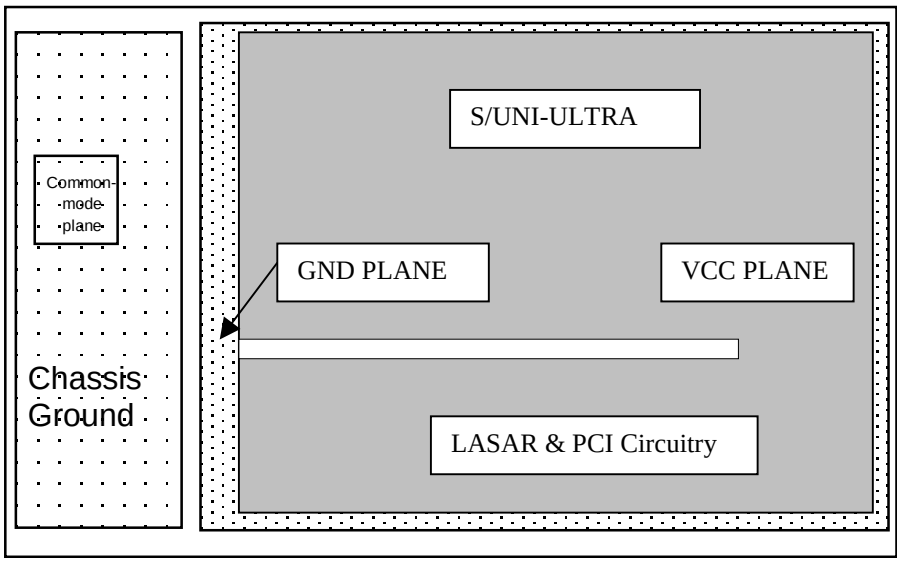
Given a characteristics impedance Zo, the dielectric thickness h1 is proportional to trace width. A small h1 will result in the traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board for a given trace impedance and adequate trace width should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication.

Using the same h1, thickness of copper, and dielectric constant, a 16 mil traces has a characteristic impedance of approximately 50 Ohms while an 6 mil trace has a characteristic impedance of 75 Ohms.

4.3 Power and Ground

One ground/Vcc pair is used for the whole board. The following diagram illustrates the power and ground plane distribution:

Figure 10 - Power/Ground Plane Outline



The PCI Bus Vcc, LASAR Vcc, and S/UNI-ULTRA are all contained in one plane. The VCC plane is cut as shown to isolate the LASAR Vcc from the S/UNI-ULTRA's Vcc as shown in the above diagram. However, this cut is for experimental purposes and solder bridges are provided to eliminate the cut is so desired.

A single ground is provided for all circuitry, except the transformer and RJ45 connector, to minimize impedance.

A common-mode termination island is placed on the Vcc layer under the RJ45 to provide a termination plane for the unused signals as well as the center taps of the transformer. This island is isolated from the power and ground planes of the rest of the board to minimize noise pickup which leads to emission. A chassis ground island is placed on the ground layer directly under the common-mode termination plane so that the common-mode island can be AC coupled to the chassis ground island.

To connect the chassis ground island to the system's chassis ground, the mounting screws can be used as chassis ground contact points as they make mechanical contact with the mounting bracket which in turn connects mechanically to the chassis. Furthermore, if a shielded RJ45 connector is used, the shield should also be connected to the chassis ground island in order for it to be effective.

The area underneath the transformer should have no planes on any layers to avoid coupling from the transformer.

4.4 Decoupling, Bypassing and Bulk Capacitors

4.4.1 Theory

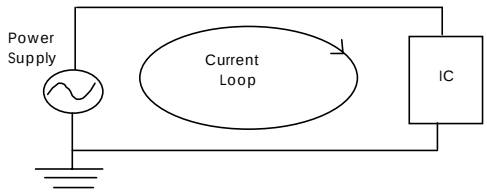
Decoupling capacitors provide localized switching current required by the power pins they connect to.

Bypassing capacitors remove unwanted power supply noise before it can enter sensitive areas.

Bulk capacitors are used to maintain constant dc voltage and provide switching currents required by all components.

The power distribution loop of power supply and an IC is illustrated below:

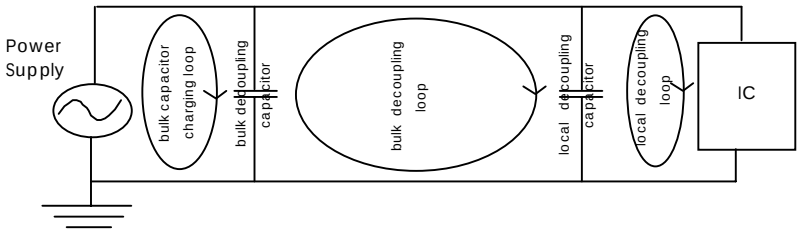
Figure 11 - Current Loop Model No Decoupling Capacitors



Without any capacitors in parallel, when the IC switches, it will attempt to draw a large switching current directly from the power supply which could be located far away. The inductance on the power and ground plane will limit this instantaneous current drawn. As a result , the voltage at the IC's power pin will drop and the output will ramp up more slowly. Furthermore, since EMI is a function of loop area and frequency. The large the loop area and the higher the frequency, the more significant the EMI.

Adding decoupling capacitors breaks the current loop into several smaller loops as illustrated below:

Figure 12 - Current Loop Model With Decoupling Capacitors



The local decoupling loop is created as a result of a decouple capacitor placed close to the IC's power pin. The bulk decoupling loop is created by charging the local decoupling capacitors via the bulk decoupling capacitor. Finally, the bulk decoupling capacitor itself is charged by the power supply via the bulk decoupling charging loop. Consequently, bulk decoupling capacitors should be placed near the power supply entrance, while local decoupling capacitors should be placed near the power pins of the ICs they decouple. In addition, bypass capacitors can be added in between the local and bulk decoupling capacitors to break the bulk decoupling loop into smaller loops.

In order for the bulk decoupling to maintain a relatively constant DC voltage, it must be able to supply all the charging current demands of the local decoupling capacitors. A rule of thumb is that the value of the bulk decoupling capacitor should be at least ten times the sum of all local decoupling and bypass capacitors.

4.4.2 Calculation of Decoupling Capacitor Values

In order for local decoupling capacitors to be effective, they must provide the least impedance at the switching frequency of the IC; otherwise, they will not discharge at all because the switching current will come from other lower impedance paths (and possibly larger loops). Therefore, one must choose a decoupling capacitor that has a resonant frequency (where it has the lowest impedance) same as (or close to) the frequency of the switching, and place the decoupling capacitor as close to the power pin as possible to reduce trace inductance. In addition, the local decoupling capacitor must be large enough to provide the instantaneous current with tolerable voltage drop. The decoupling capacitance required per Vcc pin can be calculated using the following formula:

$C = I \Delta t / \Delta V$, where

C = total capacitance in Farads

I = instantaneous switching current in Amps

Δt = the time duration of the switching current

ΔV = maximum allowed voltage drop on Vcc supply

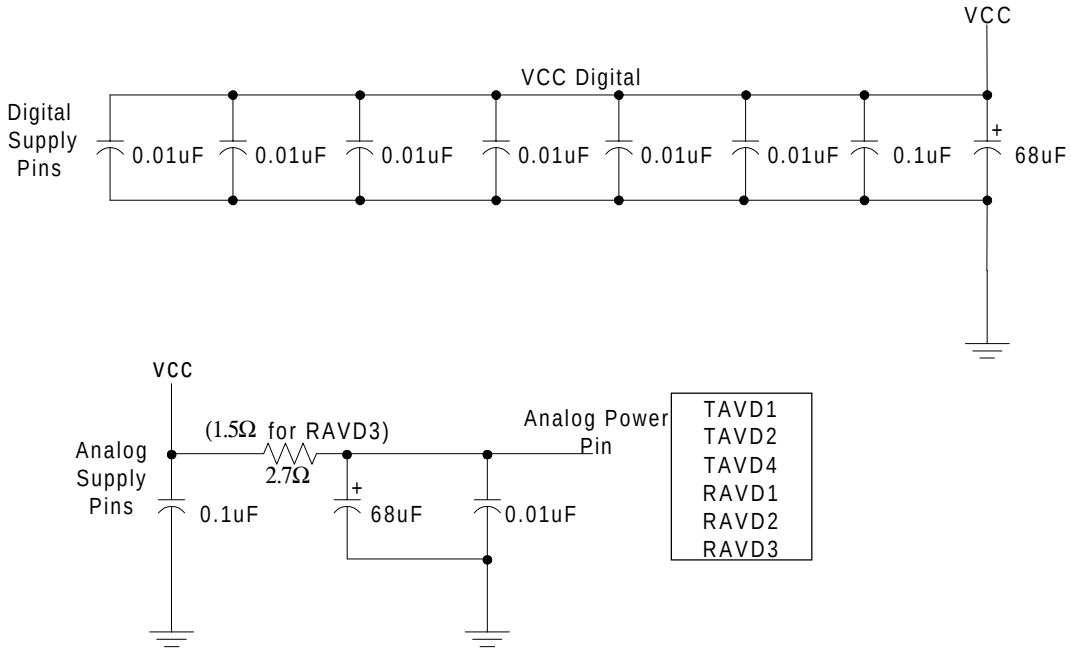
Instantaneous current (I) depends on the capacitive load of each output. The duration of the switching current depends on the capacitive load. The digital signals of the S/UNI-ULTRA Reference Design uses approximately 75 Ohm traces. When an output switches initially, it sees 75 Ohm characteristics impedance and its output series resistance. As the load charges up exponentially, the amount of current required decreases until it reaches a steady state. To calculate the largest current demand of an output, one must know the its output impedance. However, for CMOS device, the output impedance changes as the output changes. As an approximation, a S/UNI-ULTRA output will require 50 mA of switching current for charging charge a 50 pF load from 0 to 5 volts in 5ns.

Using this figure, for a Vcc pin supplying 4 outputs, each of which requires 50 mA for 5 ns, and a maximum allowable voltage spike of 100 mV, the capacitance required is 4 * 50mA * 5ns / 100mV = 0.01 uF. A 0.01 uF capacitor can be used in this case.

4.4.3 S/UNI-ULTRA and LASAR-155 Decoupling

All of the sensitive analog power supply pins of the S/UNI-ULTRA on board employs a 2.7 Ohm resistor and a 4.7 uF capacitor to filter out low frequency Vcc noise. A 0.01 uF decoupling capacitor is placed near each analog Vcc pin. A 0.01 uF decoupling capacitor is also placed near each digital power pin. Since one ground plane is used in this reference design, the analog grounds shown in the diagram below refers to ground section near the analog circuitry.

Figure 13 - Power Pin Decoupling



Analog circuitry draws a mostly constant current and requires little switching current (i.e. for internal oscillators of the CRU and CSU). The 2.7 Ohm and 68 uF pair form a low pass filter to filter out low frequency noise. A 0.1 uF capacitor is placed to provide a low impedance path to digital ground for digital noise on the Vcc plane. The 0.01 uF decoupling capacitor is placed as close to the analog power pin to minimize switching noises. A 0.01 uF decoupling capacitor is also placed as close to each digital power pin as possible. Ferrite beads are not used on the digital power pins because they add series inductance which limits the current that is required to recharge the decoupling capacitors. If noise attenuation is required, a small surface mount series resistor (1 to 10 Ohms) can be added in series with the power pin.

Bulk decoupling is provided for both the S/UNI-ULTRA's Vcc island and LASAR-155's Vcc island. The total amount of local decouple and bypass capacitance for the S/UNI-ULTRA's circuitry is approximately 2.2 uF (25 x0.01uF + 20 x 0.1 uF). Therefore, the value of its bulk decoupling capacitor must be at least 25 uF. The LASAR-155's decoupling amounts to approximately 0.5 uF, requiring a bulk decoupling capacitor of at least 5 uF. A 0.1 uF bypass cap is also placed near each bulk capacitor to provide additional filtering.

4.4.4 RAVD2 Analog Power-up ramp rate REQUIREMENT at low temperature

Description

The analog supply voltage (RAVD2) requires a minimum voltage ramp rate during up power up. If the power ramp is too slow the S/UNI ULTRA will be unable to lock to received data. The required ramp rate is a strong function of temperature, as shown in Table 1.

Table 1 Maximum RAVD2 Power-up Ramp Time vs. Temperature

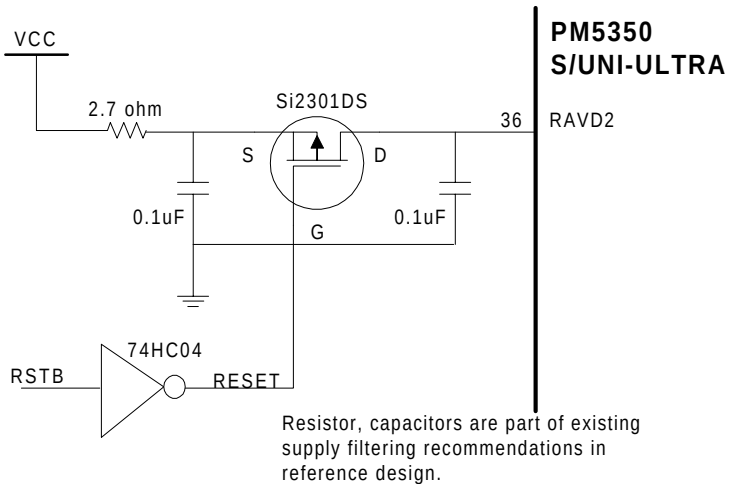
$T_{ambient}$ (°C)	Maximum Ramp Time Requirement (10% to 90% voltage ramp)
25	50ms
0	1ms
-40	1µs

Devices that are not powered up correctly will recover normal operation when the ambient temperature rises. Once operating normally, a device will continue to operate normally over the full rated temperature range.

Recommendation

Some board-level power supplies cannot provide the required voltage ramp rates for proper operation at 0°C or –40°C, so an external circuit is needed to gate the power to RAVD2. A recommended circuit is given below.

Figure 14 RAVD2 Voltage Ramp Up Fix



The RESET signal is a standard CMOS signal: 0 to 5V swing with t_{rise} and t_{fall} <20ns. During device power-up, RESET must be held active (high) for at least 10ms to allow the capacitors to discharge. Then, when RESET is brought low, the device will begin operating normally.

Please contact the PMC-Sierra Applications department for more information.

Performance with Recommendation

All devices will power-up correctly over the entire industrial temperature range (-40 to 80°C).

Performance without Recommendation

Upon power-up at low temperature, some devices may not lock to reference clock (RROOLV=1 in register 08h) and to data (RDOOLV=1 in register 80h). In this condition, the reference clock output (RCLK, pin 55) may be DC or very low frequency.

4.5 QAVD & QAVS

The QAVS and QAVD pins are used internally for isolation purposes. They draw virtually no current. Nonetheless, they should still be treated like analog power supply pins with filtering and decoupling.

Since one pair of QAVS & QAVD pins is located in the transmit side, while the other pair is located in the receive side, and they are internally connected together, an internal connection between the transmit analog Vcc/ground and receive analog Vcc/ground exist. Therefore, it is not advised to separate transmit and receive analog power supplies. Furthermore, even when a single Vcc plane and Ground plane are used, care must be taken to ensure that both QAVD pins are at the same voltage level and both QAVS pins are at the same ground level.

4.6 Routing

- All power and ground traces are as wide and short as possible to minimize trace inductance.
- All high speed traces are routed over continuous image planes (power or ground planes).
- All traces carrying transmit and receive line rate data are transmission lines with 50 Ohm controlled impedance. These traces should be routed on the same side and kept as short as possible.

- Both signals of a differential pair are of equal length and routed close to each other.

- All PCI signal traces have an impedance of 75 Ohms +/- 10%.

- All UTOPIA interface signals are also 75 Ohms +/- 10%. For each of the UTOPIA interface signal, a series termination resistor is added at each output. The value of the series termination at the source depends on the source impedance. Basically, the sum of the values of the series resistance of the output driver and the series termination resistor should be equal to the trace impedance which is 75 Ohm in this case. In addition, a 75 Ohm series resistor is also added at the input to absorb any reflection at the load. Note that these resistors will slow down the output edge rates which can lead to reduction in emission; However, they do increase the prop delay of the signals due to the slowing down of the edges.

- S/UNI-ULTRA's reference clock signal is also 75 Ohm with source and load series termination resistor. Ground guard traces are routed adjacent to the clock trace to prevent crosstalk.

- The PCICLKO output of the LASAR drives 3 parallel 75 Ohm traces (to SYSCLK input of the LASAR-155, and TFCLK and RFCLK inputs of the S/UNI-ULTRA), each with matched source and load series termination.

4.7 PCI Bus Signal Specification

This layout follows the PCI Rev. 2.0 Specification layout restrictions. **The PCI SIG specification has stringent and detailed rules on decoupling, power consumption, trace length limits, routing, trace impedance, as well as signal loading. Therefore, it is essential to check the latest PCI specification before proceeding with new designs and layouts**.

The S/UNI-ULTRA reference design board conforms to the following PCI Specification/Recommendations:

- Component height on the component side does not exceed 0.570 inches, and on the solder side does not exceed 0.105 inches.

- PCI CLK signal trace is 2.5 inches +/- 0.1 inches and is connected to only one load.

- All 32-bit interface signals have the maximum trace length of 1.5 inches.

- Trace impedance for shared PCI signals are within 60 - 100 Ohm range, and trace velocity is between 150 and 190 ps/inch.

- 20 mil wide traces are used to connect the power and ground pins on PCI connector to their respective planes and the trace lengths are limited to 250 mil.

- Route all traces over continuous image planes. Where traces have to cross planes, at least one 0.01 uF capacitor per four signals (located within 250 mil) is across the two planes.

- At least 0.01 uF of decoupling capacitance per Vcc pin.

4.8 Emission

EMI can be reduced via proper routing, decoupling, power and ground distribution, shielding, and filtering. Most of the additional measurements list below for EMI improvement also lend themselves towards improving system level performance.

4.8.1 Additional Routing Rules

Proper decoupling and termination are effective ways of reducing EMI. In addition to the above-mentioned routing and termination rules, the following are some rules which will help reduce EMI:

- Data lines should be kept away from the clock signals to avoid noise coupling.

- No high speed signals should be routed near the vicinity of the RJ45 modular jack and the transformer in order to prevent common-mode noise coupling onto the cable.

- Cuts on power and ground plane may increase BER performance of the board. In some cases, however, they may cause large return current loops. In particular, if the differential signal pair crossing the cuts are not balanced (i.e. not all of the current transmitted on one trace will return via the other trace of the pair), the difference current will have to seek alternative return path to the source. With cuts on the image plane (i.e. ground or power plane), this return current will have to find a path around the cut, resulting in a large return current loop which can pick up as well as radiate noise, and cause crosstalk onto other signals. Therefore, use one solid ground plane and Vcc plane when possible.

- Footprints of capacitors can be placed along signals with fast rise and fall times. In the event that fast edges causes excessive EMI, they can be slowed down using these capacitors.

4.8.2 Power and Ground

- It's best to have only one power and one ground plane as long as the ULTRA's analog pins are decoupled as per this document. If more planes or cuts are implemented, then here is some guidelines to follow:
- The power plane should be kept away from the RJ45 modular jack and the transformer to prevent noise coupling.
- When separate power planes are used, keep the power planes away from each other. Ensure that for each section of the power plane, there is a ground plane of larger size underneath. The larger ground plane, plus the physical separation of the power planes, will reduce the return current or noise from fringing into adjacent planes. Power planes should also be kept away from the edge of the board to prevent noise fringing between the power and ground planes at the edge of the card and causing unwanted emission.
- Ensure that power and ground planes of different sections do not overlap in order to prevent noise coupling.
- Provide a chassis ground plane under the RJ45 modular jack.

5 COMPONENT SELECTION

5.1 Transformer

The following transformers are recommended:

- Belfuse S558-5999-42 Tel: 510-227-0102
- Valor ST6114 Tel: 800-31-VALOR
- Pulse Engineering PE68517 Tel: 619-674-8100

Many other manufacturers produce datacomm transformers that are suitable for this application. The transformer provides the common-mode rejection, line isolation, and additional filtering; therefore, choosing the right transformer is critical in meeting ATM Forum specification as well as various emission standards. When qualifying a transformer, all relevant parameters should be considered. The following sections provide some guidelines on how to qualify a transformer.

The following is a typical transformer specification sheet:

Part Number	Insertion Loss (dB) Typical	Return Loss (dB) Min		Rise Time (ns) Typ 10% - 90%	Common to Differential Mode Rejection (dB) Min	Common to Common Mode Rejection (dB) Min	Inductance OCL (uH) Min	Hipot (Vrms) Min
		100K - 30MHz	30MHz - 80MHz		100KHz - 155MHz	100KHz - 155MHz	@ 8mA DC Bias	
xxxxxx	-1.0	-16	-10	2.5	40	30	350	1500

5.1.1 Insertion Loss

Insertion loss refers to the amplitude attenuation of the signal due to the bandpass nature of transformers. All transformers exhibit insertion loss. Typically, the transformers will have an insertion loss of 0.2dB at 1MHz, and 0.6 dB at 77 MHz. As frequency goes up, the insertion loss increases linearly up to a point where it starts to increase much more rapidly. Although insertion loss is not explicitly specified by the ATM Forum, its effect can be seen on the AOI output amplitude measurements. Note that the S/UNI-ULTRA can compensate for this insertion loss by allowing the user to adjust transmit output currents. The insertion loss requirement is indicated in the S/UNI-ULTRA datasheet.

5.1.2 Return Loss

Return loss refers to the impedance mismatch at a junction. Impedance mismatch causes reflection which can lead to additional emission. The smaller the return loss, the better matched the transformer. ATM Forum specification has the following return loss requirement:

Return Loss	Frequency Range
> 16 dB	2 MHz - 30 MHz
> 16 dB - 20*log(f/30 MHz)	30 MHz - 60 MHz
> 10 dB	60 MHz - 100 MHz

5.1.3 Rise Time

ATM Forum requires the output rise time to be greater than 1.5ns and less than 3.5ns. Since signals with sharp edges are rich in high frequency harmonics and will produce higher level of emission, the slowest possible edge rate within the ATM Forum specification is desired. The overall rise time at AOI can be approximated as follows:

$$\text{Ove rall Rise Time} = \sqrt{(\text{Tr\_ultra}^2 + \text{Tr\_transformer}^2)}$$

Allowing some margin, the desired transformer rise time should be less than 2.5 ns.

5.1.4 Common to Differential Mode Rejection

Common-mode signals riding on the TXD+/- signal traces may be converted to differential signals which are then added to the actual data. The transformer will not reject the differential noise on top of data. This differential noise will interfere with the receiver's ability to recover data, as well as altering the output amplitude on the transmit side (The ATM Forum specification requires the output voltage for UTP-5 cable to be 1 V +/-6%) causing non-compliance. Therefore, the greater the common to differential rejection the better.

A typical common-mode rejection is -32 dB.

5.1.5 Common to Common Mode Rejection

Once common-mode signals getting onto the twisted pair cable, they do not have any opposing field to cancel them and will radiate. Therefore, it is critical to minimize the common-mode signal before it gets onto the cable. The S/UNI-ULTRA's outputs, like many other UTP-5 transceivers, terminate via 50 Ohm to analog power rail. Any noise on the power rail (which is very likely) will go through the 50 Ohm resistor and

ride on the data signal via the TXD+/- signal traces to the transformer. Furthermore, crosstalk from nearby signals could also induce noise on the TXD+/- signal traces. Since the TXD+ trace is routed and terminated in close vicinity of TXD- trace, crosstalk and power rail noise introduced on one will likely be on the other as well.

On the transmit side these common-mode signals can be suppressed using common-mode choke on the Tx transformer input. As noise frequency can vary from system to system, the ideal transformer should have large common-mode rejection over all frequency ranges. Some vendors may extend this specification further to have 30 dB of common-mode rejection up to 500 MHz. The recommended transformers also contain a second common-mode choke on the output side of the Tx transformer. This common-mode choke reduces common-mode signals that may be traversing on the cable back to the Tx transformer.

On the receive side, a similar common-mode choke should be applied on the input side of the Rx transformer. Without the common mode choke, the common-mode noise can affect the receiver input noise margin as the actual data amplitude can be very small after 100 meters of cable. Furthermore, large common-mode noise may also permanently damage to the receiver may occur.

The typical value for common-mode reject for both transmit and receive side from 100KHz to 155MHz is 30 dB. The higher the common-mode reject and the wider the frequency range, the better the transformer.

An added benefit of common-mode to common-mode choke is that common-mode impulse noises (fast transients) of up to 500 V are also attenuated significantly.

5.1.6 Differential to Common-mode Rejection

Imbalance in the transformer will cause differential mode signal to be converted to the common-mode signal which will cause emission once get onto the cable. The differential to common-mode signal rejection should be better than -32 dB.

5.1.7 Open Circuit Inductance (OCL)

In order to meet the baseline wander requirement of the ATM Forum Specification, the minimum required OCL of the transformer should be 350 uH.

5.1.8 Isolation Voltage (Hipot)

Isolation (or Hipot) refers to the transformer's ability to withstand a high voltage without breaking down (shorting). All transformers recommended in this document have isolation voltage of at least 1500 Volts. Although not explicitly required by the

ATM Forum, the fast transient immunity guideline implicitly requires the transformer to be able to withstand at least 500 Volts because the guideline requires the system to be able to recover from 0.5 kV impulse noises (fast transients) without operator intervention (IEC 801-4 Level 2).

5.1.9 Separate or Duplex Transformer Packages

All transformers recommended in this document are duplex packages that have transmit and receive transformers in the same package. The advantage of using a duplex transformer is its compactness. The disadvantage, however, is the possibility of crosstalk between the tx and rx transformers when they are packaged together. Therefore, when using duplex transformers crosstalk characteristics must be considered. Separate transmit and receive transformer packages, on the other hand, will have minimal crosstalk.

Typical crosstalk is -35dB minimum at frequencies from 100KHz to 155MHz.

5.2 RJ45 Modular Jack

Any 8-pin 8 position RJ45 modular jack can be used. There are three types of modular jacks:

- non-filtered and non-shielded
- shielded and non-filtered
- shielded and filtered (capacitive filtering or inductive filtering)

A shielded and non-filtered jack is used in the reference design. In order for the shielding to be effective, the shield should be electrically connected to the chassis ground via a low impedance connection (i.e. using copper finger stocks or firm mechanical contact with the mounting bracket). Typically, the shielded portion of the jack will extend through the opening in the mounting bracket and make firm mechanical contact with the bracket on all sides.

The following vendors provide RJ45 connectors:

- Stewart Connectors 717-235-7512
- AMP 800-522-6752
- Kycon 800-544-6941
- Power Dynamics 201-736-5722

5.3 Optics Interface Module

Any 9X2 optical multi-mode or single-mode transceiver module can be used.

5.4 Oscillator

The on-board oscillator provides a timing reference for the transmit clock synthesis circuitry as well as the receive clock and data recovery circuitry. It should have a stability of at least +/-100 ppm for ATM user device and +/-20 ppm for ATM network device. The stability figure of an oscillator should include any variation due to calibration, temperature, voltage, load, aging, shock, and vibration, and is specified over the lift time of the oscillator. Either CMOS or TTL oscillator can be used. The following are some vendors that provide these oscillators:

Vendor	+/-20ppm or better	+/-100ppm
Motron Industries 605-665-9321	Yes	Yes
Connor Winfield 708-851-4722	Yes	Yes
K&L Oscillatek	Yes	Yes
Champion 847-451-1000	Yes	Yes
Oak Frequency Control 717-486-3411	Yes	Yes
Ecliptek 714-433-1200	Yes	Yes

5.5 Bandgap Reference Generator

The bandgap reference generator used is a Analog Device AD1580 Precision Shunt Voltage Reference. An external 3.01 KOhm (1%) resistor is used to set up a reference current for the AD1580. Any bandgap reference generator that produces 1.23V +/- 3% output can be used with the S/UNI-ULTRA. In selecting the bandgap reference generator, one must pay attention to the output voltage (1.23V) dependency on the following parameters to ensure the worst case specification will still satisfy the +/-3% accuracy requirement:

- temperature
- input/supply voltage variation
- input reference current variation
- output loading
- output noise

Other similar reference generators that can also be used are:

- Analog Device's AD589JH (Tel: 617-329-4700)
- National Semiconductor's LM385BXZ, package type TO-92 (other packages of the same device do not have the same accuracy) (Tel: 800-272-9959)

5.6 SAR

The PM7375 LASAR-155 device is used as it provides a UTOPIA interface that is directly compatible with the S/UNI-ULTRA's. The LASAR-155 implements a physical layer as well as AAL5. The physical layer portion of the device is bypassed and only the AAL5 functions are used.

5.7 Decoupling and Bypass Capacitors

The total amount of local decouple and bypass capacitance (exclude the PCI Bus power supply decoupling) is approximately 2.75 uF (75 x0.01uF + 20 x 0.1 uF). A 68 uF tantalum capacitor is sufficient as a bulk decoupling (rule of thumb requires at least 27.5 uF bulk decoupling).

The 0.01 uF local decoupling capacitor must have low series inductance and must have a resonant frequency close to the system clock rate. In this case, it is 33 MHz. For the analog side of the S/UNI-PLUS, the same 0.01 uF decoupling capacitors may also be used.

5.8 Resistors

The following resistors must be 1%, 1/10 Watt:

- TRREF resistor
- TXD+/- termination resistors
- RXD+/- termination resistor
- Series resistor used by AD1580
- All series termination resistors such as those used on REFCLK signal and UTOPIA bus signals.

The following resistors can be 5%, 1/10 Watt:

- All pull-up and pull down resistors

6 APPENDIX A: BILL OF MATERIAL

NO.	COMPONENT DESCRIPTION	Package Type	REF DES	Qty
1	PM5350 S/UNI-ULTRA	PQFP128	U2	1
2	8 BIT NON-INVERTING BUFFER, 74HC541	SOIC20W	U1	1
3	PRECISION VOLTAGE REFERENCE GENERATOR, ANALOG DEVICES, AD1580	SOT23	U5	1
4	CAPACITOR, 0.01UF, NPO	SMDCAP805	C3, C30, C31, C34, C35, C40, C47, C50, C53, C65-C71, C76, C77, C84-C88, C92, C94, C95, C99,C5-C7, C10, C13, C14, C16-C27, C29, C36, C38, C41, C43, C45, C46, C51, C52, C54, C56, C57, C59-C61, C72-C75, C81-C83, C89-C91, C96-C98, C101, C103, C105, C107-C112, C114, C116, C127	85
5	CAPACITOR, 0.047UF, X7R	SMDCAP1206	C102, C104, C106	3
6	CAPACITOR, FOR TESTING PURPOSES ONLY, VALUE TO BE DETERMINED	SMDCAP1206	C11, C28	2
7	CAPACITOR, 500 V MIN. 0.01 uF MIN., X7R, MURATA GRM43-4X7R104K500AB	SMDCAP1812	C1, C4	2
8	CAPACITOR, 0.1UF, X7R	SMDCAP1206	C2,C8,C9, C37, C39, C42, C44, C48, C49, C55, C62,C64, C79, C100, C113, C117, C119, C121-	28

NO.	COMPONENT DESCRIPTION	Package Type	REF DES	Qty
			C126, C128, C134, C135, C138, C139	
9	CAPACITOR-10UF, 10V, TANTALUM	EIA-SIZE C	C133, C136, C140	3
10	CAPACITOR-47PF, NPO	SMDCAP805	C63, C78	2
11	CAPACITOR, 68UF, 6.3V MINIMUM, TANTALUM	EIA-SIZE D	C58, C80, C93, C115, C118, C120	6
12	CAPACITOR, FOR TESTING PURPOSES ONLY, VALUE TO BE DETERMINED	SMDCAP805	C12, C15, C32, C33	4
13	FERRITE BEAD, FAIRRITE, SURFACE MOUNT BEADS, 2743019447	SURFACE MOUNT BEAD_1	L2, L3, L5-L8, L11, L12	8
14	TRANSFORMER, VALOR, ST6114	SURFACE MOUNT 16 PINS	T1	1
15	LASAR-155, PMC-SIERRA	PQFP208	U3	1
17	OSC_TTL_DIP-19.44MHZ , 20 PPM, CHA, K1110CA	CRYS14	Y1	1
16	Fiber Optics transceiver, HP HFBR5205	PMD SOCK ET	U7	1
18	OSCILLATOR, 20 PPM, CONNOR WINFIELD, H54-19.44MHZ OR EQUIVALENT	CRYS14	Y1	1
19	RESISTOR-100, 5%	SMDRES805	R9	1
20	RESISTOR-2.7, 5%	SMDRES805	R38, R43-R46	5
21	RESISTOR-270, 5%	SMDRES805	R39, R40	2
22	RESISTOR-3.01K, 1%	SMDRES805	R16	1
23	RESISTOR-332, 1%	SMDRES805	R10, R19, R22	3
24	RESISTOR-4.7K, 5%	SMDRES805	R13, R14, R17, R23, R27	5
25	RESISTOR-49.9, 1%	SMDRES805	R5,R6,R18, R20, R24, R25, R29-R32, R34-R36, R41, R42	15

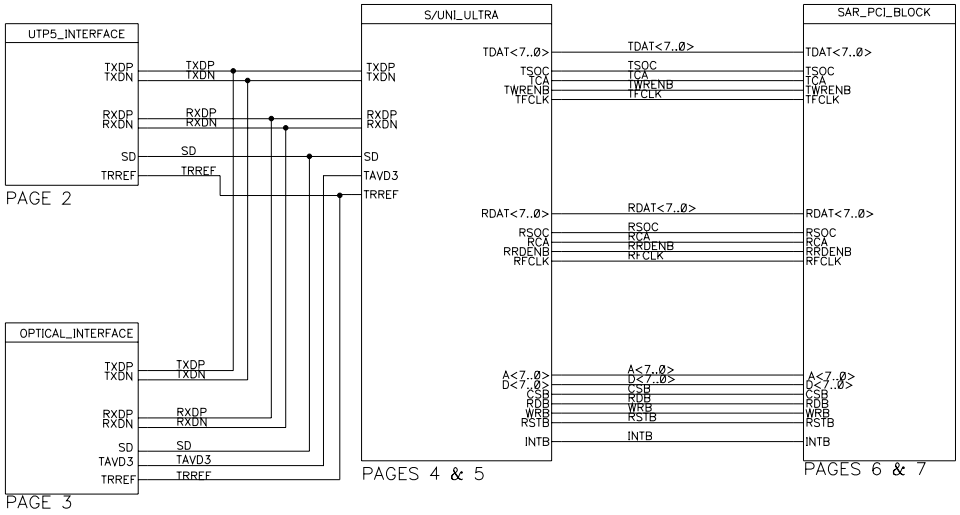
NO.	COMPONENT DESCRIPTION	Package Type	REF DES	Qty
26	RESISTOR-510, 5%	SMDRES805	R33, R37	2
27	RESISTOR-63.4, 1%	SMDRES805	R26	1
28	RESISTOR-75, 5%	SMDRES805	R1,R2,R3, R8, R11, R12, R28	7
29	RESISTOR-909, 1%	SMDRES805	R7	1
30	RESISTOR, FOR TESTING PURPOSES ONLY, VALUE TO BE DETERMINED	SMDRES805	R4, R15, R21	3
31	RESISTOR ARRAY, 15 RESISTORS IN ONE PACKAGE, 4.7 KOHM EACH	SOIC16	RN1, RN14, RN16	3
32	CHIP RESISTOR ARRAY, 4 RESISTORS IN ONE PACKAGE, PANASONIC, EXB-V8V47JV	RN4	RN5-RN7	3
33	CHIP RESISTOR ARRAY, 4 RESISTORS IN ONE PACKAGE, PANASONIC, EXB-V8V68JV	RN4	RN2-RN4, RN8-RN13	9
34	RESISTOR ARRAY, 8 RESISTORS IN ONE PACKAGE, 4.7 KOHM EACH	SOIC16	RN15	1
35	RJ45 MODULAR JACK, 8 PIN, 8 POSITION, PCB MOUNT	RJ45_SHIELD	J1	1
36	SMA CONNECTORS FOR TESTING PURPOSE ONLY	SMA	J2, J3	2
37	74HC04 inverter	74HC04	U4	1
38	p-channel FET transistor Si2301DS. SOT-23, Vishay Siliconix, www.siliconix.com	Si2301DS	Q1	1

7 APPENDIX B: SCHEMATICS

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

S/UNI-ULTRA REFERENCE DESIGN

DUAL FOOTPRINT LINE INTERFACE: UTP-5 & FIBER OPTIC



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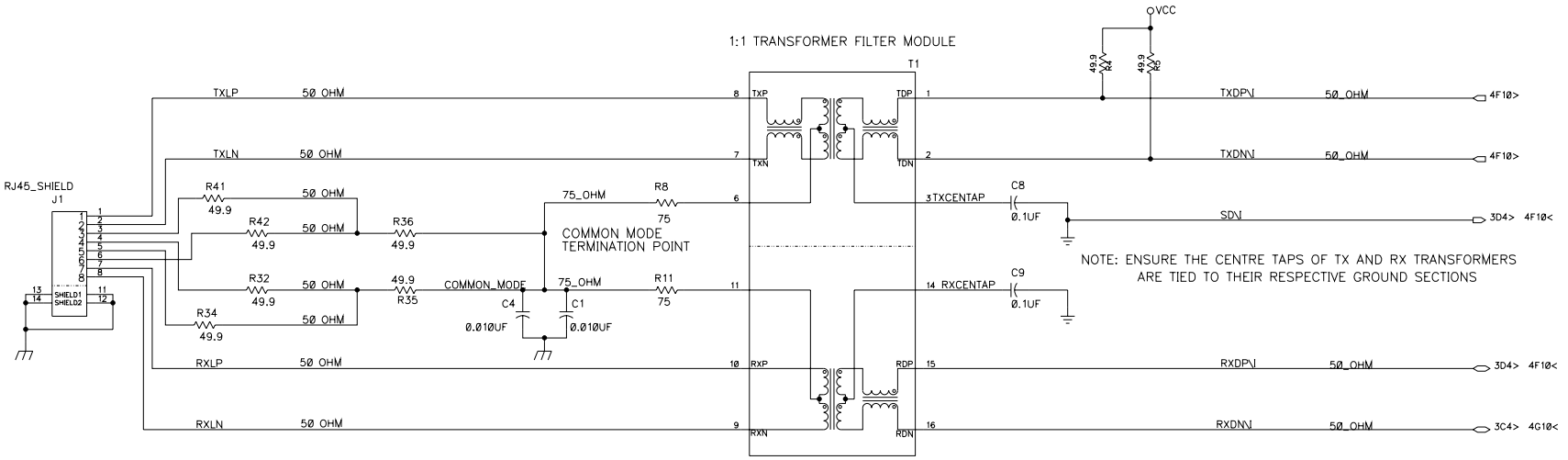
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC961062	ISSUE: 3
TITLE: S/UNI-ULTRA REFERENCE DESIGN ROOT DRAWING	DATE: NOV. 28/97
ENGINEER: WT	PAGE: 1 OF 7

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

S/UNI-ULTRA REFERENCE DESIGN
DUAL FOOTPRINT LINE INTERFACE: UTP-5 & FIBER OPTIC

RJ45 & TRANSFORMER

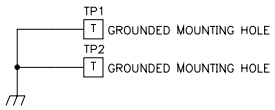


NOTE:
RJ45 IS CONFIGURED AS THAT OF AN ATM USER DEVICE.
PAIRING OF THE CABLES ACCORDING TO ANSI/TIA/EIA-568-A IS AS FOLLOWS:
PIN 1 & 2: PAIR THREE (WHITE-GREEN & GREEN) TXD+/-
PIN 3 & 6: PAIR TWO (WHITE-ORANGE & ORANGE) COMMON-MODE TERMINATION
PIN 4 & 5: PAIR ONE (WHITE-BLUE & BLUE) COMMON-MODE TERMINATION
PIN 7 & 8: PAIR FOUR (WHITE-BROWN & BROWN) RXD+/-

NOTE
CAPS WITH VALUES TBD ARE FOR ADDITIONAL FILTERING
POPULATE ONLY WHEN NEEDED.

NOTE:
THE COMMON-MODE SHOULD ALWAYS BE
AC COUPLED TO CHASSIS VIA TWO HIGH
VOLTAGE CAPACITORS

NOTE:
MOUNTING HOLES FOR PCI BRACKET TO CHASSIS



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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC961062	ISSUE: 3
TITLE: S/UNI-ULTRA REFERENCE DESIGN RJ45 & TRANSFORMER	DATE: NOV. 28/97
ENGINEER: WT	PAGE: 2 OF 7

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

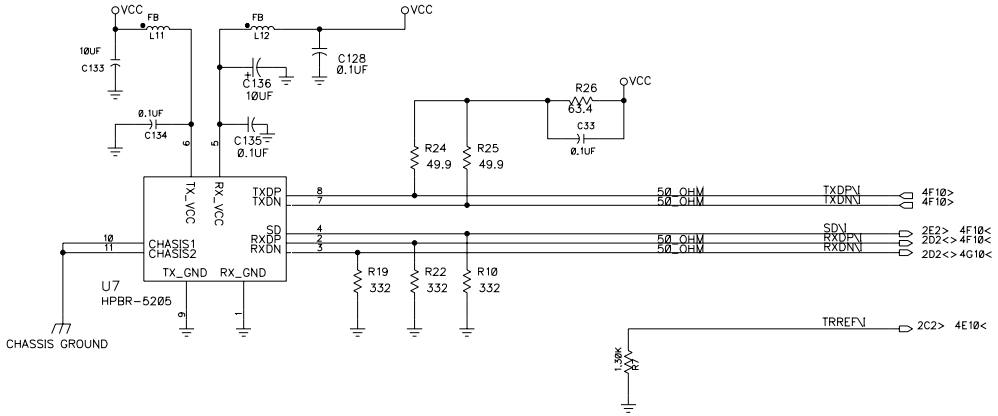
S/UNI-ULTRA REFERENCE DESIGN

DUAL FOOTPRINT LINE INTERFACE: UTP-5 & FIBER OPTIC

OPTICAL INTERFACE

NOTE

PLACE THE TXDP/N TERMINATION RESISTORS CLOSE TO THE OPTICAL MODULE



NOTE:
POPULATE THE ABOVE PARTS IF OPTICAL INTERFACE IS USED

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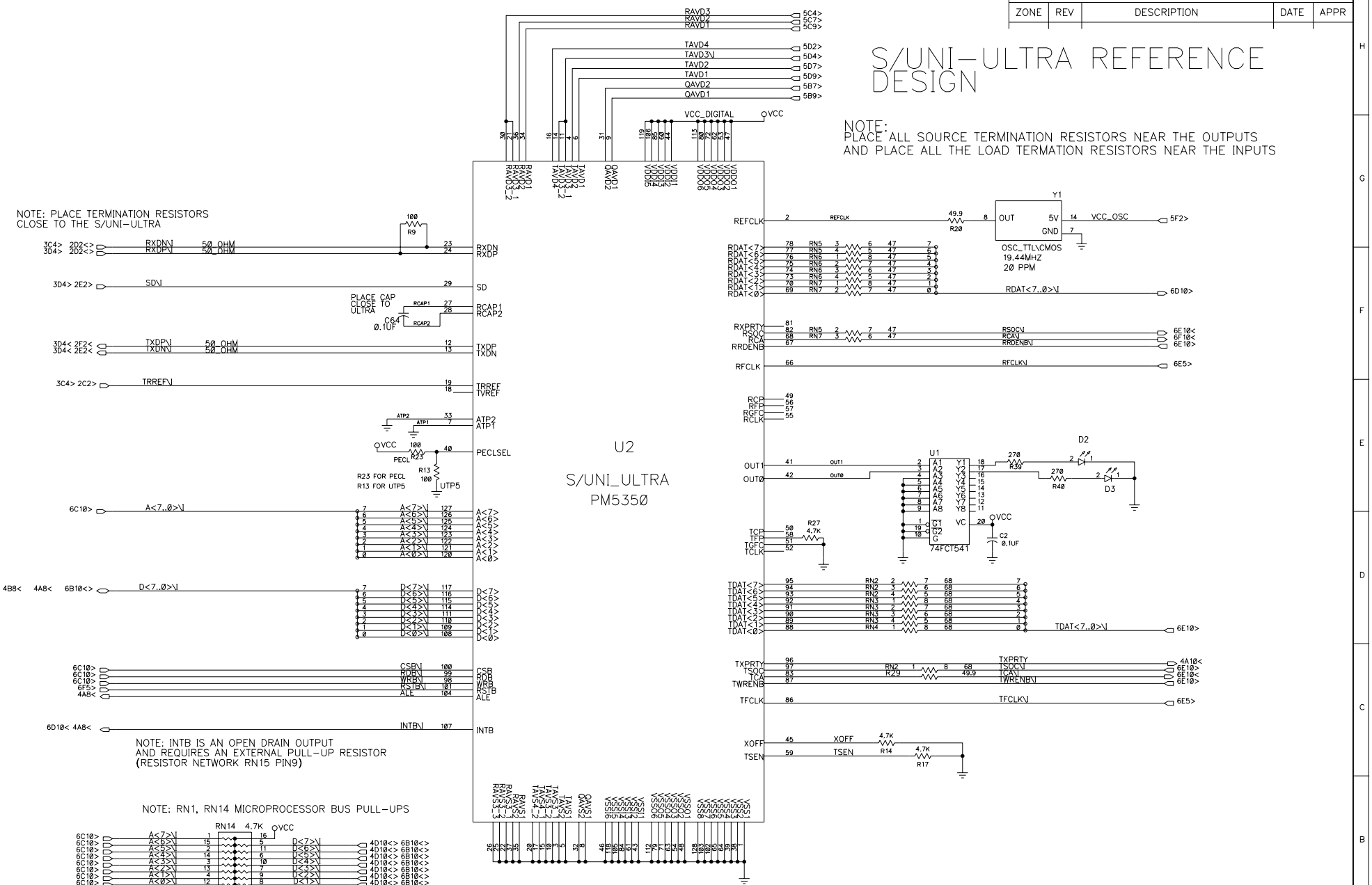
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC961062	ISSUE: 3
TITLE: S/UNI-ULTRA REFERENCE DESIGN OPTICAL INTERFACE	DATE: NOV. 28/97
ENGINEER: WT	PAGE: 3 OF 7

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

S/UNI-ULTRA REFERENCE DESIGN

NOTE:
PLACE ALL SOURCE TERMINATION RESISTORS NEAR THE OUTPUTS
AND PLACE ALL THE LOAD TERMATION RESISTORS NEAR THE INPUTS



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TITLE: S/UNI-ULTRA REFERENCE DESIGN S/UNI-ULTRA	DATE: NOV. 28/97
ENGINEER: WT	PAGE: 4 OF 7

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

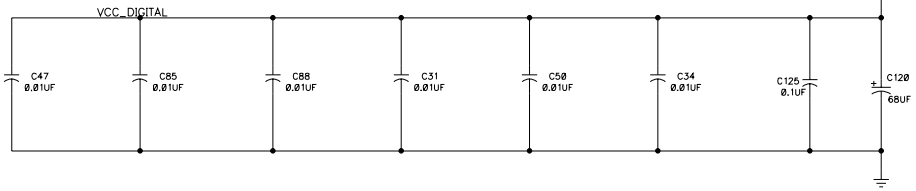
S/UNI-ULTRA REFERENCE DESIGN

DUAL FOOTPRINT LINE INTERFACE: UTP-5 & FIBER OPTIC

S/UNI-ULTRA POWER & GROUND

DIGITAL DECOUPLING CAPS

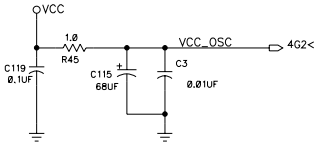
PLACE CAPS CLOSE TO THE VDD PINS OF ULTRA



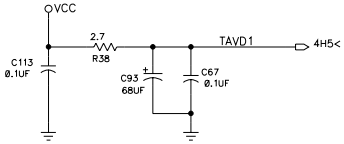
POWER SUPPLY BULK DECOUPLING

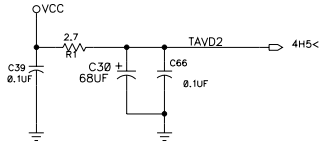
PLACE NEAR THE POWER SUPPLY SOURCE

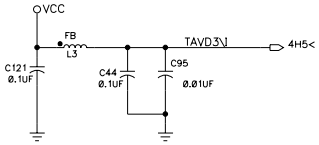
OSCILLATOR POWER SUPPLY

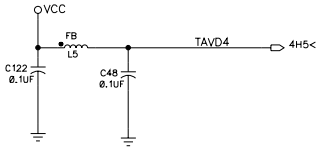


TRANSMIT ANALOG









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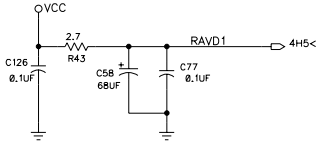

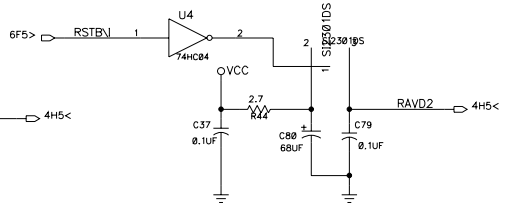

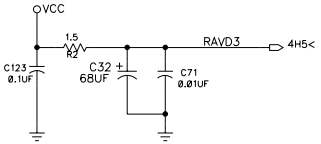

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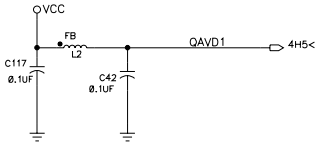

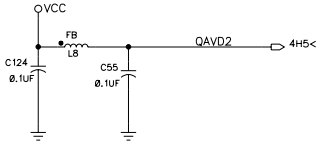

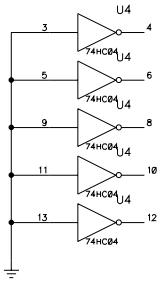

NOTE:

1. QAVD1 & QAVD2 PINS MUST BE TIED TO QUIET ANALOG VCC SECTION AND THEY MUST BE AT THE SAME VCC LEVEL
2. QAVS1 & QAVS2 PINS MUST BE TIED TO QUITE ANALOG GROUND SECTION AND THEY MUST BE AT THE SAME GROUND LEVEL.

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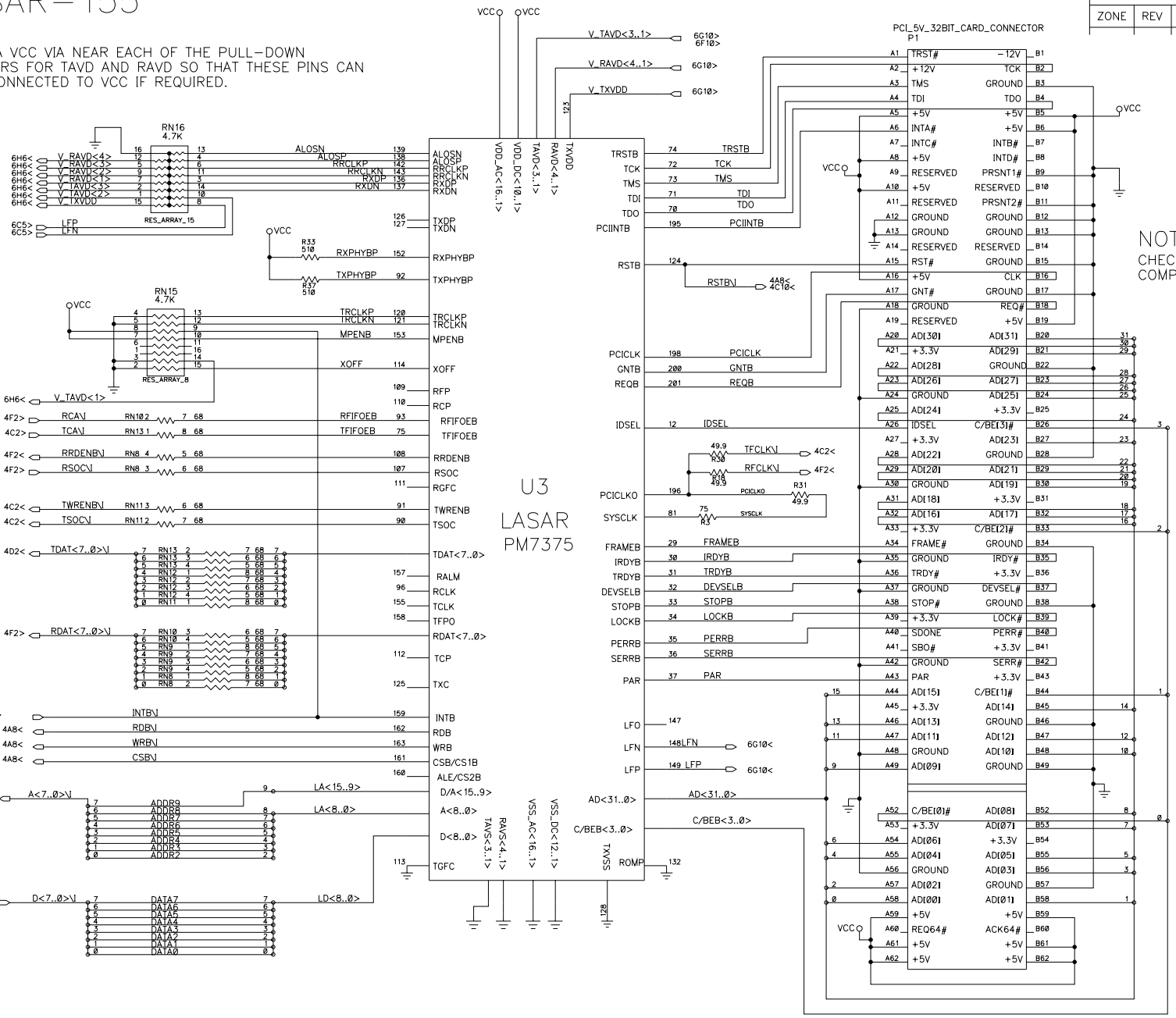
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-961Ø62	ISSUE: 3
TITLE: S/UNI-ULTRA REFERENCE DESIGN S/UNI-ULTRA POWER SUPPLIES	DATE: NOV. 28/97
ENGINEER: WT	PAGE: 5 OF 7

LASAR–155

NOTE:
PLACE A VCC VIA NEAR EACH OF THE PULL–DOWN RESISTORS FOR TAVD AND RAVD SO THAT THESE PINS CAN BE RECONNECTED TO VCC IF REQUIRED.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



NOTE:
CHECK THE LATEST PCI SPEC FOR COMPONENT AND LAYOUT RESTRICTIONS

S/UNI–ULTRA REFERENCE DESIGN
DUAL FOOTPRINT LINE INTERFACE:
UTP–5 & FIBER OPTIC

DRAWING
TITLE=SAR_PCI_BLOCK
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LAST_MODIFIED=Thu May 6 12:25:02 1999

PMC–Sierra, Inc.

DOCUMENT NUMBER: PMC961062	ISSUE: 3
TITLE: S/UNI–ULTRA REF. DESIGN LASAR–155	DATE: NOV. 28/97
ENGINEER: WT	PAGE: 6 OF 7

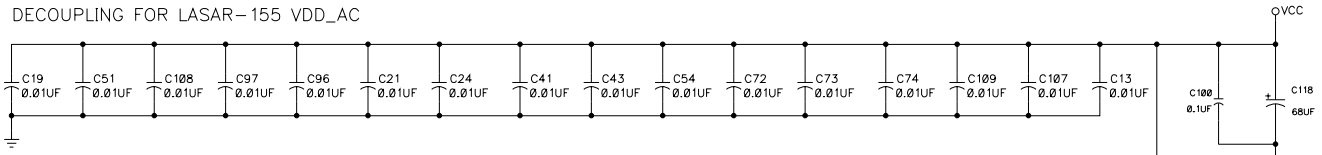
S/UNI-ULTRA REFERENCE DESIGN

DUAL FOOTPRINT LINE INTERFACE: UTP-5 & FIBER OPTIC

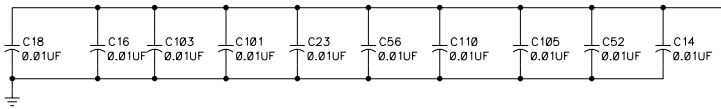
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

POWER SUPPLY DECOUPLING

DECOUPLING FOR LASAR-155 VDD_AC

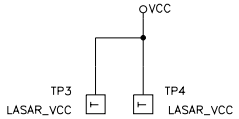


DECOUPLING FOR LASAR-155 VDD_DC

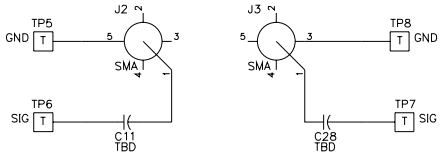


BULK DECOUPLING FOR LASAR_VCC

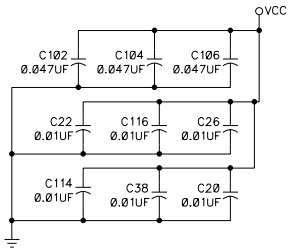
VCC TEST POINTS



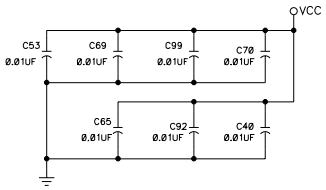
FOR TEST PURPOSES ONLY



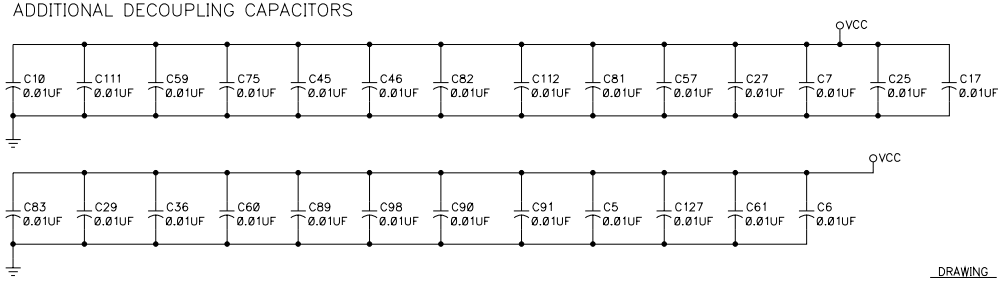
NOTE:
THE FOLLOWING DECOUPLING CAPS ARE USED FOR PCI BUS POWER RAIL. THEY SHOULD BE PLACED IN SUCH A WAY THAT AT LEAST AN AVERAGE OF Ø.Ø1UF PER VCC PIN IS ACHIEVED.



NOTE:
THE FOLLOWING DECOUPLING CAPS ARE USED FOR LASAR POWER PLANE. THEY SHOULD BE PLACED IN SUCH A WAY THAT AT LEAST AN AVERAGE OF Ø.Ø1UF PER VCC PIN IS ACHIEVED.



ADDITIONAL DECOUPLING CAPACITORS



DRAWING
TITLE=SAR_PCI_BLOCK
ABBREV=SAR_PCI_BLOCK
LAST_MODIFIED=Thu May 6 12:25:06 1999

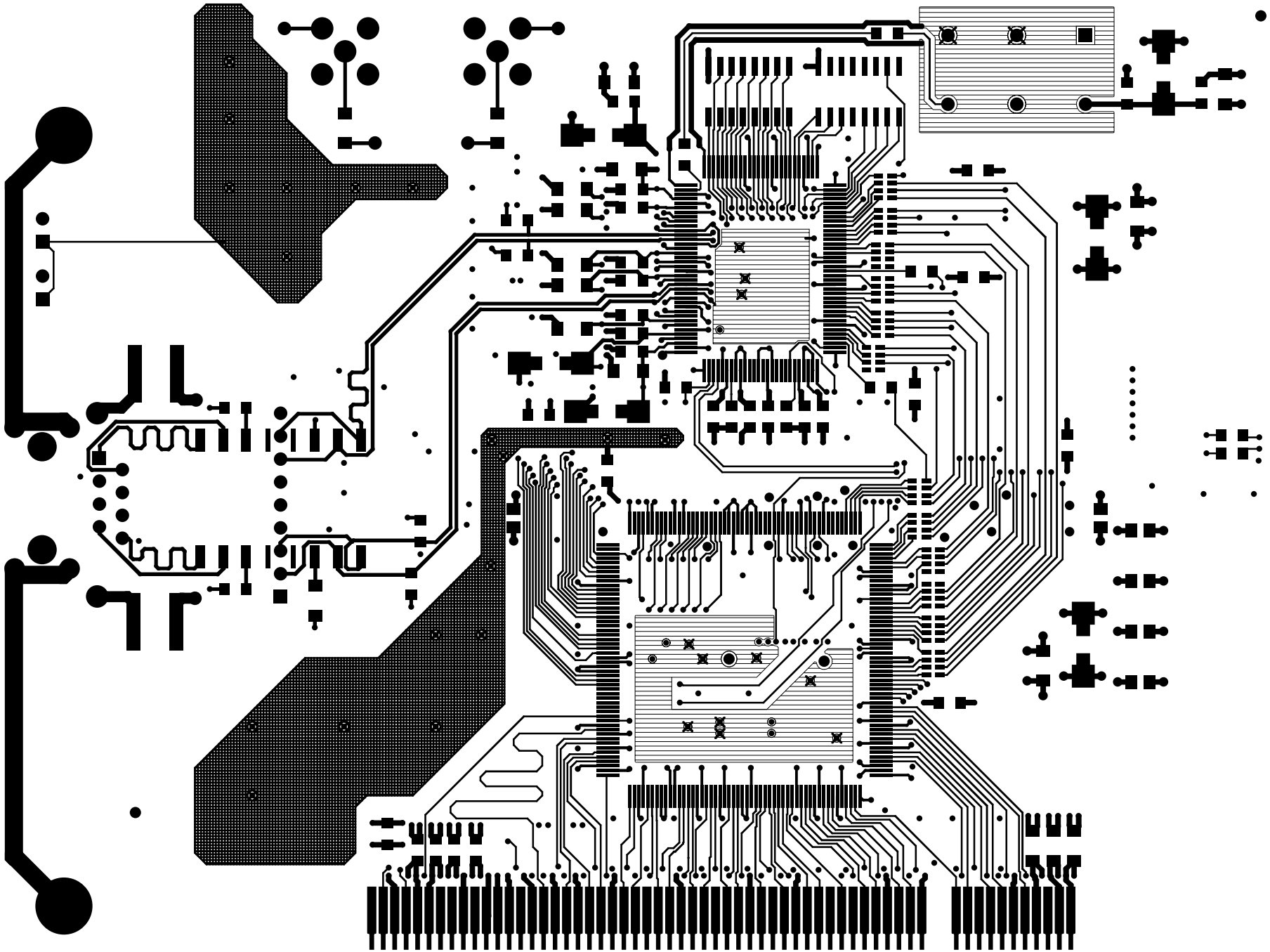
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC961062	ISSUE: 3
TITLE: S/UNI-ULTRA REFERENCE DESIGN POWER SUPPLY & DECOUPLING	DATE: NOV. 28/97
ENGINEER: WT	PAGE: 7 OF 7

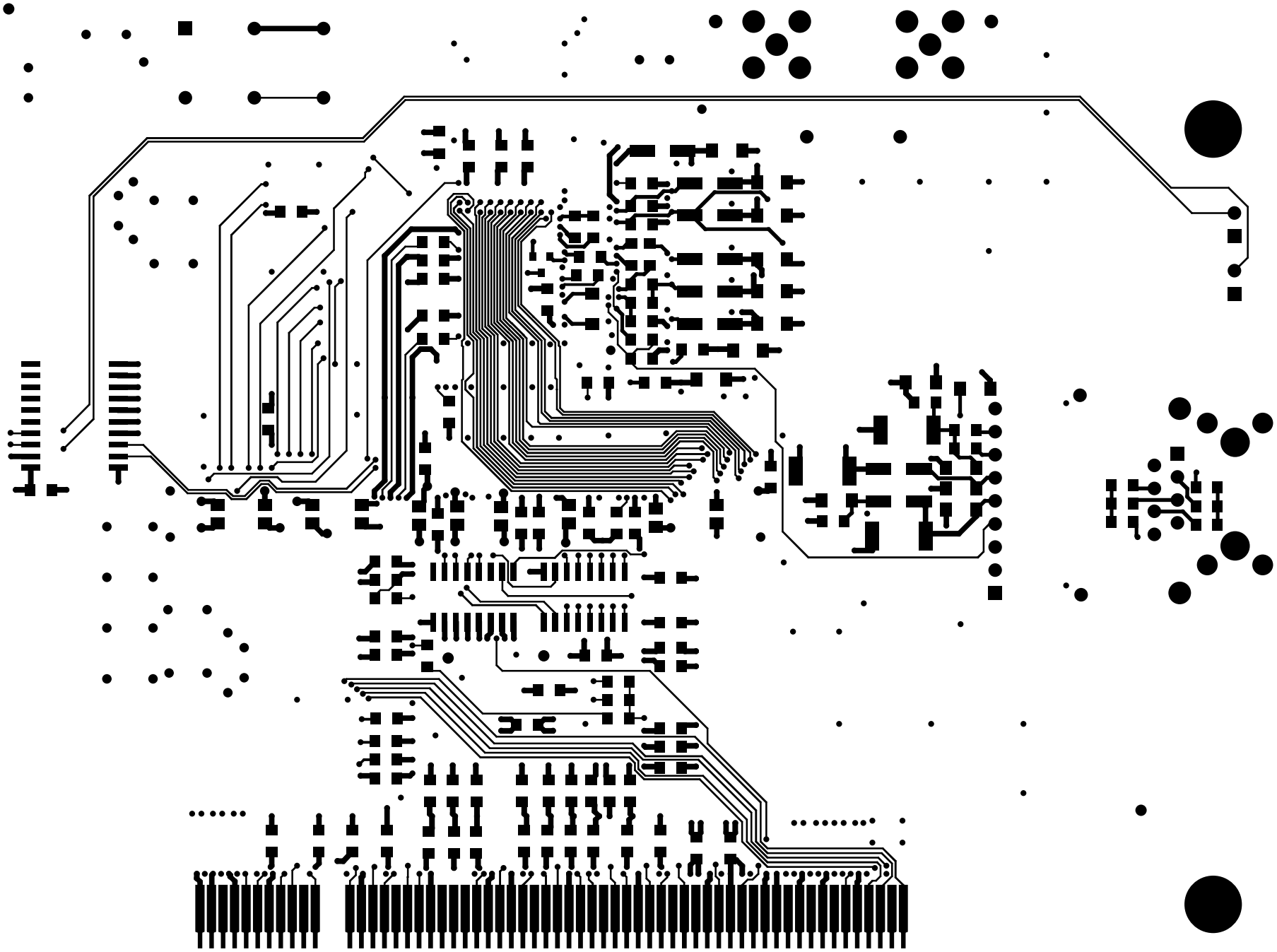
8 APPENDIX C: PCB LAYOUT

There is no Revision 3 PCB layout. Because there were only minor changes to the Rev 2 PCB, a Rev 3 PCB was not done.

TOP LAYER

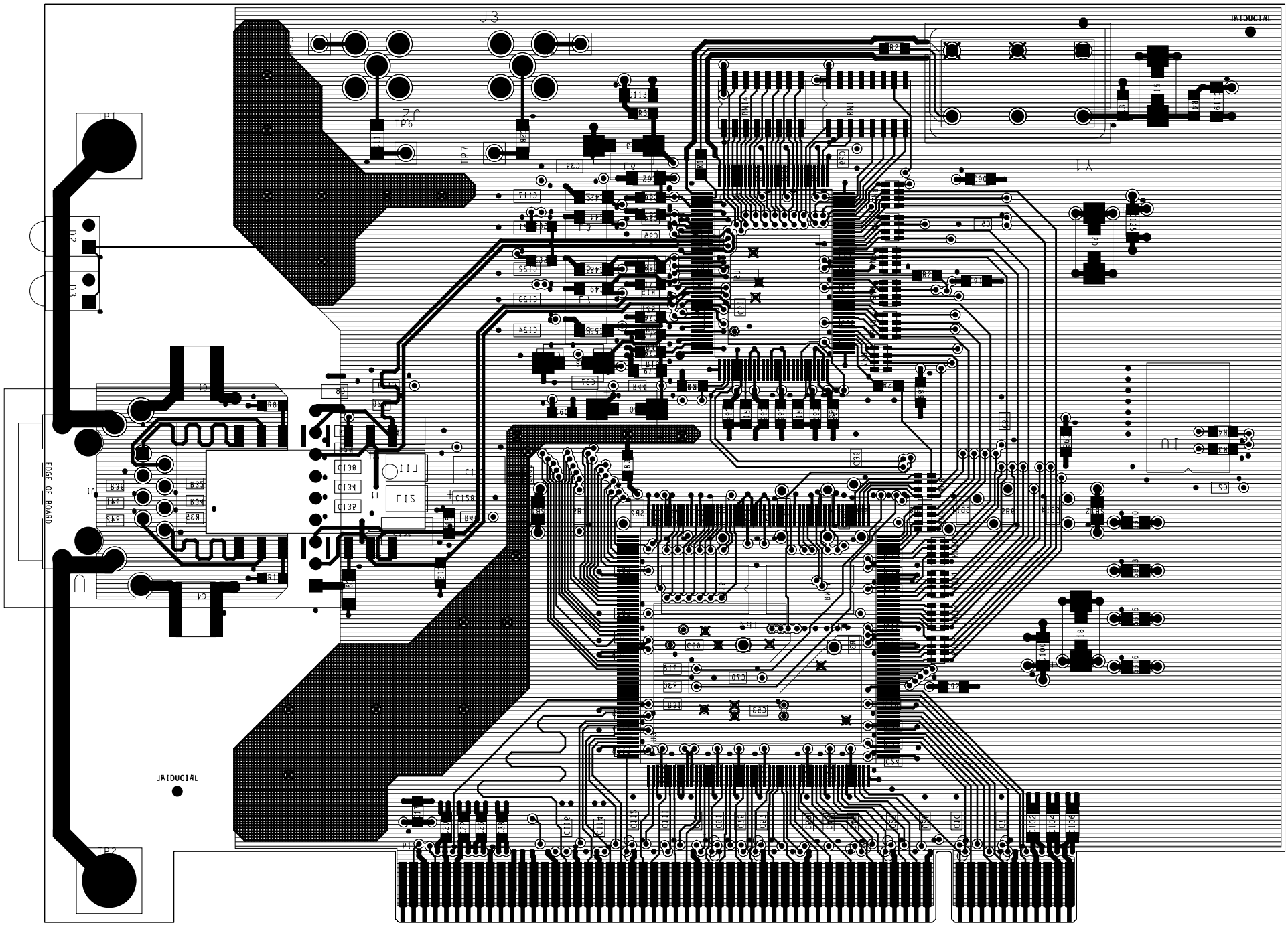


BOTTOM LAYER



GND PLANE

TOP LAYER COMP TOP BOTTOM COMP



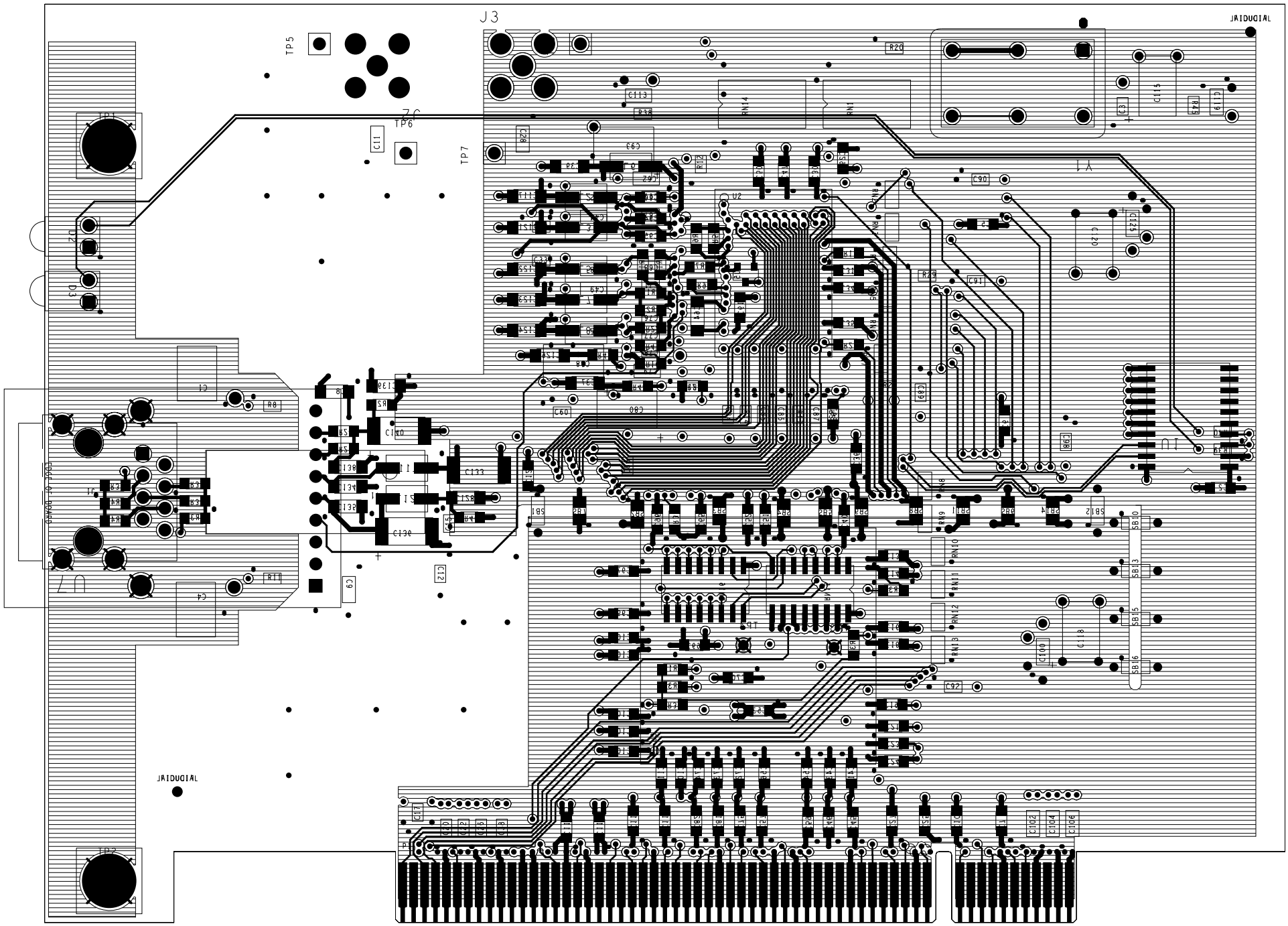
PMC-SIERRA ULTRA REFERENCE DESIGN REV.2.0 1997

PMC-SIERRA ULTRA REFERENCE DESIGN REV.2.0 1997

VCC PLANE

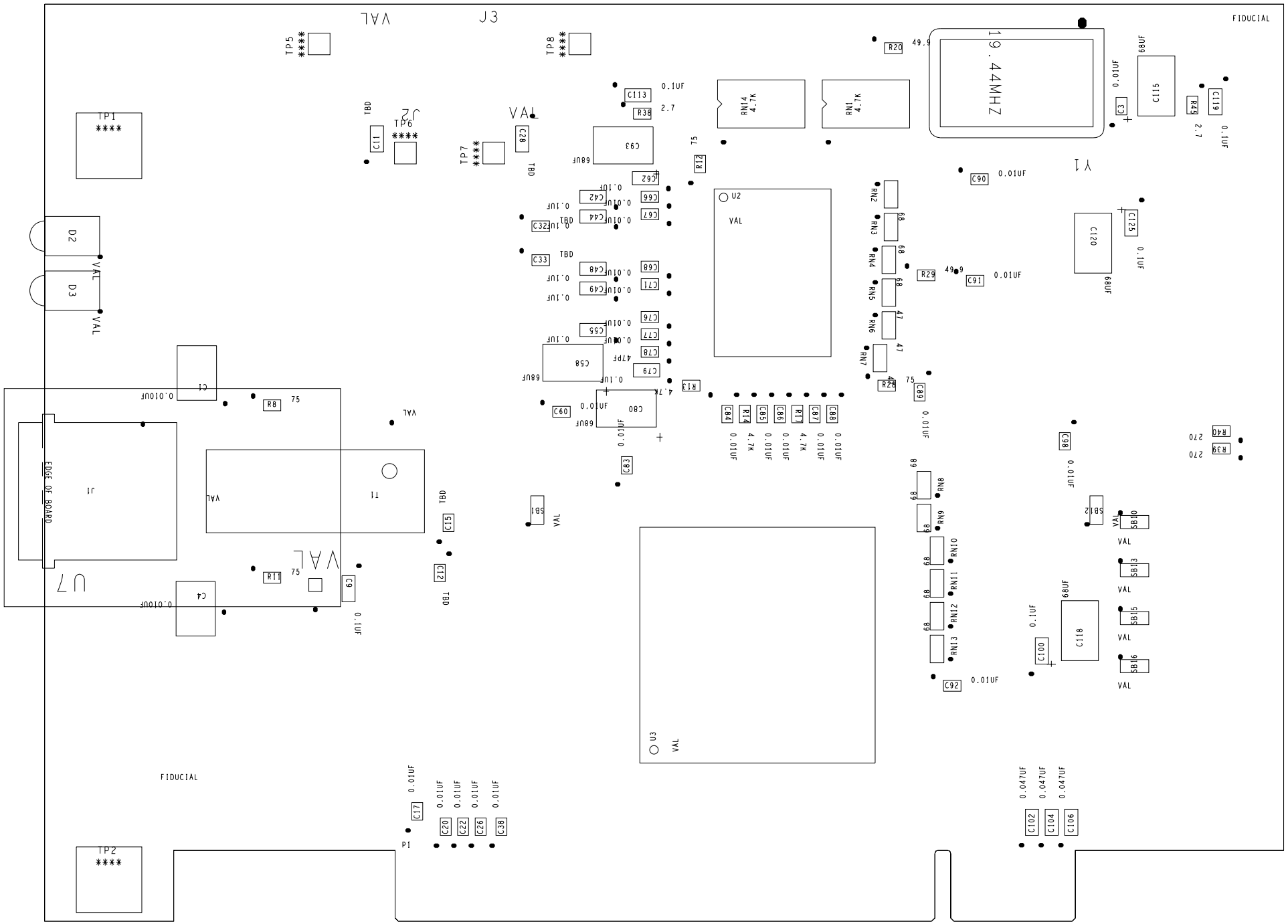
COMP TOP

BOTTOM LAYER

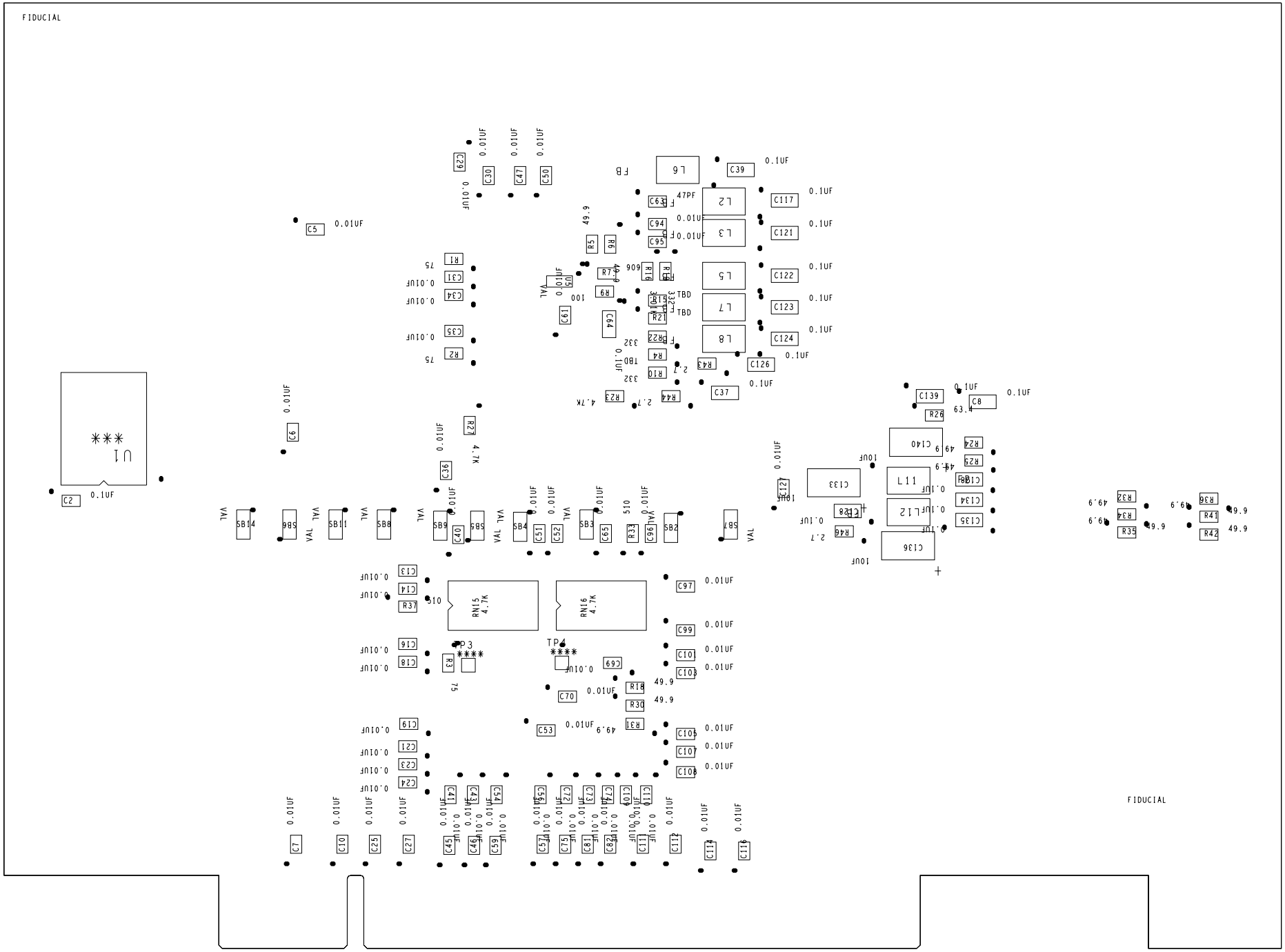


PMC-SIERRA ULTRA REFERENCE DESIGN REV.2.0 1997

PMC-SIERRA ULTRA REFERENCE DESIGN REV.2.0 1997

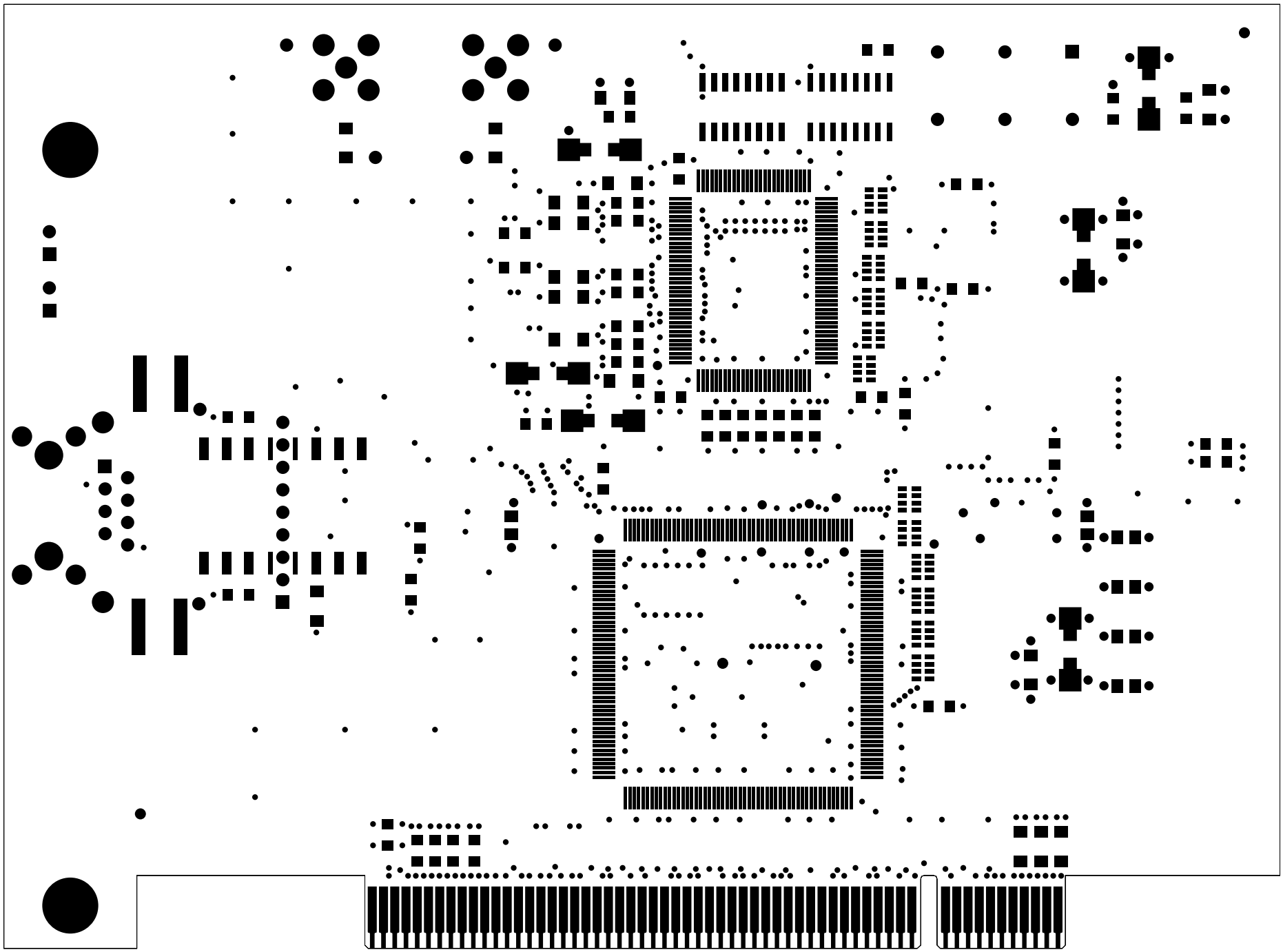

FIDUCIAL
J3
VAL
TP5
TP8
TP1
TP2
TP6
TP7
J2
TBD
C11
C28
C113
0.1UF
R38
2.7
RN14
4.7K
RN1
4.7K
R20
49.9
19.44MHZ
C3
0.01UF
C115
68UF
R45
2.7
C119
0.1UF
Y1
C90
0.01UF
C93
68UF
R12
75
C62
C66
C42
C67
C44
0.01UF
0.1UF
C32
C33
TBD
C68
C48
C71
C49
C76
C55
C77
C78
C58
47PF
C79
C60
C80
0.01UF
C83
SB1
U2
VAL
RN2
RN3
RN4
RN5
RN6
RN7
68
47
R29
49.9
C63
0.01UF
C120
68UF
C125
0.1UF
R28
C69
0.01UF
C84
R14
4.7K
C85
C86
R17
4.7K
C87
C88
0.01UF
C98
0.01UF
R40
270
R39
270
RN8
RN9
RN10
RN11
RN12
RN13
SB12
SB10
SB13
SB15
SB16
C118
C100
0.1UF
C92
0.01UF
U3
VAL
C17
C20
C22
C26
C38
P1
C102
C104
C106
0.047UF
U7
J1
EDGE OF BOARD
T1
C1
C4
R8
R11
C15
C12
C9
0.01UF
0.1UF
75

COMP BOTTOM



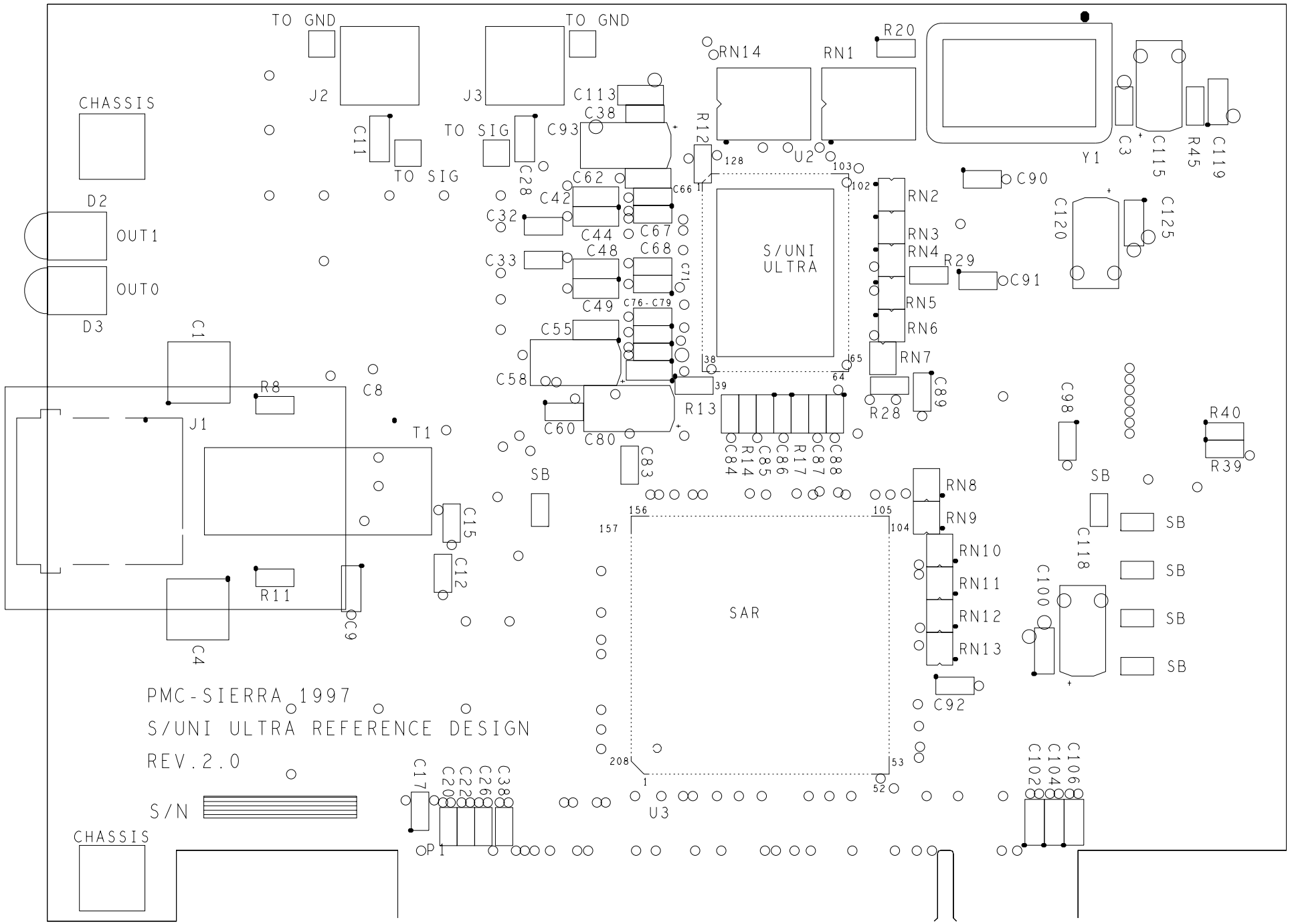
PMC-SIERRA ULTRA REFERENCE DESIGN REV.2.0 1997

SOLDERMASK TOP

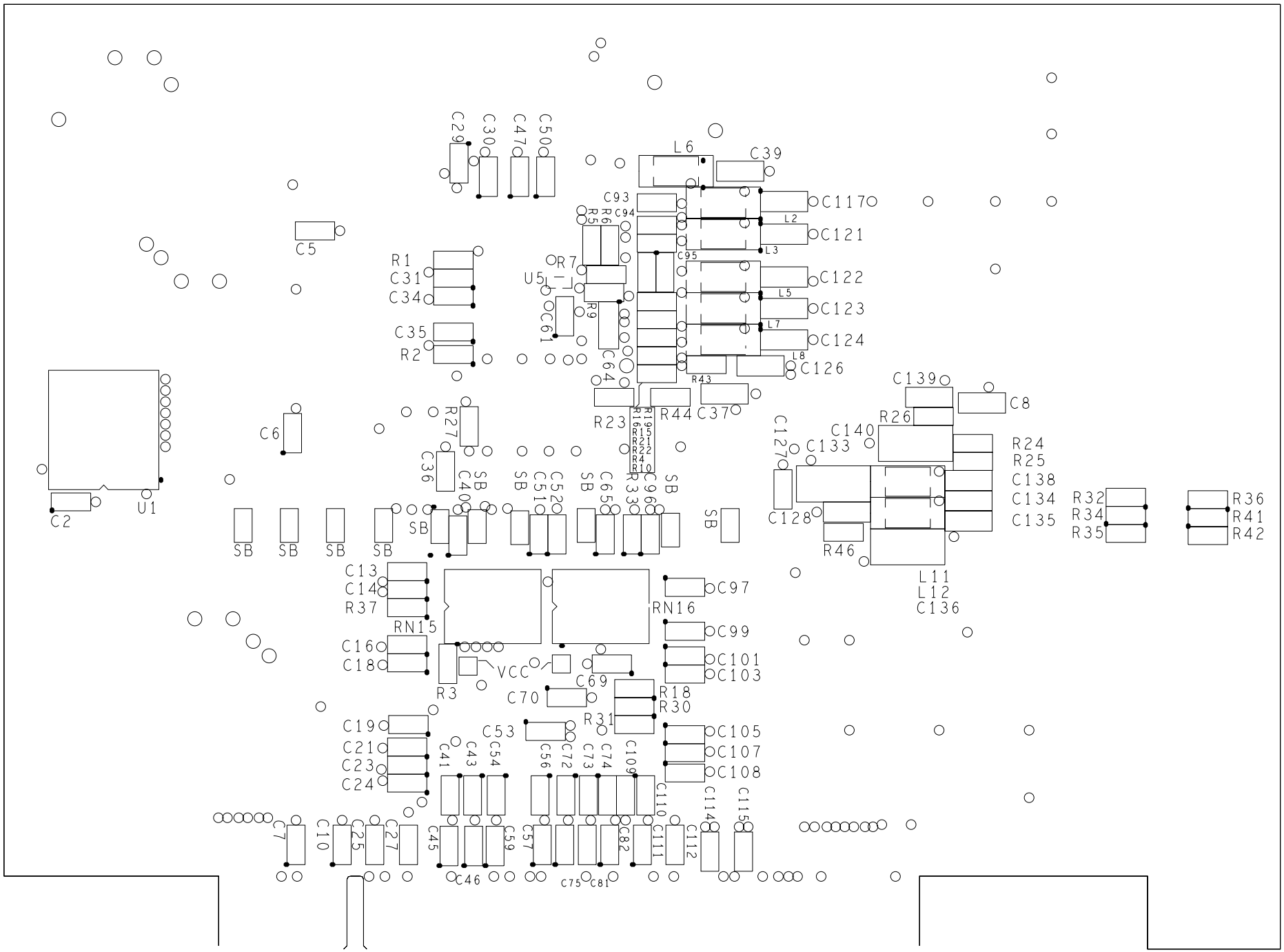


PMC-SIERRA ULTRA REFERENCE DESIGN REV.2.0 1667

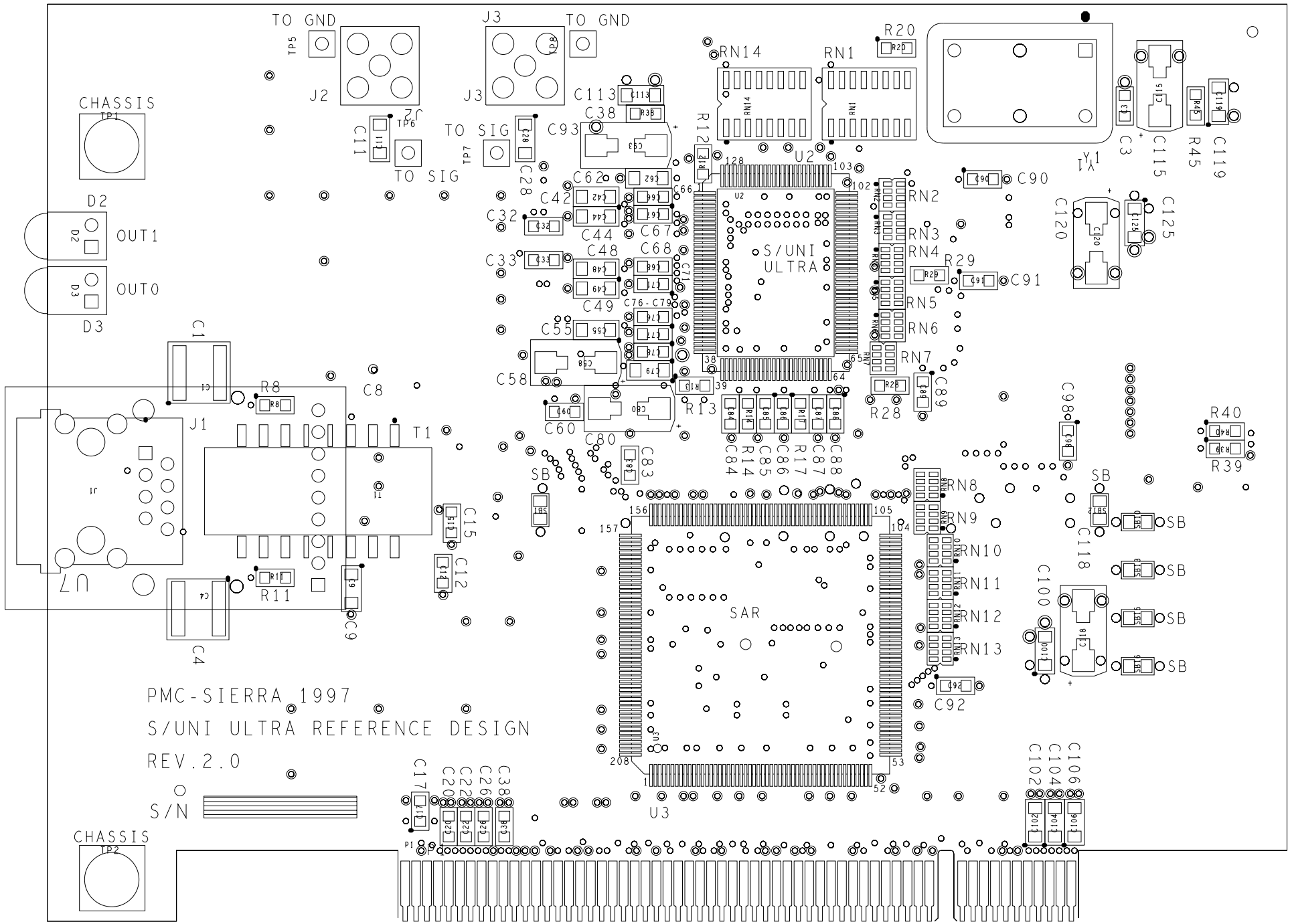
SOLDERMASK BOTTOM


TO GND
TO GND
J2
J3
CHASSIS
TO SIG
TO SIG
C11
C28
C38
C93
C113
RN14
RN1
R20
R12
U2
Y1
C3
C115
R45
C119
D2
OUT1
OUT0
D3
C62
C42
C32
C44
C67
C66
C33
C48
C68
C71
C49
C76-C79
C55
C58
C60
C80
C83
R13
C84
R14
C85
C86
R17
C87
C88
S/UNI
ULTRA
RN2
RN3
RN4
RN5
RN6
RN7
R29
C91
C90
C120
C125
C89
R28
C98
R40
R39
C1
R8
C8
J1
T1
SB
C15
C12
R11
C9
C4
SAR
RN8
RN9
RN10
RN11
RN12
RN13
C92
C118
C100
SB
SB
SB
SB
PMC-SIERRA 1997
S/UNI ULTRA REFERENCE DESIGN
REV.2.0
S/N
C17
C20
C22
C26
C38
U3
C102
C104
C106
P1
CHASSIS

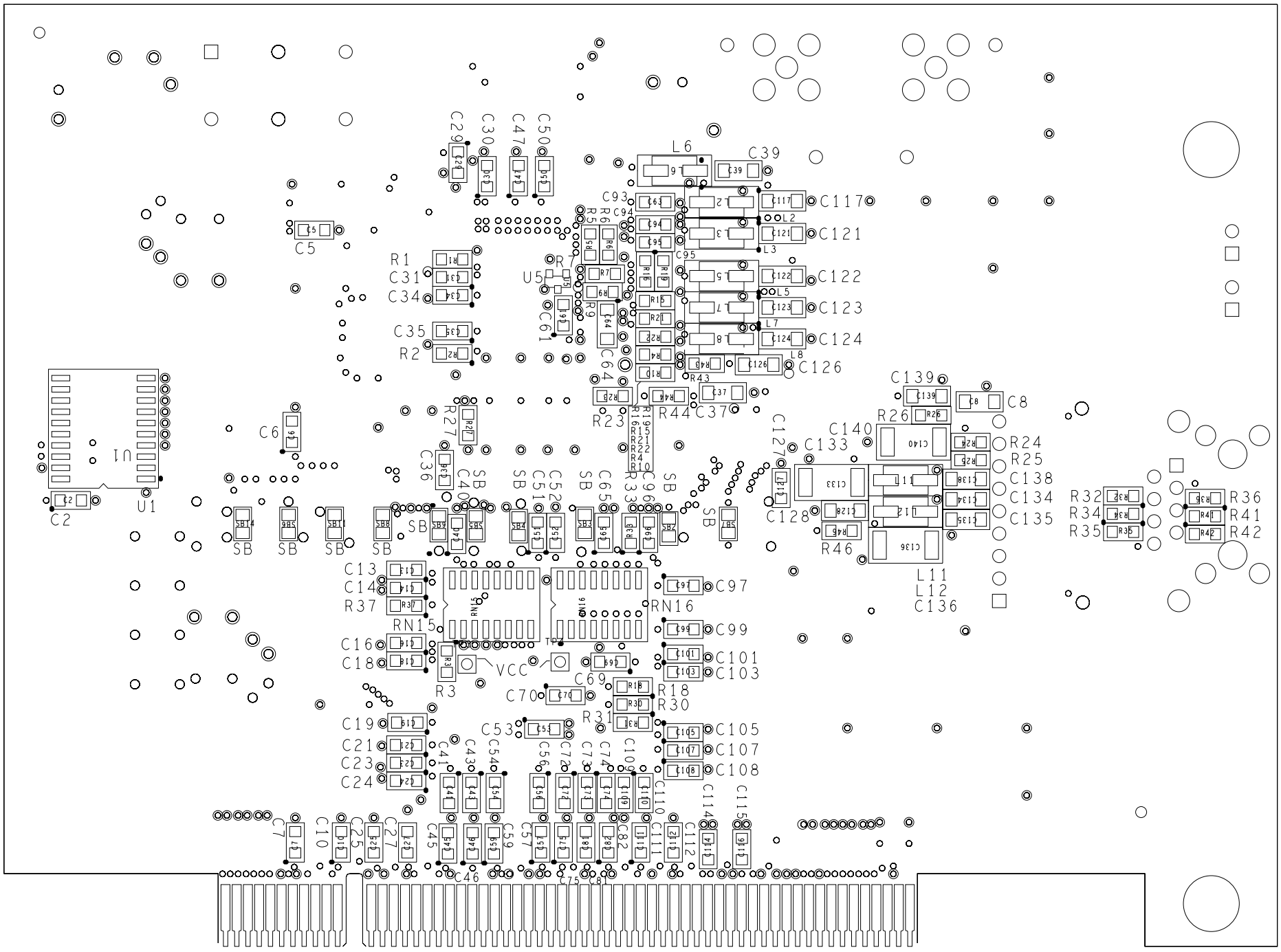
SILK SCREEN BOTTOM



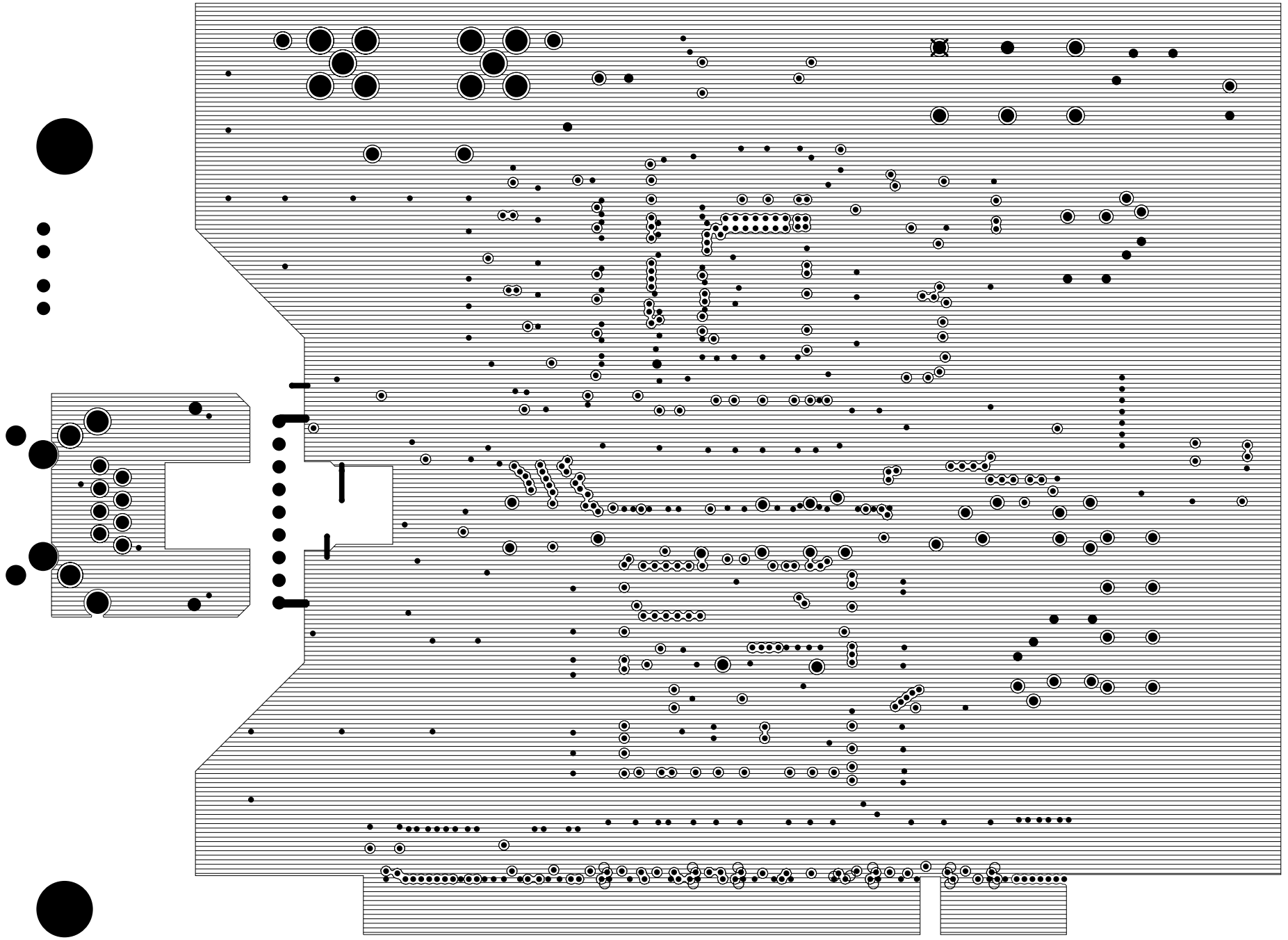
PMC-SIERRA ULTRA REFERENCE DESIGN REV.2.0 1997


TO GND
TP5
J2
J3
TO GND
CHASSIS
TP1
TO SIG
TP6
TO SIG
TP7
D2
OUT1
D3
OUT0
S/UNI
ULTRA
SAR
PMC-SIERRA 1997
S/UNI ULTRA REFERENCE DESIGN
REV.2.0
S/N
CHASSIS
TP2
U2
U3
J1
T1
U7
SB

SILK SCREEN BOTTOM

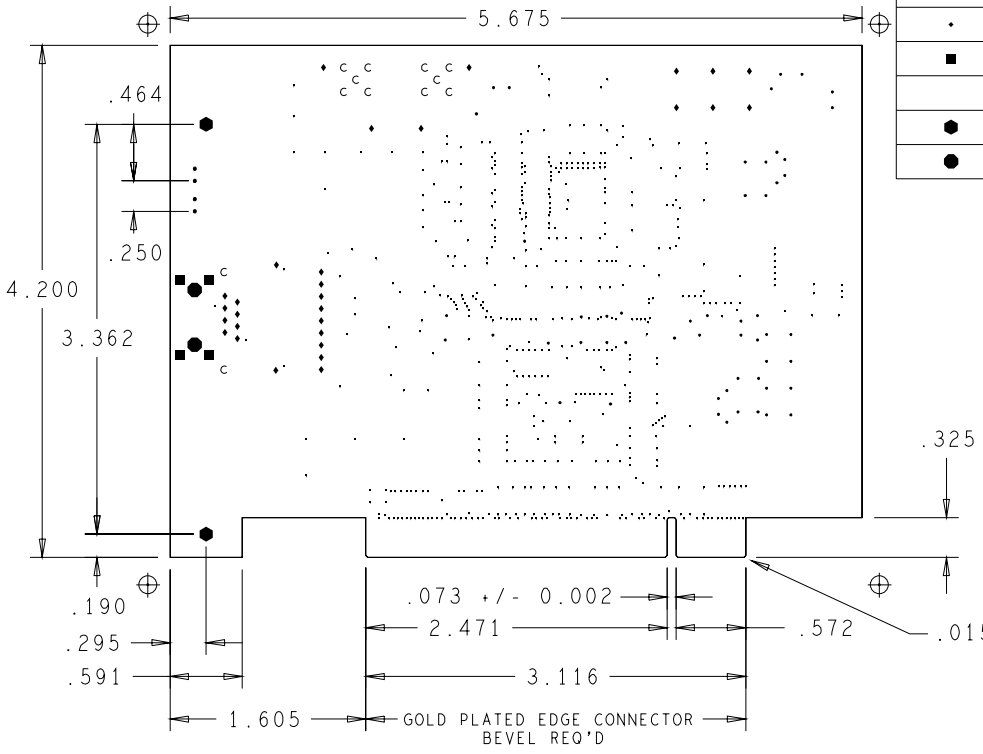


PMC-SIERRA ULTRA REFERENCE DESIGN REV.2.0 1997



REVISIONS					
REV	DESCRIPTION	DATE YY	DATE MM	DATE DD	APPROVED

PMC-SIERRA ULTRA REFERENCE DESIGN REV.2.0 1997



VIEW FROM COMPONENT SIDE B

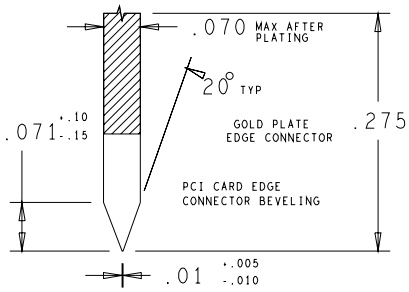
DRILL CHART			
FIGURE	SIZE	PLATED	QTY
·	13.0	PLATED	516
·	25.0	PLATED	53
•	36.0	PLATED	4
•	42.0	PLATED	29
■	76.0	PLATED	4
	79.0	PLATED	12
⬢	125.0	PLATED	2
⬢	128.0	NOT PLATED	2

	Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
#	COPPER	CONDUCTOR	TOP	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	10.0 mil	4.2
	COPPER	CONDUCTOR	GND_PLANE	POSITIVE	2.88 mil	-------
	FR-4	DIELECTRIC	-------	-------	33.0 mil	4.2
	COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	2.88 mil	-------
	FR-4	DIELECTRIC	-------	-------	10.0 mil	4.2
#	COPPER	CONDUCTOR	BOTTOM	POSITIVE	1.44 mil	-------

Note: 50 ohm controlled impedance traces with trace width of 17 mil are on Top and Bottom layers.

Notes:

1. Copper thickness is 1 oz. on outer layers and 2 oz. on gnd & vcc plane.
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are spedified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.



ARTWORK FILM
TOP LAYER
GROUND PLANE
VCC PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
MECH DRAWING
SOLDER PASTE TOP
SOLDER PASTE BOTTOM
MECH DRAWING

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES

TOLERANCES ON:
2 PL DECIMALS +/- .03
3 PL DECIMALS +/- .003
ANGLES
FRACTIONS

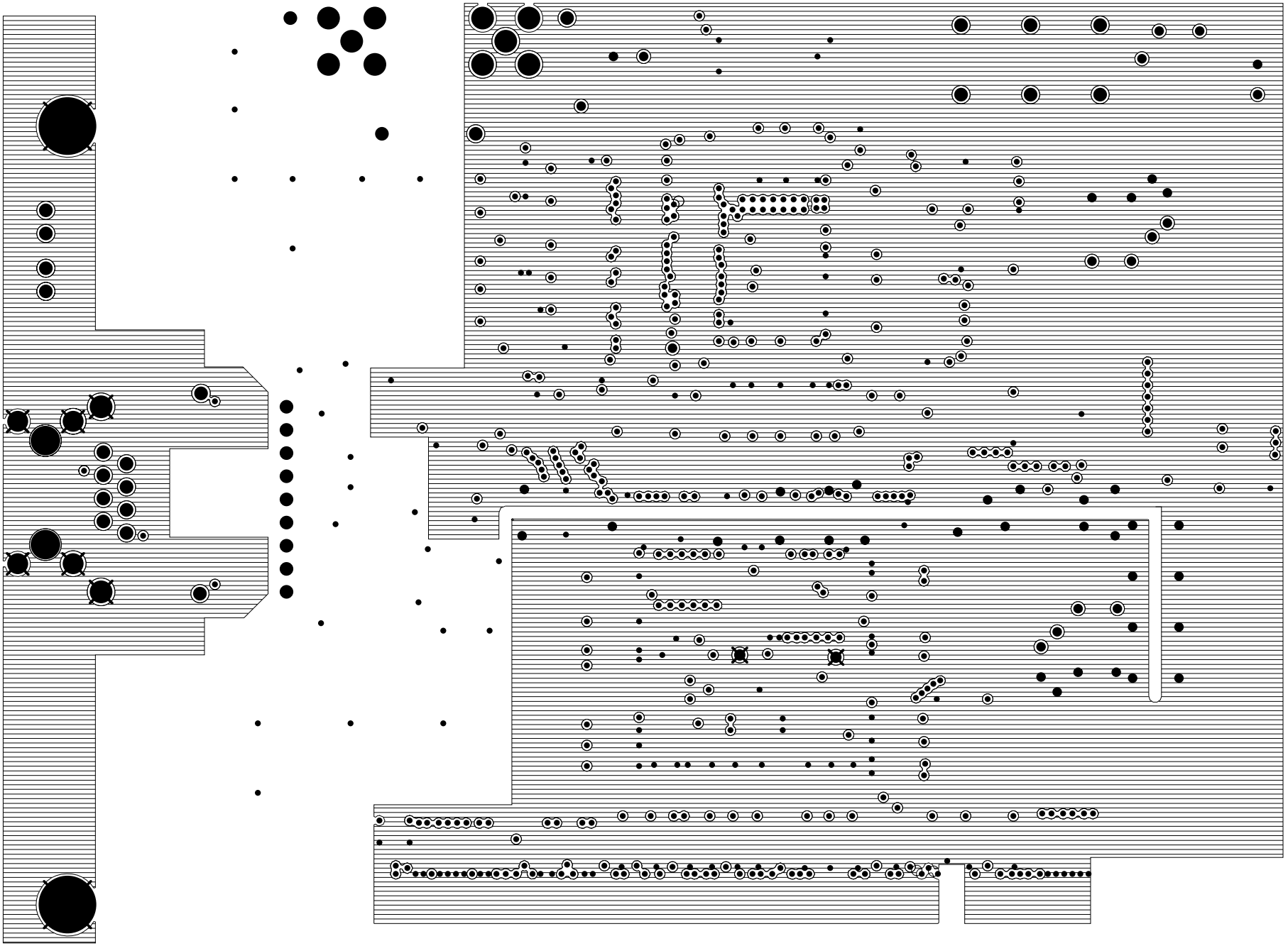
	DATE YY	DATE MM	DATE DD
DRAWN S. SIU	96	11	13
CHECKED			
ENGINEER			
APPROVED			

PMC-Sierra, Inc.
105-8555 Baxter Place, Buranby B.C.
Canada, V5A 4V7
Tel: 604 415-6000 Fax: 604 415-6200

SIZE	FSCM NO	DWG NO
B		

SCALE | SHEET 1 OF 1

VCC PLANE



9 APPENDIX D: EMI LAB TEST REPORT

Please see separate PMC-Sierra document entitled, “SUNI-ULTRA REFERENCE DESIGN EMI LAB TEST REPORT”, number PMC-990512.

PMC-Sierra, Inc.
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PMC-961062 (R3) ref PMC-960924 Issue date: July 1999