PM7364

FREEDM-32 WITH TOCTL

REFERENCE DESIGN

PRELIMINARY INFORMATION

ISSUE 1: SEPTEMBER 1997

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CONTENTS

1 OVERVIEW 1

1.1 APPLICATION PERSPECTIVE 1

1.2 DESIGN CONSTRAINTS 2

1.3 REFERENCES 3

2 FEATURE OVERVIEW 4

3 FUNCTIONAL DESCRIPTION 5

3.1 REFERENCE DESIGN CARD 5

3.2 FRAME RELAY PROTOCOL ENGINE AND DATALINK MANAGER 6

3.3 PCI BUS INTERFACE TO THE HOST PROCESSOR AND PACKET MEMORY 8

3.4 T1 FRAMERS 11

3.5 T1 LINE INTERFACE 12

3.6 T3 LINE INTERFACE 13

3.7 M13 MULTIPLEX 13

3.8 ON-BOARD MICROPROCESSOR 15

4 IMPLEMENTATION DESCRIPTION 17

4.1 SYSTEM TESTBED DESCRIPTION 17

4.2 CARD SIZE AND COMPONENT PLACEMENT 18

4.3 PCI INTERFACE 19

4.4 FIRMWARE DESCRIPTION 19

4.5 SCHEMATIC NOTES 19

5 GLOSSARY 28

6 APPENDIX A. SCHEMATICS, LAYOUT 31

7 APPENDIX B: BILL OF MATERIALS 32

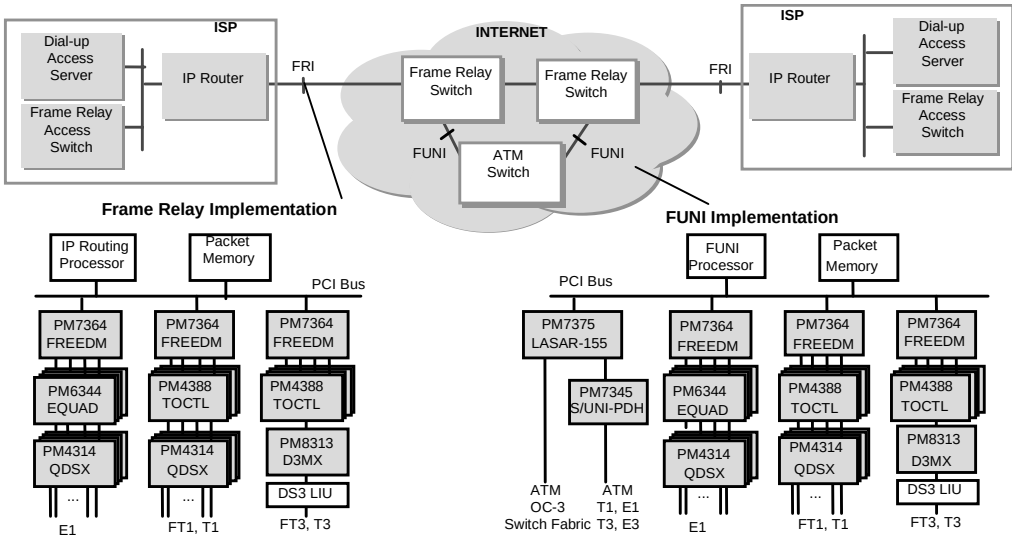
1 OVERVIEW

1.1 Application Perspective

The FREEDM-32 standard product is primarily designed for the frame relay application. Frame relay is a multiplexed data networking technology supporting connectivity between user equipment (routers, nodal processors/fast packet switches) and between user equipment and the public frame relay network. The frame relay protocol supports data transmission over a connection-oriented path and enables the transmission of variable-length data units over an assigned virtual connection.

Frame relay technology can be used in LAN interconnection, Internet access and Internet backbones using link speeds ranging from 9600 baud to the DS3 rate. Figure 1 illustrates a typical implementation of a frame relay interface (FRI) and a frame relay user to network interface (FUNI) using fractional T1 (FT1), T1, E1 and DS3 rates. Other line options such as J2 and SONET virtual tributary (VT) mapping are not shown in the illustration.

Figure 1. Frame Relay Inter-networking Overview



User equipment such as routers, T1 multiplexers, front end processors (FEPs), and packet assemblers/dissemblers (PADS) need to support the frame relay interface in order for them to be connected to a private or a public frame relay network.

1.2 Design Constraints

The purpose of the "FREEDM-32 With TOCTL" reference design is to serve as an example to assist designers of routers and frame relay switches to design their products using PMC-Sierra's FREEDM-32, TOCTL, D3MX and QDSX standard products, as shown in figure 2.

This design illustrates the frame relay application with interfaces to channelized T3, channelized T1 and unchannelized T1 data streams. The hardware which implements these interfaces is built, tested and debugged thereby assisting designers to more quickly bring their designs to market.

The following hardware constraints have been included in this design:

- Support the PCI local bus revision 2.1, which allows up to four PCI devices per PCI bus segment to be connected to a host processor and packet memory. This constraint allows the reference design to be implemented as an add-in card to any readily available processor board with a revision 2.1 compliant PCI bus. Up to four reference design cards can be interfaced to the processor board.

- Mechanical and electrical constraints for interfacing an add-in card to the processor board, as specified in revision 2.1 of the PCI local bus specification.

The software interfaces to the FREEDM-32 via a host processor on the PCI bus and enables support of network protocol layers necessary to transmit and receive data packets of a PVC. Software procedures are provided to illustrate the following:

- PCI device location and memory resource assignment
- Reset of the hardware via software
- Initialization of the hardware, software and the packet memory
- Activation/deactivation of the hardware
- Provisioning/unprovisioning of PVCs
- Transmit and receive packet processing
- Error handling
- Performance counters

- Diagnostics

The following software constraints have been included in this design:

- The FREEDM-32 data interfaces are the only interfaces the software has access to. The content of the user data field of the HDLC frame is not processed. Other upper layer functions such as congestion management, LMI protocol and multi-cast capability are not implemented.

- Source code is written in the C language and developed using the VxWorks Tornado development environment. Executable code can run on i960 or Pentium based processor boards.

1.3 References

[1] PMC-960113, PMC-Sierra, "Frame Relay Protocol Engine and Datalink Manager" Standard Product Datasheet, December, 1996, Issue 2
[2] PCI SIG, PCI Local Bus Specification, June 1, 1995, Version 2.1
[3] PCI Compact Specification, PCI Industrial Computers Manufacturers Group, 1995, Version 1.0
[4] PMC-970280, PMC-Sierra, "FREEDM-32 Software Reference Design" Application Note, March, 1997, Issue 1
[5] PMC-961061, PMC-Sierra, "FREEDM-32 PCI Bus Utilization and Latency Analysis" Application Note, February, 1997, Issue 1
[6] PMC-970281, PMC-Sierra, "FREEDM-32 Programmer's Guide" Application Note, March, 1997, Issue 1
[7] PMC-970959 PMC-Sierra, “MC68340 Software for the “FREEDM with TOCTL” Reference Design

2 FEATURE OVERVIEW

This reference design provides the following features:

- Frame relay processing of up to 128 logical channels associated with T1 or channelized T1 data streams. A logical channel can be composed of an unchannelized data stream, or a number of time-slots within a channelized data stream.
- Interfaces to a host processor and packet memory via the PCI local bus.
- Interface to one T3 link carrying channelized data.
- Interface to four T1 links carrying channelized or unchannelized data streams.
- Includes a M13 Multiplexer to provide 28 T1 data streams from a T3 link.
- Includes a T1 framer for each of the 32 T1 data streams.

3 FUNCTIONAL DESCRIPTION

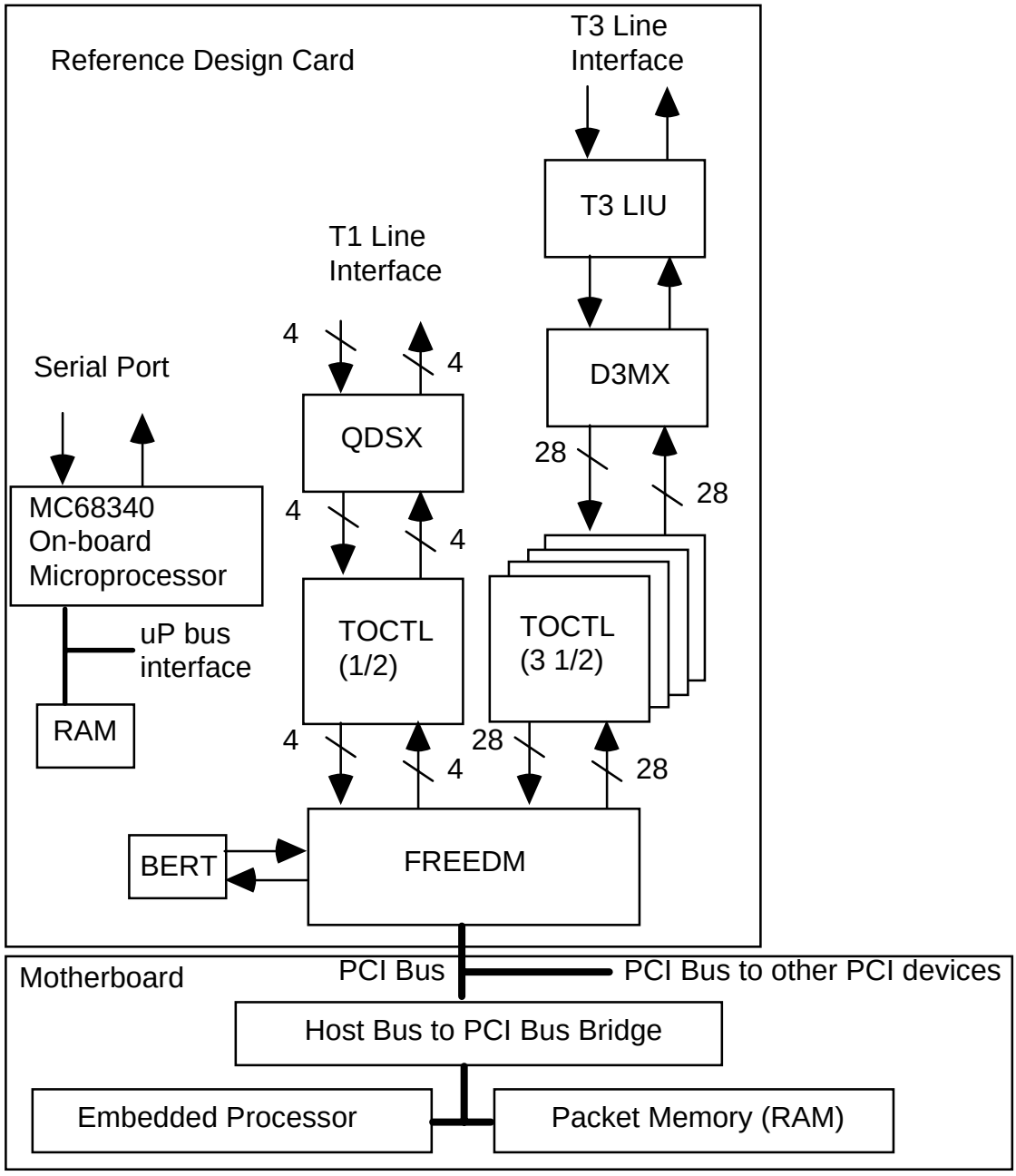
3.1 Reference Design Card

The FREEDM-32 with TOCTL reference design card is an add-in card that connects the FREEDM-32 to a host processor and packet memory. The host processor may function as an IP routing processor, which serves to route packets among FREEDM-32 channels of the same reference design card, and/or FREEDM-32 channels of different reference design cards. A block diagram showing the reference design card is shown in figure 2.

The frame relay packets from a remote node are available at one of the T1 line interfaces or the channelized T3 interface. There are four T1 line interface connectors to provide four of the T1 data streams to the FREEDM-32 via the QDSX. The remaining 28 serial ports of the FREEDM-32 contain T1 data streams that are multiplexed via the D3MX from the channelized T3 line interface.

The on-board microprocessor has a serial port, which enables control and monitoring of the T1 LIU's, the T1 framers, the M13 multiplexer and the BERT. The serial port can be interfaced to the motherboard, or attached to a terminal.

Figure 2. Reference Design Card Block Diagram



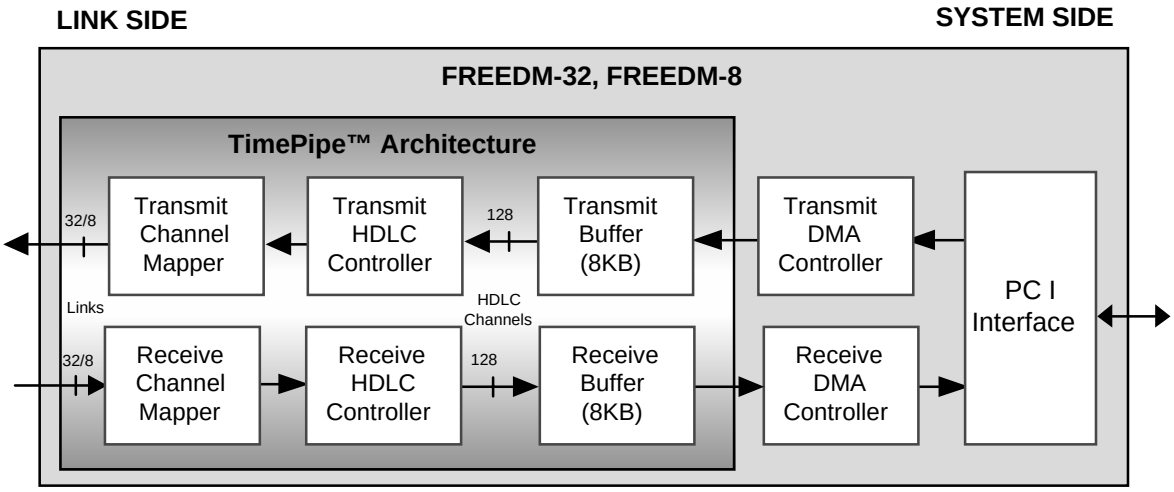
3.2 Frame Relay Protocol Engine and Datalink Manager

The **FR**ame **E**ngin**E** and **D**ata Link **M**anager (FREEDM) is a family of advanced data link layer processors that is ideal for applications such as Internet access equipment,

frame relay switches, ATM switches, packet-based CDMA base station controllers and Digital Subscriber Loop Access multiplexers (DSLAM).

The cornerstone of the FREEDM product family is the revolutionary TimePipe™ architecture (as shown in Figure 3). The TimePipe architecture enables a single FREEDM device to support up to 32 physical links, 128 HDLC channels and 8 KB of integral packet buffer in each of the transmit and receive direction. Each one of the 32 physical links can be independently timed from 56 Kbit/s to 52 Mbit/s. This unparalleled level of integration not only simplifies networking equipment designs, but also enables a new generation of line card designs that can use a common data link layer processor for a wide variety of line rates ranging from T1, E1, E3, T3 to HSSI.

Figure 3: FREEDM Block Diagram and the TimePipe Architecture



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Power is useful only if it can be directed to perform the intended work. The TimePipe architecture is not only powerful but also highly configurable as well. A flexible channel mapper mechanism is provided such that any link can be assigned to any HDLC channel in software. In the case of a channelized application, data carried on one or more time-slots within the same link can be grouped and assigned to a single HDLC channel.

The 8KB packet buffer can be flexibly allocated to active HDLC channels. The 8KB buffer is organized as 512 blocks of 16 byte FIFOs. The number of blocks assigned to any HDLC channel is configurable in software.

In the receive direction, the Receive HDLC Controller performs flag delineation, bit destuffing, CRC verification using either CRC-32 or CRC-CCITT algorithm and length checking. In the transmit direction, the Transmit HDLC Controller performs flag insertion, bit stuffing and CRC calculation using either CRC-32 or CRC-CCITT algorithm.

On the system side, FREEDM provides a 33 MHz, 32 bit PCI 2.1 compliant bus interface. Two efficient transmit and receive DMA controllers are provided to support burst data transfers across the PCI bus.

The following documents should be consulted for further information on the operation and interfaces of the FREEDM-32:

- FREEDM-32 Long form Datasheet [1]
- FREEDM-32 Programmer's Guide [6]
- FREEDM-32 PCI Bus Utilization and Latency Analysis [5]

3.3 PCI Bus Interface to the Host Processor and Packet Memory

The FREEDM-32 is configured, controlled and monitored across the PCI bus interface by a host processor and packet memory (RAM). In some configurations there may be multiple reference design cards on the PCI bus, and during a bus transaction one of the FREEDM-32 devices may act as the bus master in accessing the packet memory, or the host processor may act as the bus master in accessing one of the FREEDM-32 registers of a reference design card.

Figure 4 shows an address map for a PCI bus, which shows one FREEDM-32 device. The data structures shown are required to interface one FREEDM-32 to the PCI bus. In this figure, PCI addresses are 32-bit physical addresses, which can be observed at the address pins of the PCI bus interface.

When multiple FREEDM-32's are attached to the bus each FREEDM-32 must have a unique set of the following data structures.

- Transmit Descriptor Table
- Receive Descriptor Table

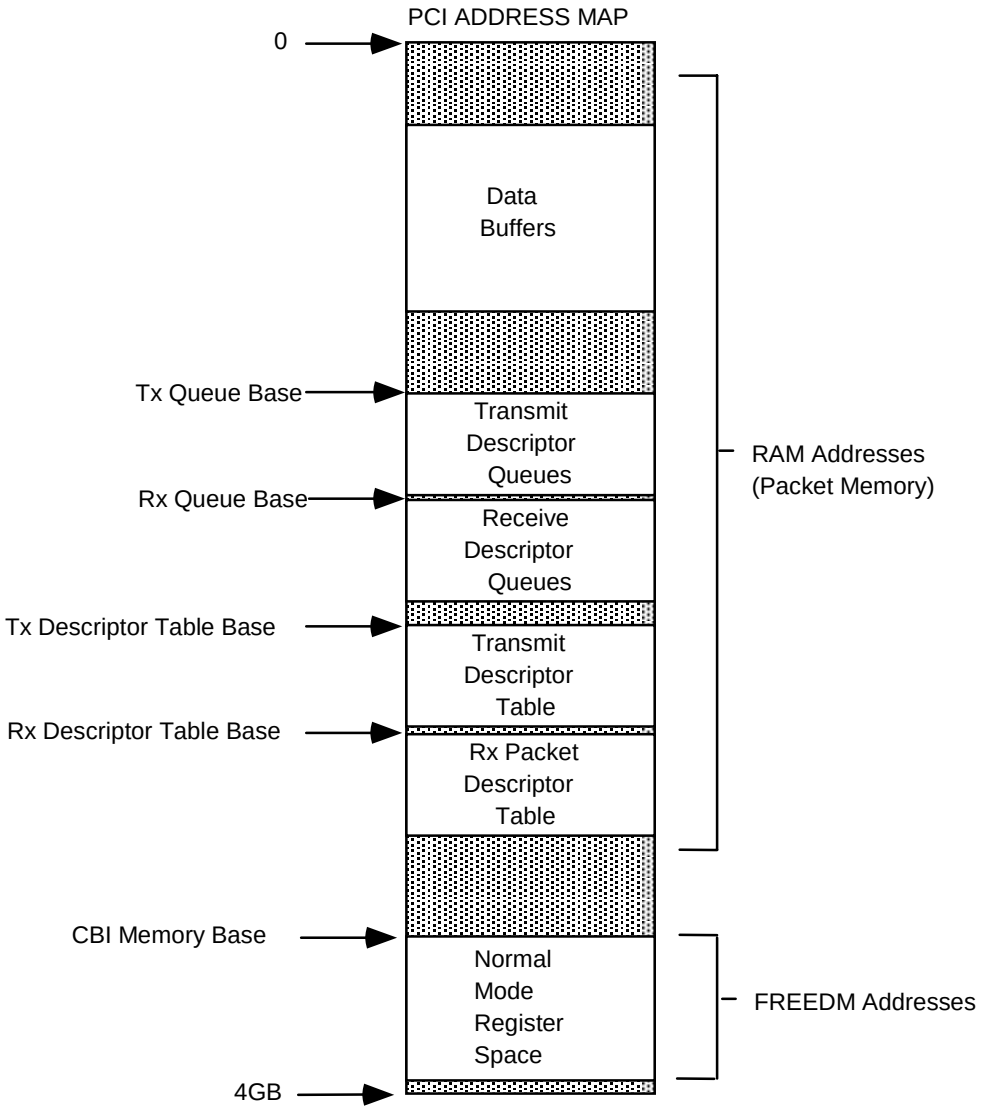
- Transmit Queue Space
- Receive Queue Space
- Normal Mode Register Space

The data structures within packet memory are accessed by software running on the host processor, or by the FREEDM-32. The software specifies the location of these data structures by writing base addresses into the appropriate FREEDM-32 registers, before activating the FREEDM-32.

The data Buffers are filled with the data received by the FREEDM-32, or contain transmit data which is read by the FREEDM-32. The descriptor tables and the queues are required to manage these buffers.

The Normal Mode Register space is accessed by the software running on the host processor to manage and control operation of a FREEDM-32 device. This register space is located in the FREEDM-32 and is mapped into the PCI address space by the software running on the host processor during the boot-up sequence.

Figure 4. PCI Address Map



The PCI Configuration Space does not reside in the PCI address map, but it is a requirement for all PCI devices. The Configuration Space is a block of 256 contiguous bytes that reside in the PCI device (the FREEDM-32 in this case), and is accessed by the host processor in a PCI bus Configuration Read (or Write) transaction, rather than a Memory Read (or Write) transaction. Access to this configuration space is system specific and a thorough discussion of it can be found in the PCI specification[2].

A description of the software running on the host processor can be found in the document "FREEDM-32 Software Reference Design".

3.4 T1 Framers

T1 framing for the 32 T1 data streams is provided via four PM4388 octal T1 framers (TOCTL). The TOCTL is a feature-rich device for use primarily in systems carrying data over DS1 facilities. Each of the eight framers within a TOCTL is independently software configurable, allowing feature selection without changes to external wiring.

On the receive side, each of eight independent framers can be configured to frame to either of the common DS1 signal formats: (SF, ESF) or to be bypassed (unframed mode). The TOCTL detects and indicates the presence of YELLOW and AIS patterns and also integrates YELLOW, RED, and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, out-of-frame events, and changes of frame alignment is provided. The TOCTL also detects the presence of in-band loopback codes, ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link. The HDLC messages are terminated in a 128 byte FIFO. An elastic store that optionally supports slip buffering and adaptation to back plane timing is provided, as is a signaling extractor that supports signaling de-bounce, signaling freezing and interrupt on signaling state change on a per-DS0 basis. The TOCTL also supports idle code substitution and detection, digital milliwatt code insertion, data extraction, trunk conditioning, data sign and magnitude inversion, and pattern generation or detection on a per-DS0 basis.

On the transmit side, the TOCTL generates framing for SF or ESF DS1 formats, or framing can be optionally disabled. The TOCTL supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion, zero-code suppression, and pattern generation or detection on a per-DS0 basis.

The TOCTL can also generate in-band loopback codes, ESF bit oriented codes, and transmit HDLC messages on the ESF data link. The HDLC messages are generated from a 128 byte FIFO.

The TOCTL can generate a low jitter transmit clock, and also provides jitter attenuation in the receive path.

It should be noted that the TOCTL device operates on unipolar data only: B8ZS substitution and line code violation monitoring, if required, must be processed by the T1 LIU, in this case the QDSX.

Further information on the TOCTL can be found in the long form datasheet.

Note: The TOCTL is not necessarily a replacement for two PM4344 TQUAD devices because the TOCTL is optimized for data applications. No additional glue logic is required to interface TOCTL's to the FREEDM-32 and so, we recommended that the TOCTL, not the TQUAD, be used with the FREEDM-32.

3.5 T1 Line Interface

The PM4314 QDSX Quad T1/E1 Line Interface Device is a monolithic integrated circuit that supports G.703-compatible transmit and receive interfaces for four 1544 kbit/s T1 data streams.

In the incoming direction, the T1 signal for each quadrant of the QDSX are first processed by the receive data slicer. The receive data slicer converts the line signal received via a coupling transformer to dual rail RZ digital pulses. Adaptation for attenuation is achieved using an integral peak detector that sets the slicing levels. Through use of passive external attenuation circuitry, either terminated or bridge monitored T1 signal levels can be accommodated. The low signal level condition or signal squelch may be enabled to generate interrupts. Clock and data are recovered from the dual rail RZ digital pulses using a digital phase-locked loop that provides excellent high frequency jitter tolerance. The recovered data is decoded using B8ZS line code rules. Loss of signal and line code violations are detected as well as excessive zeros, and B8ZS signatures. These various events or changes in status may be enabled to generate interrupts. Additionally, loss of signal and line code violations are also indicated on outputs.

In the outgoing direction, each quadrant of the QDSX encodes the T1 stream using B8ZS line code rules, or it may accept pre-encoded data in dual rail NRZ format. Jitter attenuation is provided by passing the outgoing data through a FIFO. A low jitter clock is generated by an integral digital phase-locked loop and is used to read data from the FIFO. FIFO overrun or underrun may be enabled to generate interrupts. Alarm indication signal (all ones) may be substituted for the FIFO data. The digital data is converted to high drive, dual rail RZ pulses that drive the T1 interface through a coupling transformer. The shape of the pulses is programmable to ensure that the T1 pulse template is met at the DSX-1 distribution frame. Driver performance monitoring is provided and may be enabled to generate interrupts upon driver failure.

The jitter attenuation function can optionally be moved to the receive side. The recovered clock and data is passed through the jitter attenuator before being presented at the digital receive outputs.

Internal high speed timing for all quadrants of the QDSX is provided by a common 37.056 MHz master clock.

Diagnostic loopback is provided and the loopback may be invoked past the analog transmit outputs using the driver performance monitors or invoked prior to the conversion to analog. Line loopback with jitter attenuation is provided.

The QDSX may insert an unframed 2^{15}-1 O.151 compatible pseudo-random bit sequence into the transmitted PCM data stream. Optionally, the PRBS insertion may be switched to the received side where it overwrites the data from the slicer.

The QDSX detects an unframed 2^{15}-1 O.151 compatible pseudo-random bit sequence input to the receive slicer. This PRBS detector can operate in the presence of a 10^{-2} bit error rate. Bit errors are detected and recorded. The PRBS detector can optionally be switched to the transmit side where it can detect unframed PRBS data from the unipolar input transmit data stream.

The QDSX operates in conjunction with external line coupling transformers, resistors, and capacitors. An external crystal oscillator may be used for high speed timing generation. The QDSX is configured, controlled, and monitored using registers that are accessed via a generic microprocessor interface.

Further information on the QDSX can be found in the long form datasheet.

3.6 T3 Line Interface

The T3 line interface is provided by the SSI 78P7200 line interface transceiver IC, along with transformers and a few passive components.

The receiver has a very wide dynamic range and accepts B3ZS-encoded bipolar inputs; it provides CMOS logic level clock, positive and negative data and low-level signal detect outputs. An on-chip equalizer improves the intersymbol interference tolerance on the receive path.

The transmitter converts CMOS logic level clock, positive and negative data input signals into a bipolar signal with the appropriate pulse shape for T3 transmission.

3.7 M13 Multiplex

The M13 multiplex function is provided by the PM8313 D3MX M13 Multiplexer. It is configured in this design to support asynchronous multiplexing and demultiplexing of 28 DS1s into a DS3 signal.

Receive DS3 framing is provided by the DS3 FRMR Framer Block. The FRMR accepts either a B3ZS encoded bipolar, or a unipolar signal compatible with M23 and C-bit parity applications. The FRMR frames to a DS3 signal with a maximum average reframe time of 1.5 ms in the presence of a 10^{-3} bit error rate. The FRMR indicates line code violations, loss of signal, framing bit errors, parity errors, C-bit parity errors, and far end block errors (FEBE). The FRMR detects far end receive failure (X-bits set to 0), the alarm indication signal (AIS), and the idle signal. The FRMR is an off-line framer, indicating both out of frame (OOF) and change of frame alignment (COFA) events. The error events (FER, CBIT PARITY ERROR, FEBE, etc.) are still indicated while the framer is OOF, based on the previous frame alignment.

The C-bit parity far end alarm channel (FEAC) and path maintenance data link are supported. Bit oriented codes in the FEAC channel are detected by the RBOC Bit-Oriented Code Receiver Block. If enabled, the RBOC generates an interrupt when a valid code has been received. The path maintenance data link is terminated using either the RFDL Data Link Receiver Block or an external HDLC receiver. The RFDL supports polled, interrupt driven, and DMA servicing.

DS3 error event accumulation is provided by the DS3 PMON Performance Monitor Block. The PMON accumulates framing bit errors, line code violations, excessive zeros occurrences, parity errors, C-bit parity errors, and far end block errors. Error accumulation continues even while the off-line framer is indicating OOF. The counters should be polled once per second, and are sized so as not to saturate at a 10^{-3} bit error rate. Transfer of count values to holding registers is initiated through the microprocessor interface.

DS3 transmit framing insertion is provided by the DS3 TRAN Transmitter Block. It outputs either a B3ZS encoded bipolar signal, or a unipolar signal. The DS3 TRAN inserts the X, P, M, C, and F bits into the outgoing DS3 stream. The DS3 TRAN block inserts far end receive failure, AIS, and the idle signal under the control of external inputs, or internal register bits. Diagnostic features are provided to allow the generation of line code violation error events, parity error events, framing bit error events, and when enabled for the C-bit parity application, C-bit parity error events, and far end block error events. External inputs allow substitution of the overhead bits or the source of the AIS signal, idle signal or far end receive failure indication.

When configured for the C-bit parity application, bit oriented codes in the FEAC channel are inserted by the XBOC Bit-Oriented Code Transmitter Block. The FEAC code is controlled by an internal register. The path maintenance data link is inserted using the XFDL Data Link Transmitter Block or an external HDLC transmitter. The XFDL supports polled, interrupt driven, and DMA servicing.

The demultiplexing and multiplexing of seven 6312 kbit/s data streams into and out of the DS3 is performed by the MX23 M23 Multiplexer Block. The MX23 contains FIFOs and performs bit stuffing for the rate adaptation of the DS2s. The C-bits are set appropriately, with the option of inserting DS2 loopback requests. The MX23 may be configured to generate an interrupt upon the detection of loopback requests in the received DS3. AIS may be inserted in the any of the 6312 kbit/s tributaries in both directions. C-bit parity is supported by using a 6.3062723 MHz clock, which corresponds to a stuffing ratio of 100%.

Framing to the demultiplexed 6312 kbit/s data streams is provided by the DS2 FRMR Framer. It supports both DS2 (ANSI TI.107) and CCITT Recommendation G.747 frame formats. The maximum average reframe time is 7 ms for DS2 and 1ms for G.747. In DS2 mode, it detects far end receive failure and accumulates M-bit and F-bit errors. In G.747 mode, it detects remote alarm and accumulates framing word errors and parity errors. The DS2 FRMR is an off-line framer, indication both OOF and COFA events. Error events (FERF, MERR, FERR, PERR, RAI, framing word errors) are still indicated while the DS2 framer is indicating OOF, based on the previous alignment.

The multiplexing and demultiplexing of the low speed tributaries into and out of a 6312 Kbit/s data stream is performed by seven MX12 M12 Multiplexers. Each of the MX12 blocks may be independently configured to multiplex and demultiplex four 1544 Kbit/s DS1s into and out of a DS2 formatted signal or to multiplex and demultiplex three 2048 Kbit/s signals into and out of a G.747 formatted signal. Each MX12 may be independently bypassed so an external DS2 may by multiplexed and demultiplexed directly into and out of the DS3. The MX12 contains FIFOs and performs bit stuffing to accommodate the tributary frequency deviations. The C-bits are set appropriately, with the option of inserting DS1 loopback requests. The MX12 block may be configured to generate an interrupt upon the detection of loopback requests in the received DS2. AIS may be inserted in any of the low speed tributaries in both directions.

Further information on the D3MX can be found in the long form datasheet.

3.8 On-board Microprocessor

The Motorola 68340 is used to monitor and control the TOCTL, QDSX, D3MX and BERT devices. It provides the following features:

- 16-bit data bus
- Interrupt controller
- Address decoder

- Timer
- Serial interface

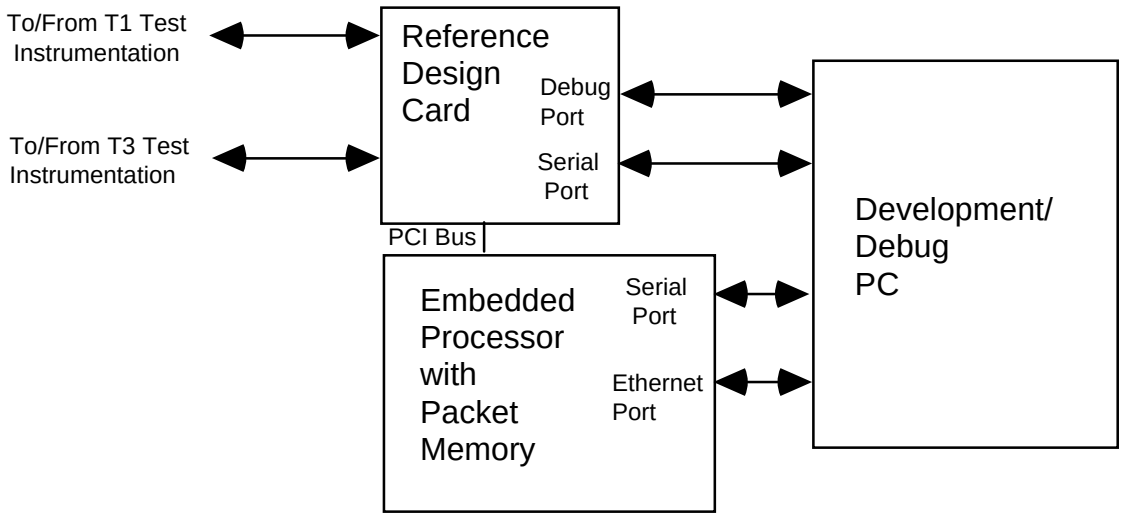
The 68340, is commonly used in many host applications, and its main advantage is that it requires a very small number of external components to be operational. The components include clock circuitry, RAM, ROM, and a serial interface (RS232). It also has an abundance of third-party software support, such as real-time operating systems and C-compilers. In addition, the 68340, has a built-in background debug function, which greatly simplifies the code debugging operation.

4 IMPLEMENTATION DESCRIPTION

4.1 System Testbed Description

The FREEDM-32 reference design card is connected to the test system as shown in figure 5. The T1 and channelized T3 interfaces are attached to external instrumentation. The instrumentation can source data into the receive link of the reference design card and the data is returned on the transmit link after loopback through the packet memory, or loopback at a line interface.

Figure 5. System Testbed Block Diagram



Alternatively, the host processor and packet memory can source the transmit data. The diagnostic loopback mode of the devices can be used to loopback the transmit data to the receive path.

The serial port of the reference design card allows the development/debug PC to monitor the status of the TOCTL's, D3MX, QDSX and BERT chips. This port is also used to program registers for initialization, software reset and diagnostics.

The debug port of the reference design card allows the development/debug PC to load software and monitor the status of the software running on the on-board microprocessor. Software can be downloaded through the debug port or provided via the ROM. This port is required during the software development cycle, and is not required for normal operation of the reference design card.

The serial port of the host processor is used to monitor and control the operation of the FREEDM-32 and the host processor via the development/debug PC.

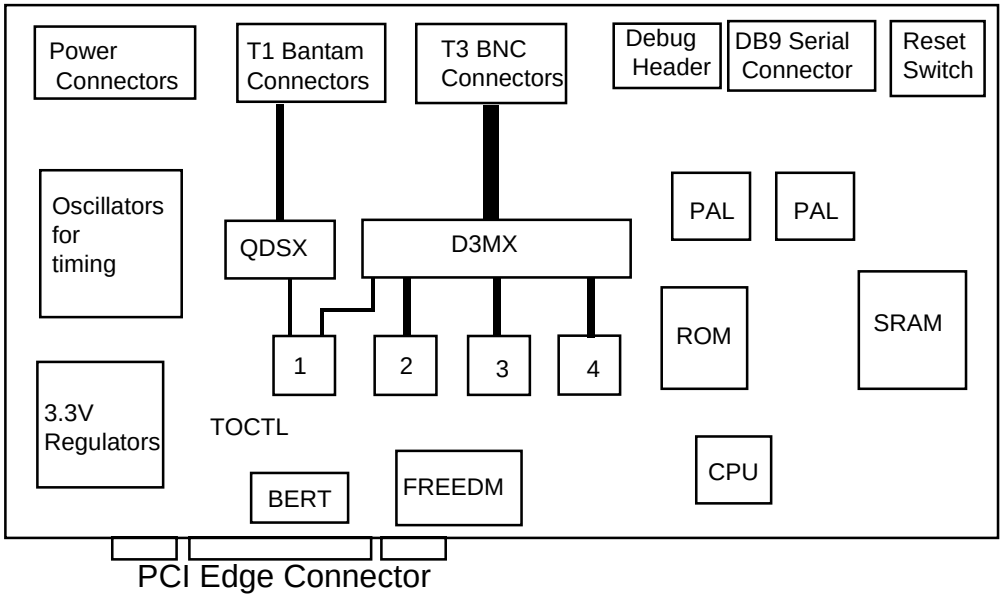
The processor's Ethernet port is provided to download software into the host processor more quickly than can be achieved via the serial port.

4.2 Card Size and Component Placement

The card size does not conform to the height constraints for a PCI add-in card as specified in the PCI specification, but the length of 4.2" meets the constraint of maximum length. Violation of the height constraint for a PCI add-in card is not a problem since the FREEDM-32 is not expected to be used as an add-in card with this density of T1 data streams, instead it is expected to be integrated onto the same board as the host processor. The height has been made larger to illustrate the high density of T1 and channelized T3 links, which can be interfaced to the FREEDM-32.

The card floor plan is shown in figure 6.

Figure 6. Card Floorplan



4.3 PCI Interface

The reference design card supports a 32-bit PCI local bus interface. The PCI edge connector is a universal type allowing it to be plugged into a motherboard that supports either the 5V or the 3.3V signaling environments.

A 3.3V supply is provided to the FREEDM-32 by regulation of the 5V supply at the PCI edge connector.

4.4 Firmware Description

The firmware in the ROM enables the reading and writing to registers. This enables the TOCTL, D3MX, QDSX and BERT devices to be reset, initialized and monitored for errors etc. Please refer to document [7] for more information.

4.5 Schematic Notes

The following is a detailed description of the key functional components shown in the schematics. The actual schematics are included in Appendix A.

Sheet 1: Root Drawing

This sheet provides a block view of the interface signals between each block. The transmit/receive signals are available at the line interfaces within the T3 line interface block or within the T1 interface block. The transmit/receive data streams are terminated within the FREEDM-32 block . The following notes are provided:

- The reset signal from the microprocessor is routed to each device except the FREEDM-32. The FREEDM-32 is reset via the PCI bus, whenever the system is reset, or whenever the FREEDM-32 is reset under software control.
- An on-board microprocessor block provides an interface to program each of the TOCTL, D3MX, QDSX, and BERT registers. It also provides a separate interrupt line for each of the D3MX, QDSX, BERT and the set of TOCTL's.
- The FREEDM-32 is programmed via an host processor at the PCI Interface.
- A JTAG chain connects the FREEDM-32, the TOCTL's, the QDSX, the D3MX and the MC68340.

- The BERT RLOS output is connected to the LED array within the D3MX block.

- The Timing block provides a separate clock trace to each device that requires a clock (i.e. the D3MX, TOCTL's, and the QDSX). This minimizes the adverse effects of reflections on the traces. When a device requires the same clock on multiple pins and the pins are closely spaced then only one trace is used to supply the clock signal.

Sheet 2: FREEDM-32 and PCI Bus Interface

This sheet provides the frame relay processor using the PM7364 (FREEDM-32).

- The PCI Interface is run to a card edge connector. The 3.3V power pins at the edge connector are not used since the commonly available motherboards do not provide power to the 3.3V pins and/or do not provide a 3.3V connector (or combined 5V/3.3V connector) on the motherboard. Instead, the power supply is provided by regulation of +5V as described for sheet 3.

Sheet 3: Power Supply

This sheet contains the 3.3V and the 5V power supplies for the reference design board. It also includes the 0.01uF de-coupling capacitors for the FREEDM-32.

- Connectors (either J1 or J4) supplies the +5V (VCC) and GND from the motherboard power supply. This supply is routed directly to all parts requiring +5V power.

- VCC in supplied the regulator LT1129-5 shown as U22 on the schematic provides +3.3 V power for the TOCTL devices.

- U27 provides a regulated +3.3V supply from the +5V PCI bus power that is used to power the FREEDM-32.

- The TOCTL devices can be powered from either the PCI bus or the motherboard power supply, but not both. Solder bridges SB1, SB2 and SB3 are shorted when the motherboard power supply is chosen. Solder bridges SB4, SB5, and SB6 are shorted when the PCI bus is chosen as the power supply.

Sheet 4,5: T1 Framers - TOCTL

These sheets provide T1 framing for 32 T1 data streams using four PM4388 (TOCTL) devices.

- Capacitors of 0.01uF are used on all power pins for de-coupling the power supply noise.

- Series termination resistors are provided on TLCLK, ICLK, and ECLK to reduce the effects of reflections on the clock edges.

Sheet 6: BERT Diagnotics

This sheet provides a bit error rate tester using the DS2172 (BERT). Pins are connected as per the manufacturers data sheet.

- Commands are provided to this device via software using the microprocessor interface.

- An inverter shown as U30 in the schematic inverts the TBCLK output signal of the FREEDM-32. This is so the BERT can source transmit data during the falling edge of TBCLK, and the FREEDM-32 samples this transmit data on the rising edge of TBCLK, when it is known to be valid.

Sheet 7: M13 Multiplex - D3MX

This sheet provides an M13 multiplexor using the PM8313 (D3MX).

- The quad 2-input multiplexer shown as U4, and the jumper J15, enable the transmit data to be either loop-timed (J15 shorted) or timed via the on-board oscillator (J15 open).

- The 44.736 MHz timing is provided via a 75ohm controlled impedance trace.

- Transmit and receive signals from the T3 line interface are provided via 75 ohm controlled impedance traces.

- An 8-bit line driver shown as U7 in the schematic drives an LED array based on D3MX signal pins RLOS, REXZ, RAIS, ROOF/RRED, and based on the BERT signal pin RLOS. Unused inputs are tied to ground to prevent LED flickering.

- Capacitors of 0.01uF are used on all power pins for de-coupling the power supply noise.

- Series termination resisters are used on RDICLK to reduce the effects of reflections on clock edges.

Sheet 8: T3 Line Interface

This sheet provides an interface to the T3 port using the SSI78P7200 DS-3 Line Interface Transceiver. Resistors and capacitors are connected as outlined in the manufacturer's datasheet for a DS-3 interface.

- The LOWSIGB output is used to gate the receive signals, RPOS and RNEG, whenever the received line signal level is below the threshold - such as when the cable is disconnected from the connector. This prevents upstream circuitry from falsely locking onto data when the receive signal is invalid.

- Jumper J16 at the LBO pin is for the transmitter line build out control. The jumper should set LBO low for cable of 225' or longer, or high for short cable.

- A 75 ohm controlled impedance trace and driver is provided on the RCLK output.

- 75 ohm controlled impedance traces are used for transmit and receive signals.

- Ferrite beads and de-coupling capacitors are provided on power pins to reduce the effects of noise from the power supply.

Sheet 9,10: T1 Line Interface - QDSX

These sheets provide an interface to the four T1 ports using the PM4314 (QDSX).

- Ferrite beads and capacitors on each power pin are provided as necessary to minimize the effects of noise from the power supply.

- Series termination resistors on RCLKO are provided to reduce the effects of reflections on clock edges.

Sheet 11: Timing

This sheet provides timing to the TOCTL's, QDSX and D3MX.

- The 8-bit line drivers shown as U11 and U14 drive separate impedance controlled traces (75 ohm) to each of the TOCTL, D3MX and QDSX device pins.

- The 44.736 MHz oscillator (Y1) provides the T3_CLK signal which indirectly connects to the TICLK pin of the D3MX (This clock is bypassed when JP2 is set for loop-timed operation). The transmit input clock pin (TICLK) provides timing for the transmit direction of the T3 interface.

- The 37.056 MHz oscillator (Y2) provides the XCLK signal. This connects via separate impedance controlled traces to the XCLK pins of the D3MX and the four TOCTL devices. This clock provides a timing reference for the devices and is used for jitter attenuation.

- The 1.544 MHz oscillator Y3 provides the T1_CLK signal. This connects via separate impedance controlled traces to each of the four TOCTL devices. Each trace is routed to CTCLK and CECLK pins of a TOCTL in series to minimize the adverse effects of reflections. This oscillator supplies each TOCTL with the common transmit clock and common egress clock.

Sheet 12: Microprocessor Decode Logic

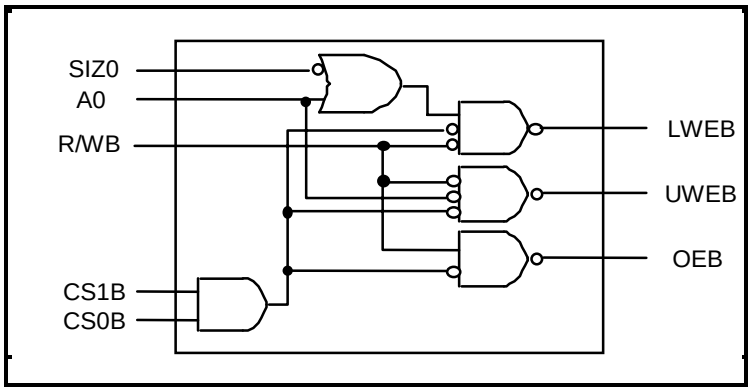
This sheet contains decode logic for the MC68340 that is necessary to interface to the SRAM, the EPROM, the four TOCTL's, the D3MX, the QDSX, and the BERT. The following notes are provided for this sheet:

- Address pins A0 through A17 of the MC68340 address bus is connected to external circuitry. The line drivers provided by U26 serve to minimize loading of the MC68340 address pins A0 through A15. These provide a capacitive load that is well within the tolerable limit of 100pF for the MC68340. The propagation delay for signals passed through the line drivers is within the maximum of 10ns for address valid to address strobe (AS) asserted, or for address valid to chip select (CS0, CS1, CS2, CS3) asserted. U26 drives 16 address pins of the SRAM. EPROM (U34) drives A0 through A10 which are connected to the four TOCTLs, A0 thorough A8 on one QDSX, and A0 through A8 on one D3MX. U33 drives A0 through A7 which is connected to the BERT device.

- The data pins D8 through D15 of the MC68340 are extended to the four TOCTL, the QDSX, and the D3MX via the 8-bit transceiver shown as U24. These same data pins combined with the D0 through to D7 data pins from U25 are extended to the SRAM and EPROM. Data pins D8 through D15 are connected on a multiplexed bus to the BERT via the 8-bit transceiver shown as U32.

- The 128 Kword of SRAM consisting of U16 and U17 is driven for read or write access by decode logic within a 22V10 PAL shown as U10. Figure 7 shows the decode logic based on the MC68340 signals provided to the PAL.

Figure 7. Logic of Signals Provided to SRAM



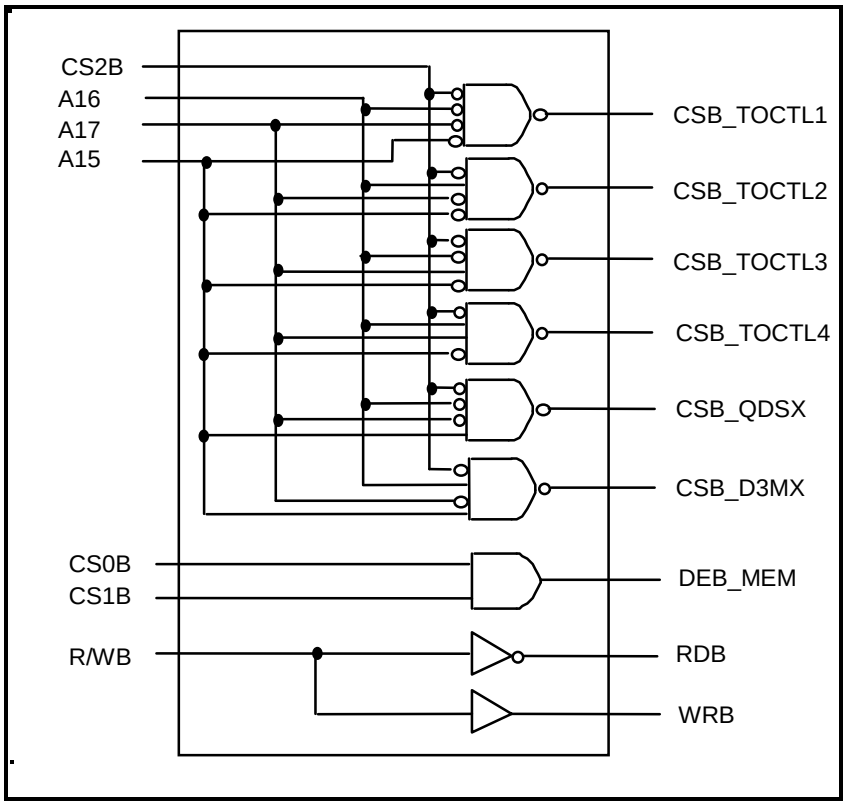
Note: CS1B and CS0B are AND'ed together (i.e. either CS0B or CS1B asserted) since the MC68340 always asserts CS0B during code download into SRAM using the background debug monitor, while it asserts CS1B during normal SRAM accesses. This applies to the case where only the SRAM is being used (typically during code development). If the EPROM is used (which is selected by CS0B), then this AND gate should be removed, and only CS1B should be used here.

- CS0B of the MC68340 provides an active low chip select to the EPROM shown as U15.

- CS2B of the MC68340 provide an active low chip select to the four TOCTL's, the QDSX, and the D3MX using the decode logic shown in figure 8. The decode logic is implemented by the 22V10 PAL shown as U9 in the schematic. The RDB and WRB signals are also derived from the R/WB signal.

- The decode logic of the PAL in figure 8 also provides an output enable to the data transceiver U25 connected to the SRAM and EPROM. CS2B is used as the output enable to the data transceiver U24.

Figure 8. Decode Logic Provided by U9

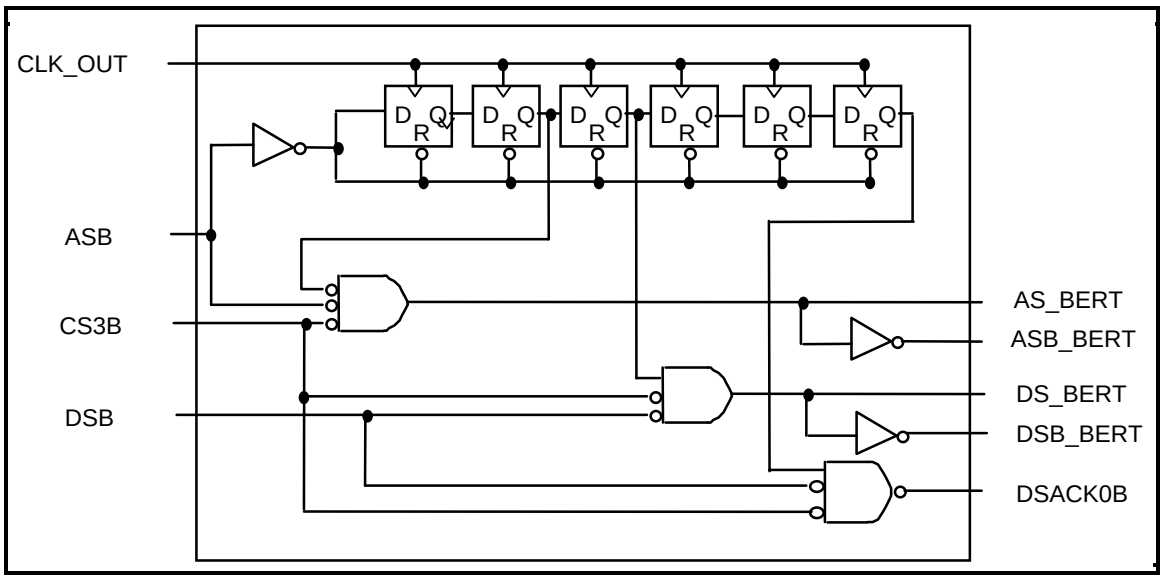


- Wait states are required during read accesses to TOCTL, D3MX and QDSX devices. The datasheet specifies a maximum propagation delay of 80ns, which implies that 1 wait state is necessary to interface the MC68340 with each of these. The wait state is programmed via a register within the MC68340 such that whenever the CS2B is active there is one wait state inserted.

- The BERT has a multiplexed 8-bit address/data bus, which requires the data transceiver, provided by U32, and the address buffer, provided by U33, to interface to the MC68340. The output enables for U32 and U33 is provided by the derived signals ASB_BERT and DSB_BERT.

- The following additional signals are derived to interface the BERT to the MC68340: AS_BERT, DS_BERT, and DSACK0. These signals are derived within a 22V10 PAL shown as U10 in the schematic and an octal D flip flop shown as U23 in the schematic. The logic for the required signals is shown in figure 9.

Figure 9. Decode Logic to Interface BERT



Sheet 13: On-board Microprocessor - MC68340

This sheet contains a 25MHz MC68340 microprocessor, a serial interface for user control and monitoring, a reset circuit, and a debug connector for software development. The following notes are provided for this sheet:

- MAX203 (U8) (+5V supply only, and no external capacitors needed) is used for the RS232 interface. A 3.6864MHz oscillator shown as Y5 is used for the RS232 interface.

- The reset circuit, controlled by switch, SW1, resets the MC68340 and provides RSTB to reset all other devices.

- Background Debug Monitor (BDM) connector, J4, is used for software development. Note that pin BKPTB must be pulled-up to VCC (through 10K). It is recommended that pin BERRB be pulled up also in a similar fashion. CLKOUT from the MC68340 needs to be connected to a test point to be used by the BDM connector. XFC pin of the MC68340 needs to be de-coupled with 0.1uF to ground.

- Other details on the MC68340:

  - XTAL must be left open if external oscillator used for SYSCLK, which is the case in this reference design

  - VCCSYN needs to be pulled up to VCC

  - All unused inputs are pulled up through 10K

- De-coupling Capacitors of 0.01uF are used for each power pin of the MC68340.

5 GLOSSARY

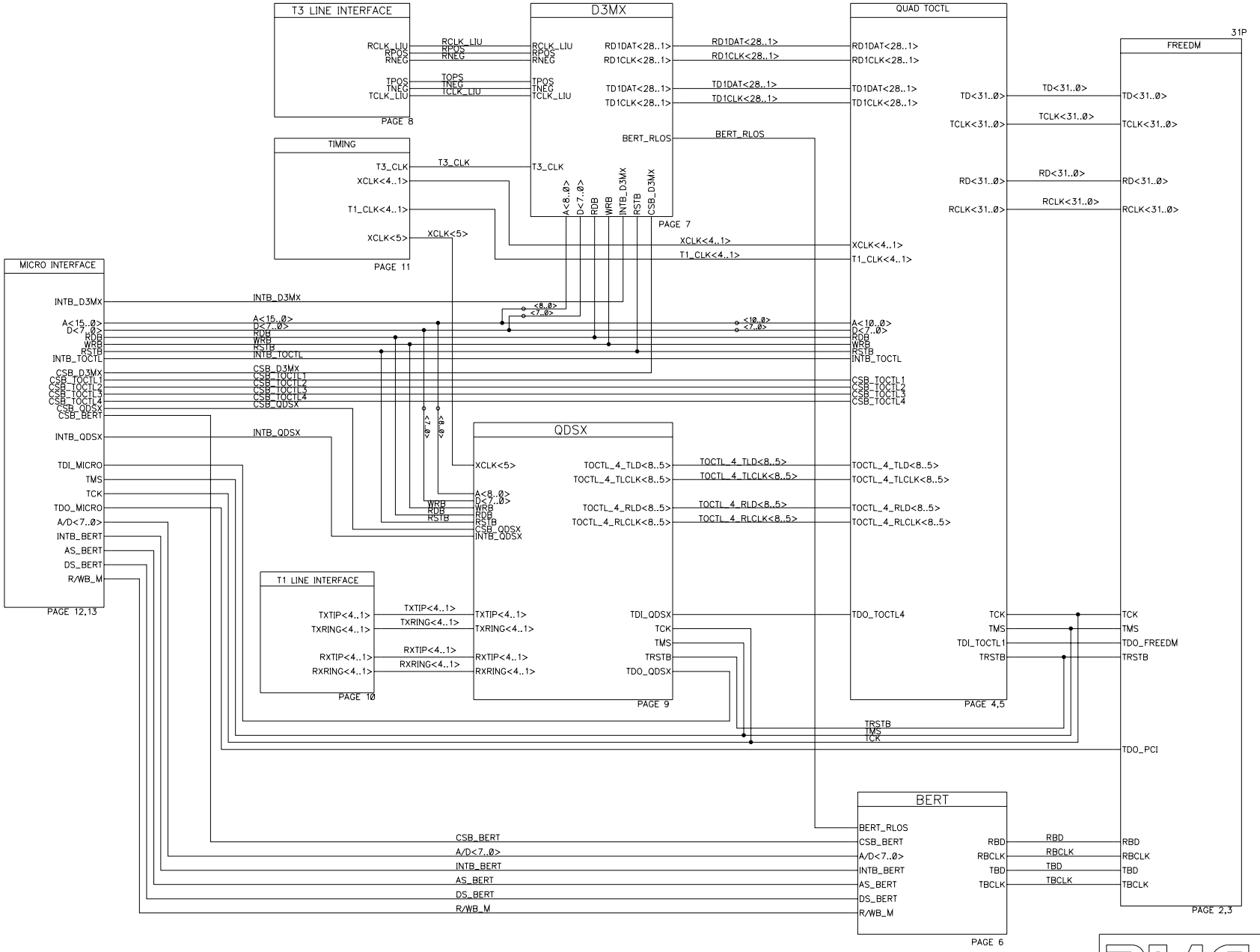
Bit Stuffing	A process in data communications protocols where a string of "one" bits in the data payload is broken by an inserted "zero". The idea of inserting the zero is to ensure that no flag control character is found in the user payload.
CRC	Cyclic Redundancy Check: Check sums generated from recursive algorithms that can be used to determine the integrity of data by a receiver. Certain CRC algorithms allows the receiver to detect as well as correct certain number of bit errors.
DLCI	Data Link Connection Identifier (DLCI): The frame relay virtual circuit number corresponding to a particular destination which is part of the frame relay header and is usually ten bits long. The DLCI is typically associated with a particular PVC on the network.
DS-0	Digital Service, level 0: There are 24 DS-0 channels in a DS-1. Each DS-0 has a bandwidth of 64 Kbit/s.
DS-1	Digital Service, level 1: It is 1.544 Mbit/s in North America. In channelized mode, each DS-1 consists of 24 DS-0 channels. In unchannelized mode, each DS-1 has a full-duplex bandwidth of 1.544 Mbit/s.
DS-3	Digital Service, level 3: DS-3 is equivalent to 28 DS-1 channels. It operates at 44.736 Mbit/s.
DSLAM	Digital Subscriber Loop Access Multiplexer.
FCS	Frame Check Sequence: Bits added to the end of a frame for error detection. In bit-oriented protocols, a frame check sequence is a 16-bit field added to the end of a frame that contains transmission error-checking information.
Flag	In synchronous transmission, a flag is a pattern of "01111110" used to mark the beginning and end of a frame.
FRAD	Frame Relay Access Device.

Frame	A frame is also referred to as a "packet" and is a logical transmission unit. A frame consists of a group of data bits in a specific format. Generally, a flag is used at each end of the frame to delimit the start and end of the frame.
Frame Relay	The term "frame relay" is used in multiple contexts and can be used to refer to a switching technology, an interface standard or a set of data services.
Full-Duplex	Refers to simultaneous transmission in two directions.
FUNI	Frame Relay User Network Interface
HDLC	High Level Data Link Control: A standard bit-oriented protocol developed by ITU.
HSSI	High Speed Serial Interface
ISP	Internet Service Provider:
Multiplexor	Electronic equipment which allows two or more signals to pass over one communication circuit.
NAP	Network Access Point:
OSI	Open System Interconnect: An ISO publication that defines seven independent layers of communication protocols. Each layer enhances the communication services of the layer just below it and shields the layer above it from the implementation details of the lower layer.
OSI Model	The only internationally accepted framework of standards for communication between different systems made by different vendors. The OSI model organizes the communications process into the following seven layers: Layer 1 - Physical Layer Layer 2 - Data Link Layer Layer 3 - Network Layer Layer 4 - Transport Layer Layer 5 - Session Layer Layer 6 - Presentation Layer Layer 7 - Application Layer
Packet	A packet is also referred to as a "frame" and is a logical transmission unit.
PCI	Peripheral Component Interconnect

POP	Point of Presence: In telecommunication, POP refers to the physical place within a LATA where a long distance carrier interfaces with the network of the local exchange carrier.
UNI	User Network Interface: The physical and electrical demarcation point between the user and the public network service provider.

6 APPENDIX A. SCHEMATICS, LAYOUT

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING

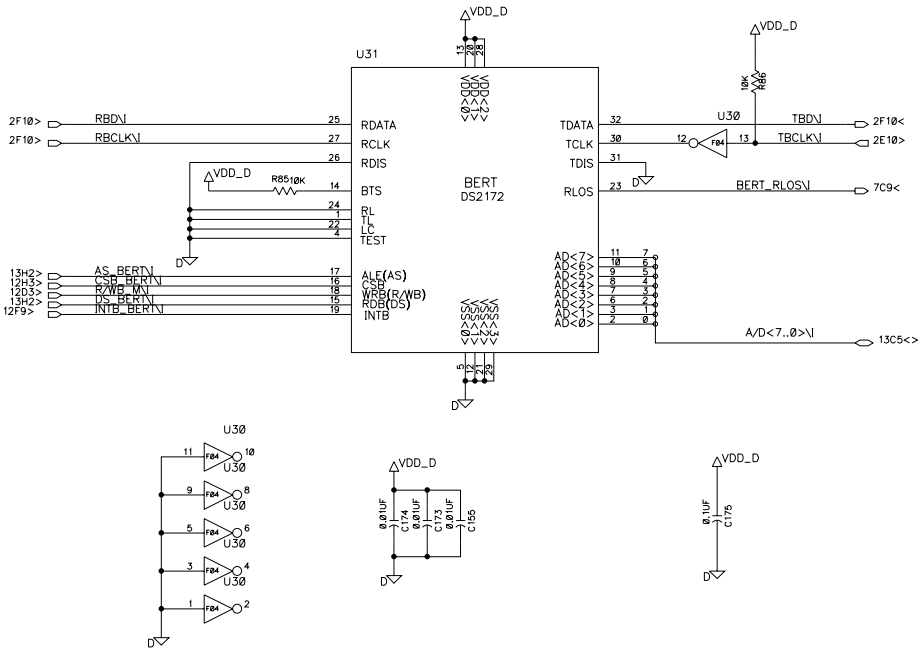
TITLE=FREEDM_ROOT
ABBREV=FREEDM_ROOT
LAST_MODIFIED=Tue Sep 9 12:23:47 1997

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN ROOT DRAWING	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 1 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

BERT



DRAWING

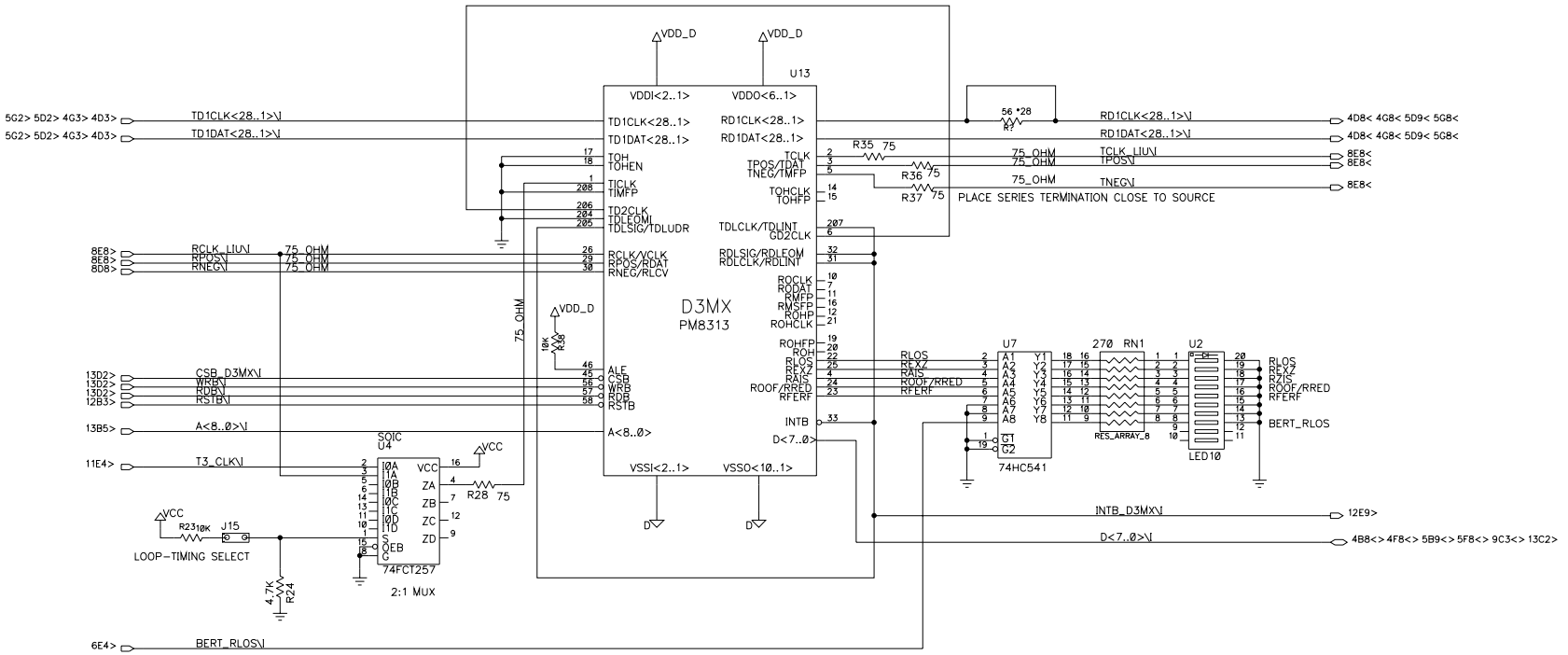
TITLE=BERT
ABBREV=BERT
LAST_MODIFIED=Fri Oct 17 16:17:10 1997

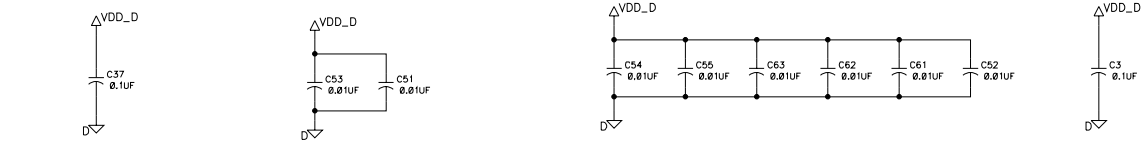
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN BERT	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 6 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

M13 MULTIPLEXER/DEMULTIPLEXER





DECOUPLING CAPS FOR FCT257

DECOUPLING CAPS FOR VDDI

DECOUPLING CAPS FOR VDDO

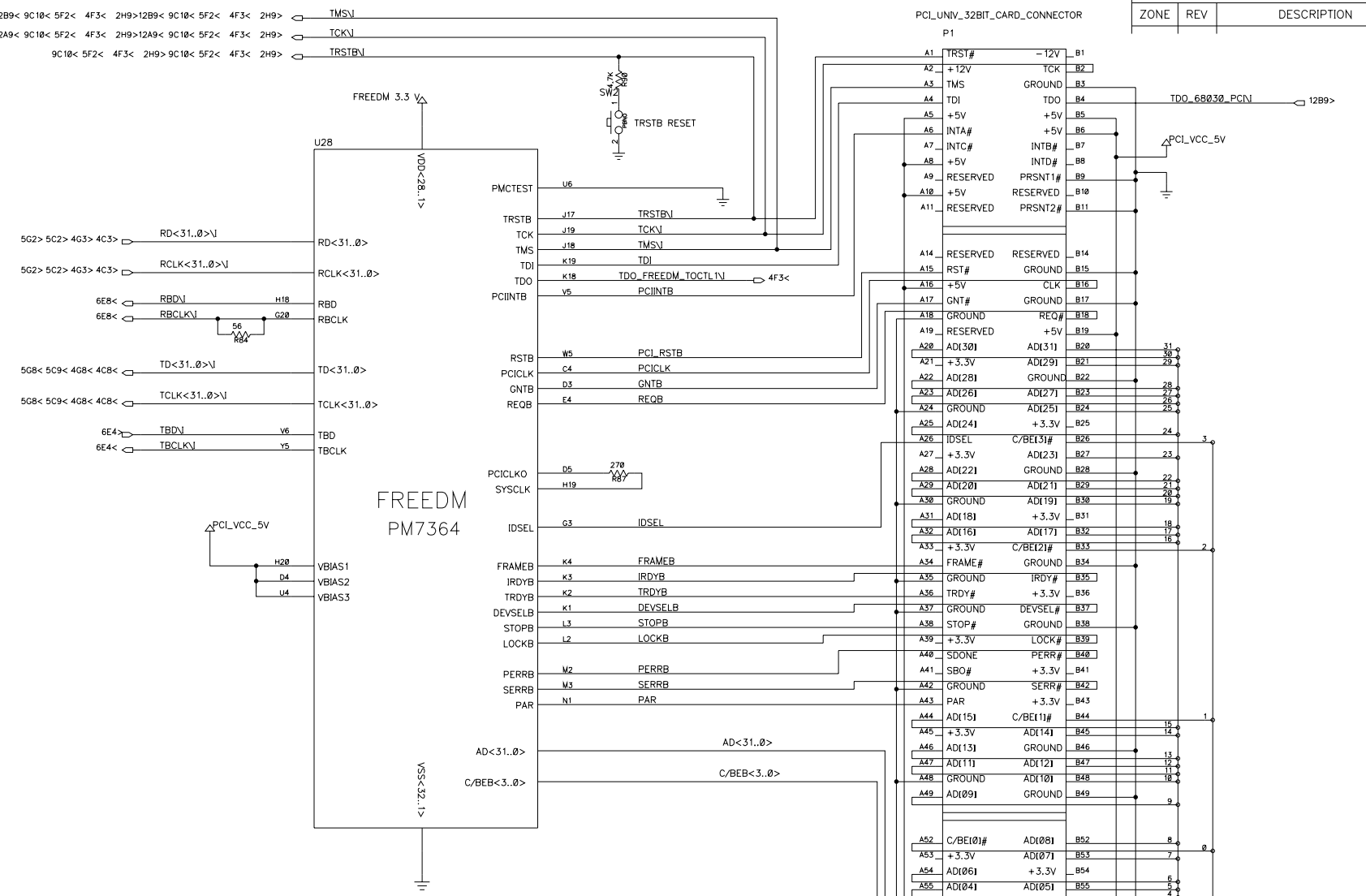
DECOUPLING CAPS FOR 541

DRAWING

TITLE=D3MX_BLOCK
ABBREV=D3MX
LAST_MODIFIED=Fri Oct 17 16:17:31 1997

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN D3MX	DATE: FEB 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 7 OF 13



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

NOTE

CHECK THE LATEST PCI SPEC FOR
COMPONENT AND LAYOUT RESTRICTIONS

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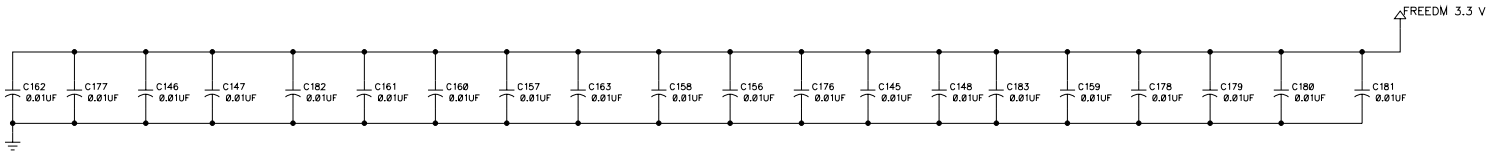
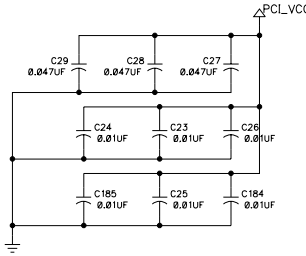
DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN FREEDM & PCI CONNECTOR	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 2 OF 13

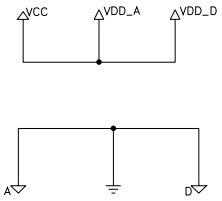
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

DECOUPLING CAPS FOR FREEDM VDD

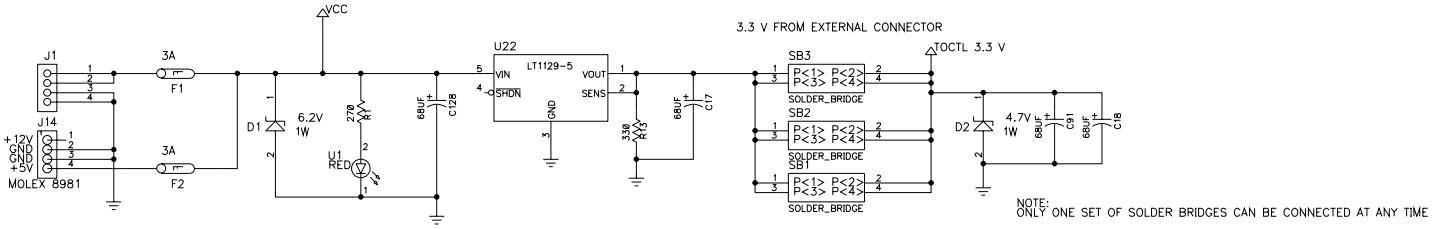


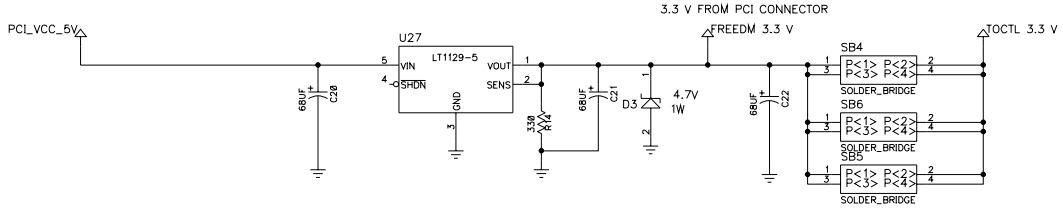


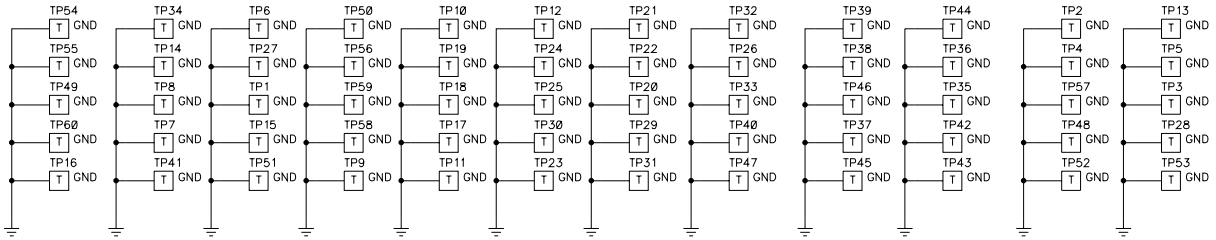
NOTE:
THE FOLLOWING DECOUPLING CAPS ARE USED FOR PCI BUS POWER RAIL. THEY SHOULD BE PLACED IN SUCH A WAY THAT AT LEAST AN AVERAGE OF Ø.Ø1UF PER VCC PIN IS ACHIEVED.



SINGLE GROUND PLANE USED







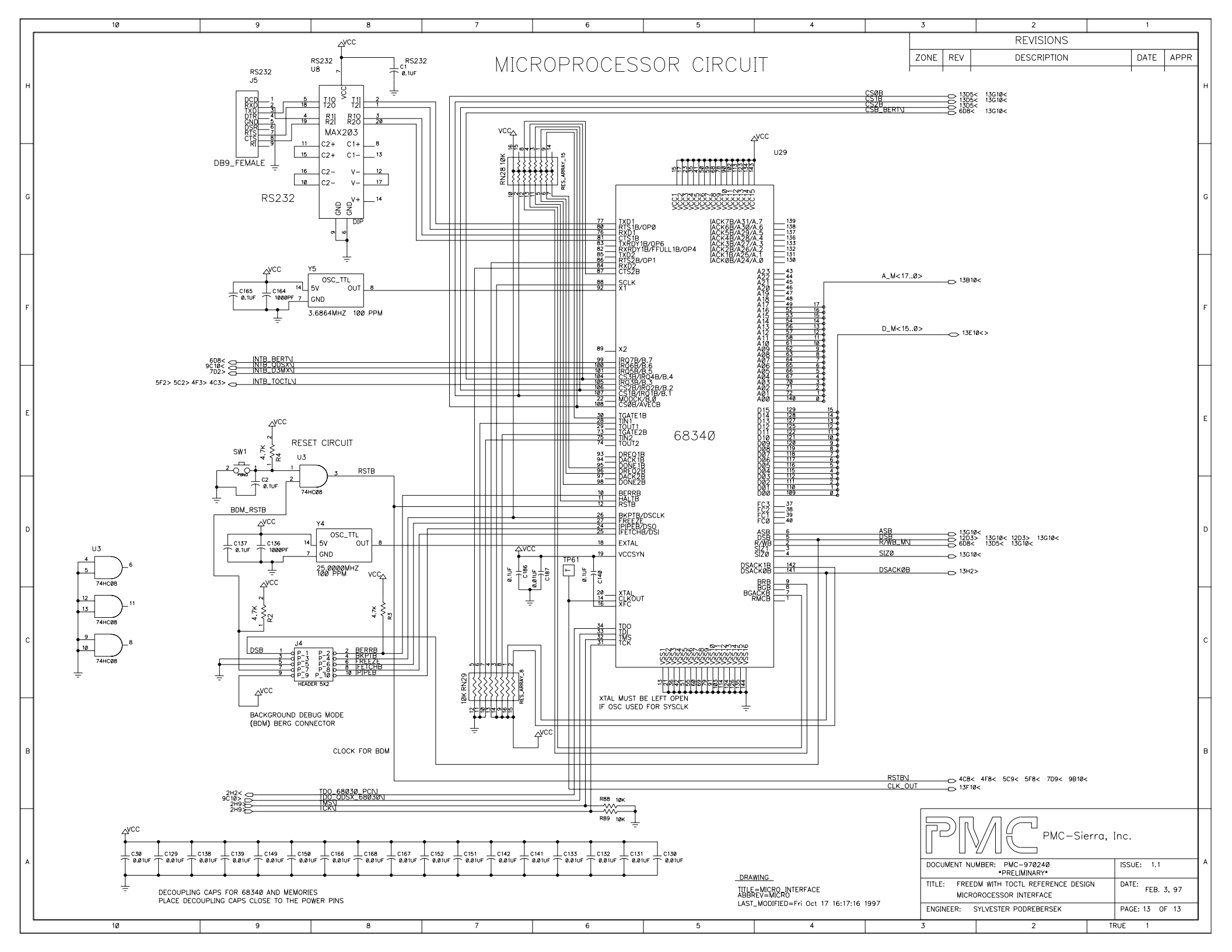
DRAWING
TITLE=FREEDM_BLOCK
ABBREV=FREEDM
LAST_MODIFIED=Fri Oct 17 16:17:27 1997

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN POWER AND DECOUPLING CAPS	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 3 OF 13

MICROPROCESSOR CIRCUIT

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

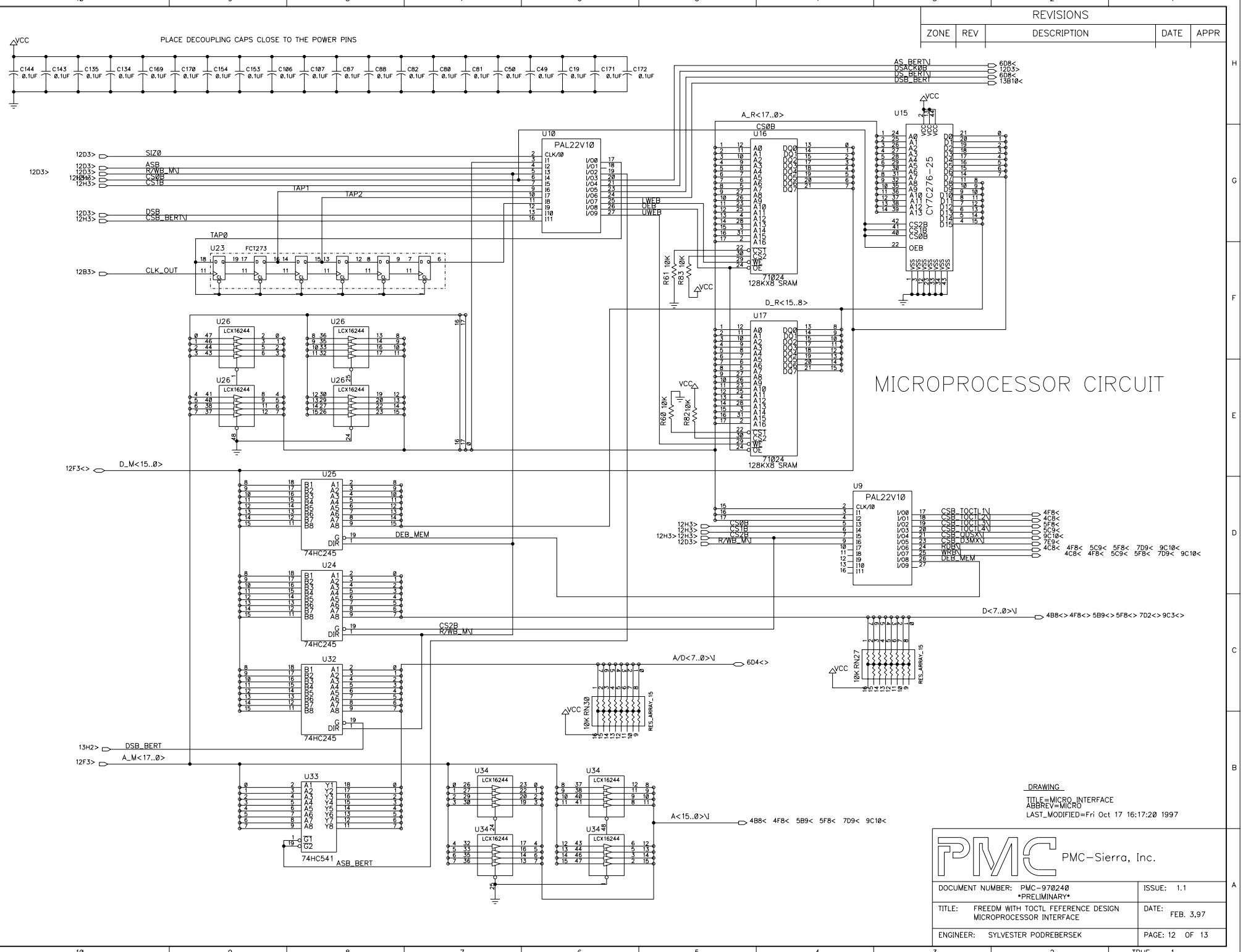


DRAWING

TITLE=MICRO_INTERFACE
ABBREV=MICRO
LAST_MODIFIED=Fri Oct 17 16:17:16 1997

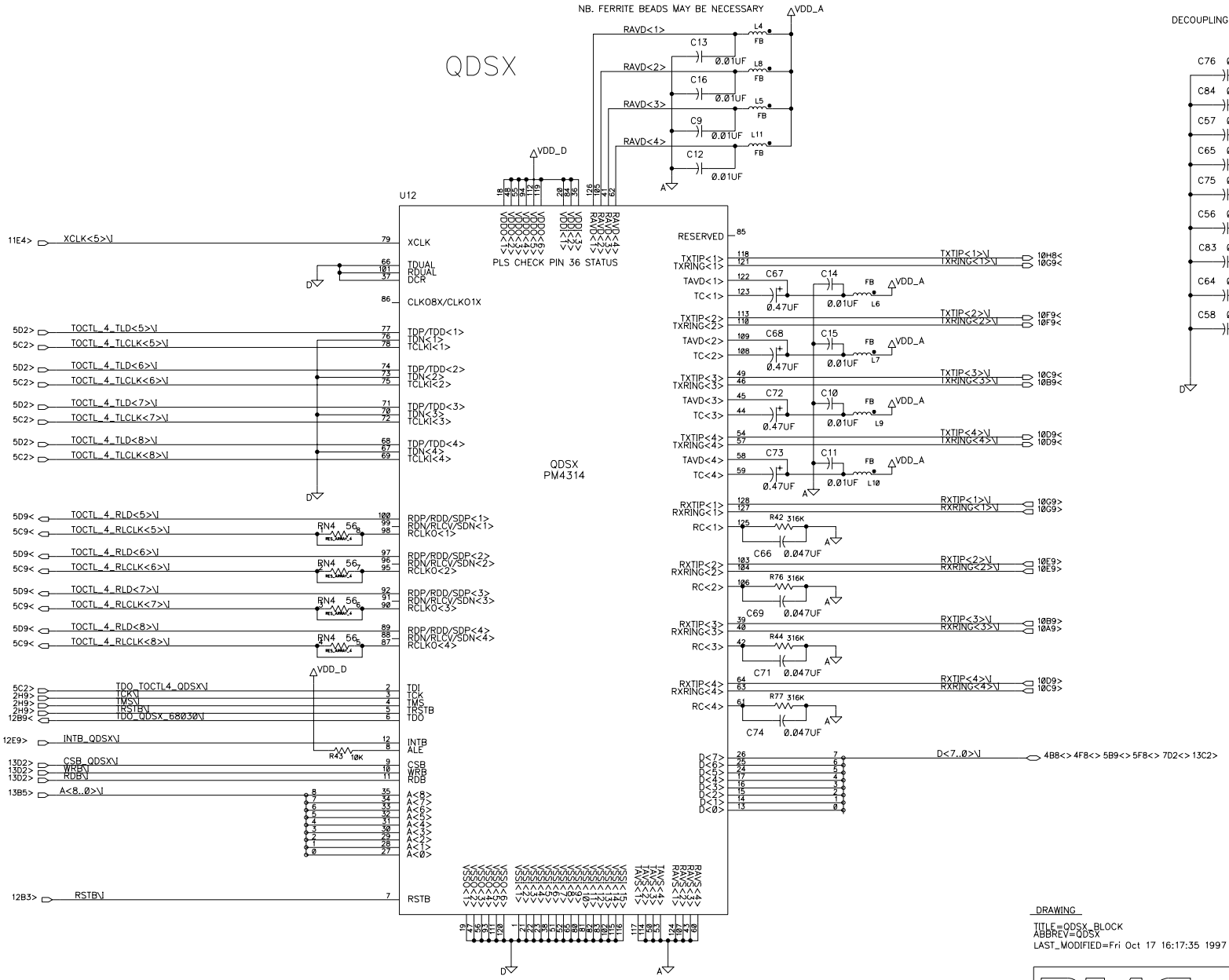
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN MICROROCESSOR INTERFACE	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 13 OF 13


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
PLACE DECOUPLING CAPS CLOSE TO THE POWER PINS
MICROPROCESSOR CIRCUIT
U10 PAL22V10
U15 CY7C276-25
U16 71024 128KX8 SRAM
U17 71024 128KX8 SRAM
U9 PAL22V10
U23 FCT273
U25 74HC245
U24 74HC245
U32 74HC245
U33 74HC541
U26 LCX16244
U34 LCX16244
R61 10K
R83 10K
R60 10K
R82 10K
10K RN30
10K RN27
RES_ARRAY_15
SIZ0
ASB
R/WB_M\I
CS0B
CS1B
DSB
CSB_BERT\I
TAP1
TAP2
TAP0
CLK_OUT
LWEB
OEB
UWEB
AS_BERT\I
DSACK0B
DS_BERT\I
DSB_BERT
A_R<17..0>
D_R<15..8>
D_M<15..0>
DEB_MEM
CS2B
A/D<7..0>\I
D<7..0>\I
A_M<17..0>
A<15..0>\I
ASB_BERT
CSB_TOCTL1\I
CSB_TOCTL2\I
CSB_TOCTL3\I
CSB_TOCTL4\I
CSB_DUDX\I
CSB_D3MX\I
RDB\I
WRB\I
DRAWING
TITLE=MICRO_INTERFACE
ABBREV=MICRO
LAST_MODIFIED=Fri Oct 17 16:17:20 1997
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*
ISSUE: 1.1
TITLE: FREEDM WITH TOCTL FEFERENCE DESIGN MICROPROCESSOR INTERFACE
DATE: FEB. 3,97
ENGINEER: SYLVESTER PODREBERSEK
PAGE: 12 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

QDSX



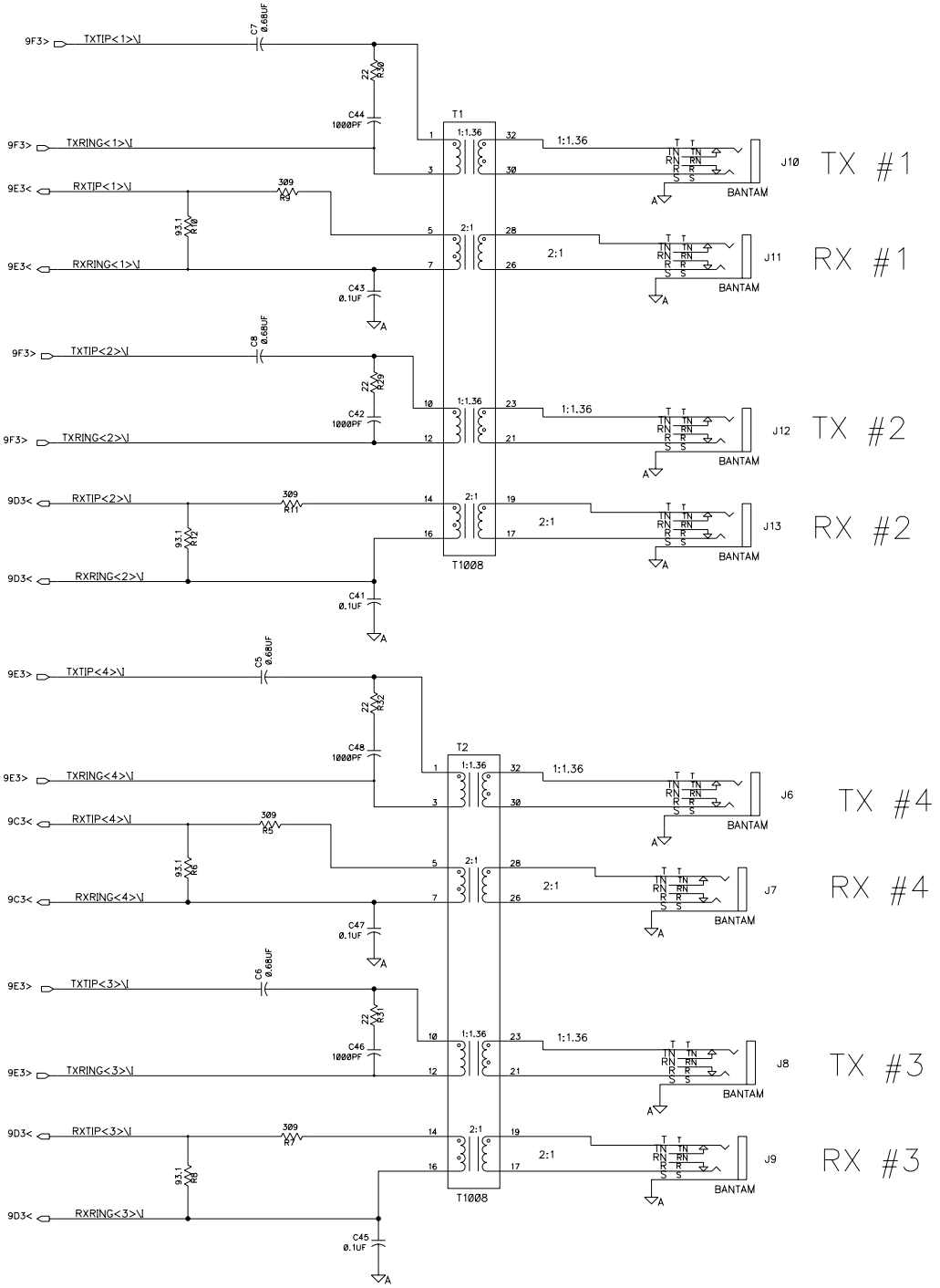
DRAWING

TITLE=QDSX_BLOCK
ABBREV=QDSX
LAST_MODIFIED=Fri Oct 17 16:17:35 1997

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN QDSX	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 9 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



LINE INTERFACE TRANSMIT/RECEIVE

DRAWING TITLE=T1_LINE_INTERFACE
ABBREV=T1_LIU

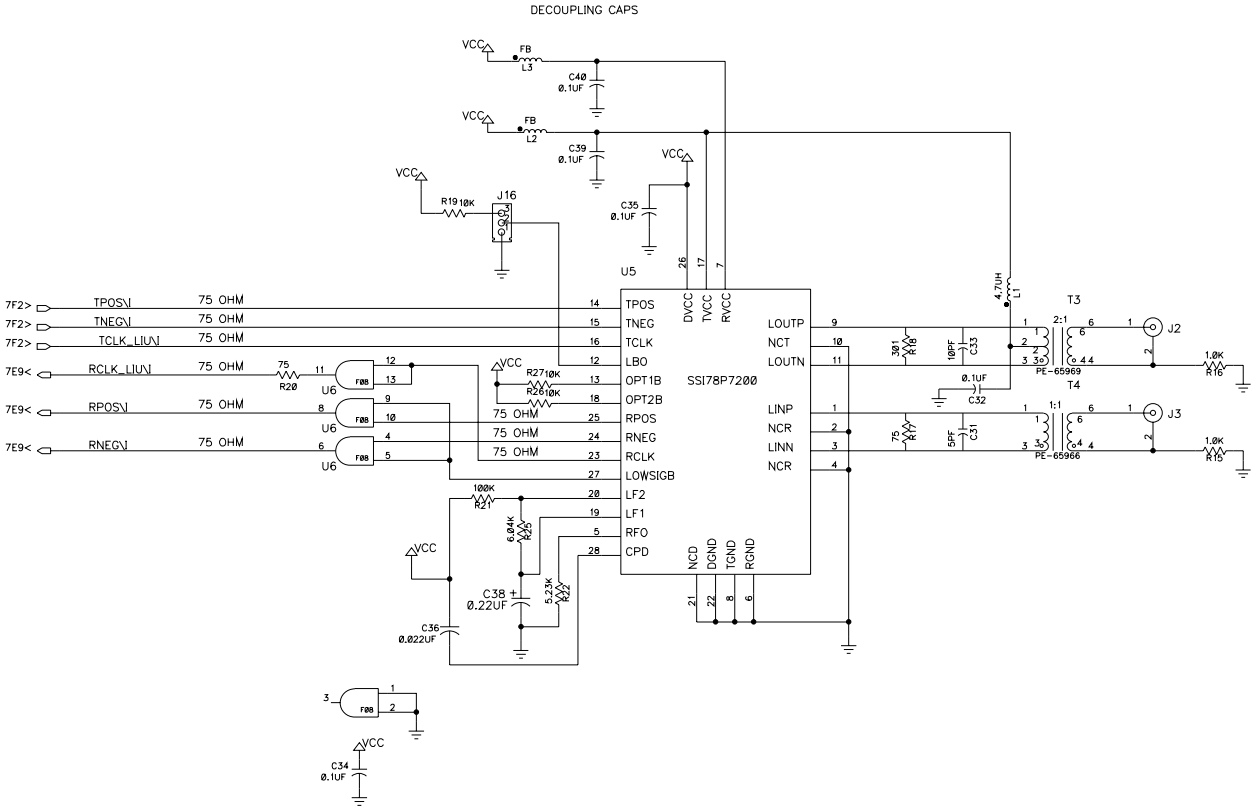
LAST_MODIFIED=Fri Oct 17 16:17:08 1997

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN T1 LINE INTERFACE TRANSMIT/RECEIVE	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 10 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

T3 LINE INTERFACE



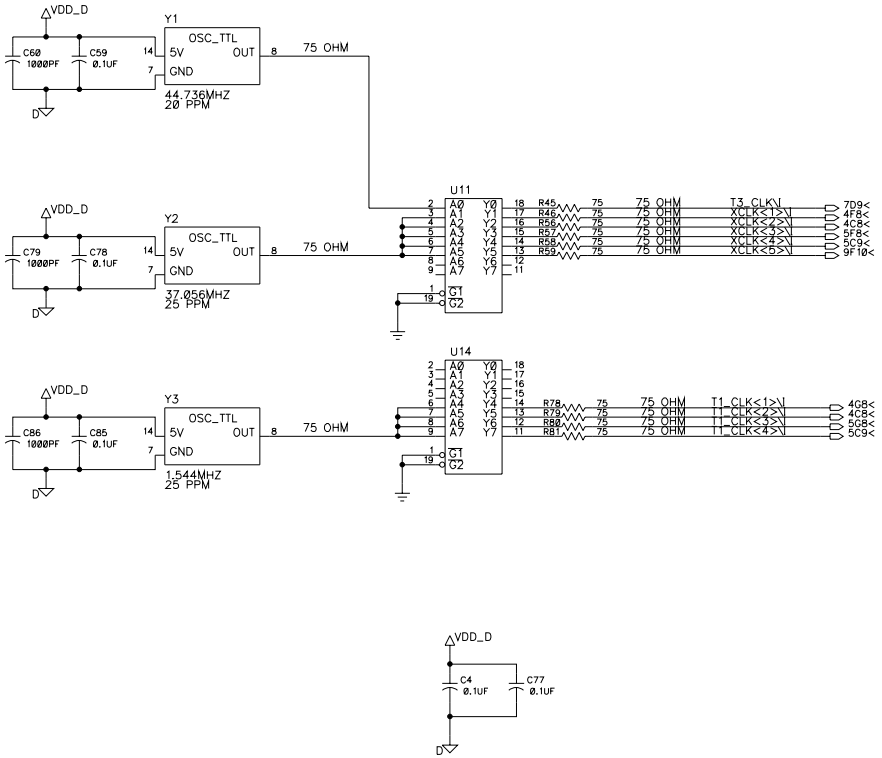
DRAWING

TITLE=T3_LINE_INTERFACE
ABBREV=T3_LIU
LAST_MODIFIED=Fri Oct 17 16:17:06 1997

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN T3_LINE_INTERFACE	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 8 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING

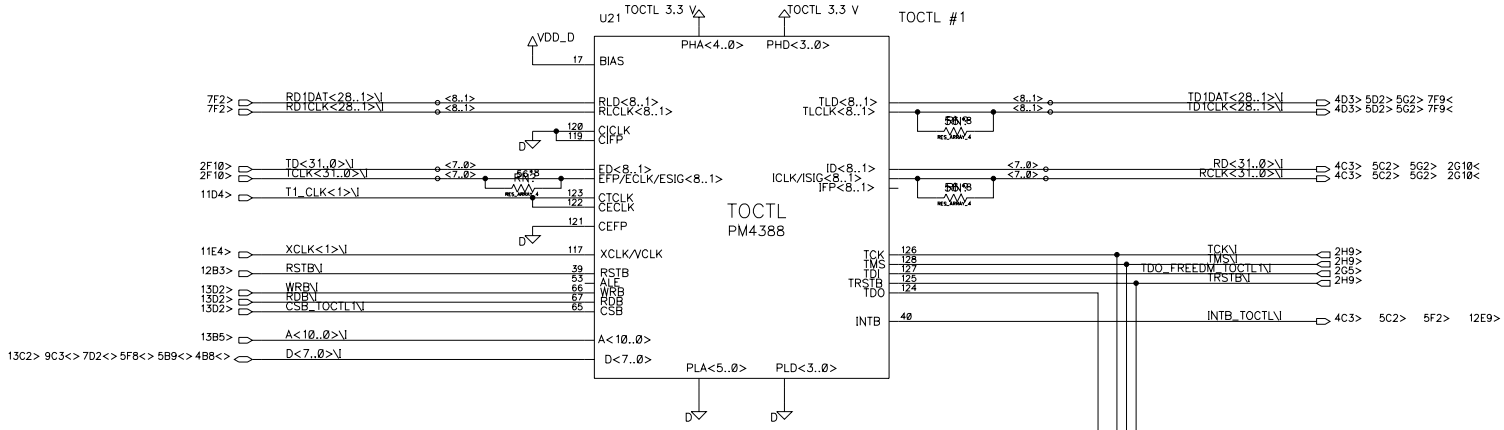
TITLE=TIMING
ABBREV=TIMING
LAST_MODIFIED=Fri Oct 17 16:17:12 1997

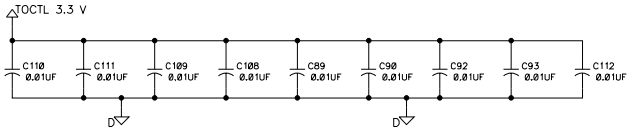
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN TIMING	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 11 OF 13

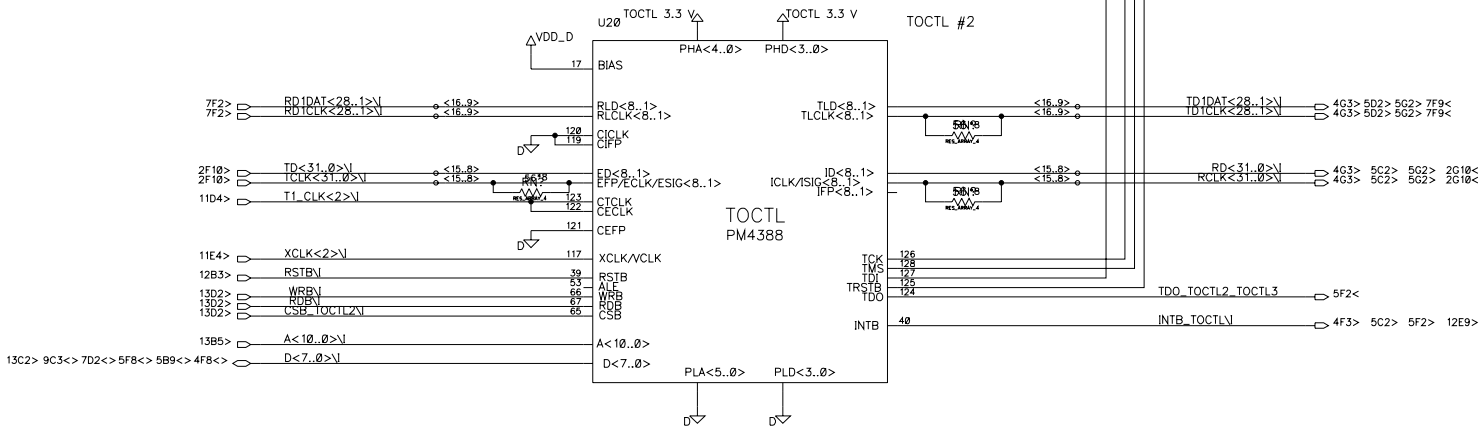
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

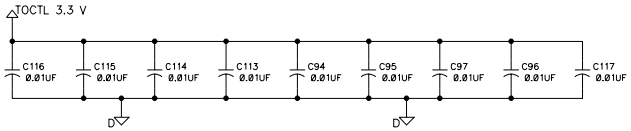
OCTAL T1 FRAMER





NOTE: PLACE ALL DECOUPLING CAPS NEAR POWER PINS





NOTE: PLACE ALL DECOUPLING CAPS NEAR POWER PINS

DRAWING

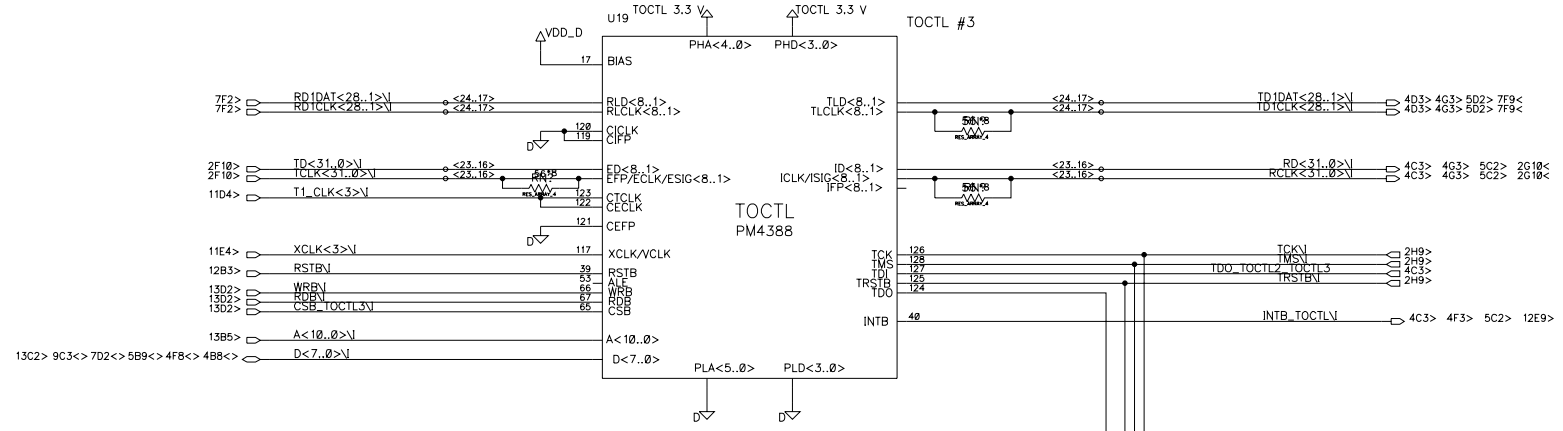
TITLE=TOCTL_BLOCK
ABBREV=TOCTL
LAST_MODIFIED=Fri Oct 17 16:17:01 1997

PMC-Sierra, Inc.

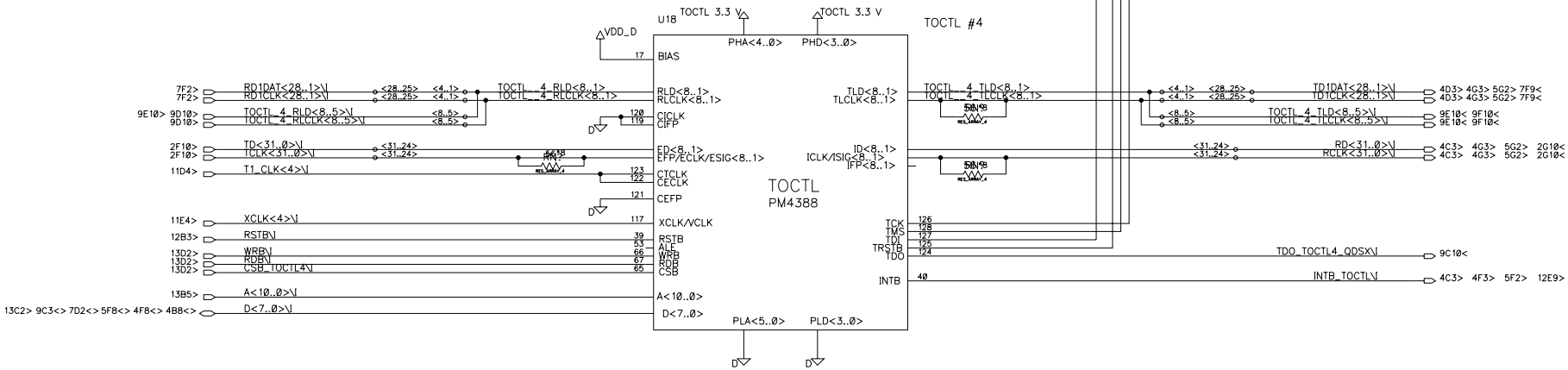
DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN QUAD TOCTLS	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 4 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

OCTAL T1 FRAMER



NOTE: PLACE ALL DECOUPLING CAPS NEAR POWER PINS



NOTE: PLACE ALL DECOUPLING CAPS NEAR POWER PINS

DRAWING

TITLE=TOCTL_BLOCK
ABBREV=TOCTL
LAST_MODIFIED=Fri Oct 17 16:17:03 1997

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240 *PRELIMINARY*	ISSUE: 1.1
TITLE: FREEDM WITH TOCTL REFERENCE DESIGN QUAD TOCTLS	DATE: FEB. 3, 97
ENGINEER: SYLVESTER PODREBERSEK	PAGE: 5 OF 13

7 APPENDIX B: BILL OF MATERIALS

Item	Description	Vendor Part No.	Reference Designator	QTY
1	128K BY 8 STATIC RAM	FAI.ELECTRONICS IDT71024S15TY	U16, U17	2
2	HEX INVERTER (SOIC-14)	DIGI-KEY 74F04SC-ND	U30	1
3	QUAD 2 INPUT AND GATE (SOIC –14)	DIGI-KEY 74F08SC-ND	U6	1
4	QUAD 2 INPUT MUX (SOIC-16)	DIGI-KEY PI74FCT257ATS-ND	U4	1
5	QUAD D FLIP FLOP WITH RESET (SOIC-20)	DIGI-KEY P174FCT273ATS-ND	U23	1
6	NON-INV OCTAL BUFFER/LINE DRIVER (SOIC-20)	DIGI-KEY PI74FCT541ATS-ND	U11, U14	2
7	16 BIT BIDIRECTIONAL TRANSCEIVER (48 SSQP)	DIGI-KEY 74LCX16244MEA-ND	U26, U34	2
8	QUAD 2 INPUT AND GATE (SOIC-14)	DIGI-KEY MM74HC08M-ND	U3	1
9	OCTAL TRI STATE BUS TRANSCEIVER (SOIC-20)	DIGI-KEYMM74HC245AWM-ND	U24, U25, U32	3
10	OCTAL TRI STATE BUFFER	DIGI-KEY MM74HC541N-ND	U7, U33	2
11	ADC BANTAM CONNECTORS	ELECTROSONIC PC83J(BLACK)	J6-J13	8
12	BNC CONNECTOR (RIGHT ANGLE)	DIGI-KEY ARF1065-ND	J2, J3	2
13	CAPACITOR 10000PF	DIGIKEY PCC103BNCT-ND	C9-C16, C56-C58, C64, C65, C75, C76, C83, C84	17
14	CAPACITOR 47000PF	DIGIKEY PCC473BCT-ND	C66, C69, C71, C74	4
15	CAPACITOR POL-0.47UF, 25V, TANT A	DIGI-KEY PCT5474CT-ND	C67, C68, C72, C73	4
16	CAPACITOR POL-10UF, 16V, TANT THE	DIGI-KEY PCT3106CT-ND	C70	1
17	CAPACITOR-0.001UF	DIGI-KEY PCC102CGCT-ND	C42, C44, C46, C48, C60, C79, C86, C136, C164	9
18	CAPACITOR-0.01UF, 50V, X7R_805	DIGI-KEY PCC103BNCT-ND	C23-C26, C30, C51-C55, C61-C63, C89, C90, C92-C105, C108-C127, C129-C133, C138, C139,	91

			C141, C142, C145-C152, C155-C163, C166-C168, C173, C174, C176-C185, C187	
19	CAPACITOR-0.022UF, 50V, X7R_805	DIGI-KEY PCC223BGCT-ND	C36	1
20	CAPACITOR-0.047UF, 50V, X7R_1206	DIGI-KEY PCC473BCT-ND	C27-C29	3
21	CAPACITOR-0.1UF, 50V, X7R_1206	DIGI-KEY PCC104BCT-ND	C1-C4, C19, C32, C34, C35, C37, C39-C41, C43, C45, C47, C49, C50, C59, C77, C78, C80-C82, C85, C87, C88, C106, C107, C134, C135, C137, C140, C143, C144, C153, C154, C165, C169-C172, C175, C186	43
22	CAPACITOR-0.22UF, 35V, TANT THE	DIGI-KEY PCT6224CT-ND	C38	1
23	CAPACITOR-0.68UF, 16V, Y5V_805	NEWAEK 52F007	C5-C8	4
24	CAPACITOR-10PF, 50V, NPO_805	DIGI-KEY PCC100CNCT-ND	C33	1
25	CAPACITOR-5PF, 50V, NPO_805	DIGI-KEY PCC050CNCT-ND	C31	1
26	CAPACITOR-68UF, 6.3V, TANT THE	DIGI-KEY PCT1686CT-ND	C17, C18, C20-C22, C91, C128	7
27	CYPRESS 16K X 16 PROM	ARROW-ELECTRONICS CY7C276-25J-CCYPRESS REPROGRAMMABLE	U15	1
28	D3MX (M13 MULTIPLEXER)	PM8313	U13	1
29	DB9 FEMALE CONNECTR	DIGI-KEY A2100-ND	J5	1
30	DIODEZENER_SMD-4.7V, 1W	DIGI-KEY ZM4732ACT-ND	D2, D3	2
31	DIODEZENER_SMD-6.2V, 1W	DIGI-KEY ZM4735ACT-ND	D1	1
32	DALLAS BERT 32 PIN TQFP	FAI ELECTRONICS DS2172	U31	1
33	FREEDM-32 (FRAME RELAY PROTOCOL ENGINER AND DATA LINK MANAGER)	PM7364	U28	1
34	FUSE 3A	DIGI-KEY F1147TR-ND	F1, F2	2
35	1 X 2 JUMPER	DIGI-KEY S101136-ND	J15	1
36	2 X 5 JUMPER	DIGI-KEY S201236-ND	J4	1
37	1 X 3 JUMPER	DIGI-KEY S101136-ND	J16	1

38	INDUCTOR-4.7UH	DIGI-KEY PCD1236CT-ND	4.7UH	1
39	INDUCTOR-FB, 50, FAIR RITE	FAIR RITE 2743019447	L2-L11	10
40	LED-RED, PCB RIGHT ANGLE	DIGI-KEY LU20091-ND	U1	1
41	RED LED10, 25MA, 2.1V	DIGI-KEY LT1066-ND	U2	1
42	3A LOW DROPOUT LINEAR TECHNOLOGY REGULATOR	ARROW-ELECTRONICS LT1528CQ-LINEAR TECHNOLOGY	U22, U27	2
43	RS2332 TRANSCEIVER	DIGI-KEY MAX203CPP-ND	U8	1
44	MC68340 MOTOROLA CPU	FAI-ELECTRONICS MC68340FE25E	U29	1
45	P.C. DISK DRIVE POWER CONNECTOR	MOLEX 8981-4R-1	J14	1
46	OSC_TTL DIP-1.544MHZ, 25 PPM, CHA	CONNOR WINFIELD HC13R8	Y3	1
47	OSC_TTL DIP-25.0000MHZ, 100 PPMA	DIGI-KEY CTX176-ND	Y4	1
48	OSC_TTL DIP-3.6864MHZ, 100 PPM, A	DIGI-KEY CTX154-ND	Y5	1
49	OSC_TTL DIP-37.056MHZ, 25 PPM, CA	CONNOR WINFIELD HC13R8	Y2	1
50	OSC_TTL_DIP-44.736MHZ, 20 PPM, CA	CONNOR WINFIELD HC54R8	Y1	1
51	PAL	FAI-ELECTRONICS PALCE22V10H-5JC	U9, U10	2
52	RESET SWITCH	DIGI-KEY CKN4002-ND	SW1	1
53	1:1 LINE TRANSFORMER FOR T3 RECEIVE	SAGER ELECTRICAL SUPPLY PE65966	T4	1
54	1:2 LINE TRANSFORMER FOR T3 TRANSMIT	SAGER ELECTRICAL SUPPLY PE65969	T3	1
55	POWER BLOCK CONNECTR	FUTURE ACTIVE INDUSTRIAL ELECTRIC 15-24-4041	J1	1
56	QDSX (QUAD T1/E1 LINE INTERFACE)	PM4314	U12	1
57	RESISTOR-1.0K, 5%, 805	DIGI-KEY P1.0KABK-ND	R15, R16	2
58	RESISTOR-100K, 5%, 805	DIGI-KEY P100KABK-ND	R21	1
59	RESISTOR-10K, 5%, 805	DIGI-KEY P10KABK-ND	R19, R23, R26, R27, R38, R43, R60, R61, R82, R83, R85, R86, R88, R89	14
60	RESISTOR-22, 5%, 805	DIGI-KEY P22ABK-ND	R29-R32	4
61	RESISTOR-270, 5%, 805	DIGI-KEY P270ABK-ND	R1, R87	2

62	RESISTOR-301, 1%, 805	DIGI-KEY P301CCT-ND	R18	1
63	RESISTOR-309, 1%, 805	DIGI-KEY P309CCT-ND	R5, R7, R9, R11	4
64	RESISTOR-316K, 1%, 805	DIGI-KEY P316CCT-ND	R42, R44, R76, R77	4
65	RESISTOR-330, 5%, 805	DIGI-KEY P330ABK-ND	R13, R14	2
66	RESISTOR-4.7K, 5%, 805	DIGI-KEY P4.7KABK-ND	R2-R4, R24	4
67	RESISTOR-5.23K, 1%, 805	DIGI-KEY P5.23CCT-ND	R22	1
68	RESISTOR-56, 5%, 805	DIGI-KEY P56ABK-ND	R33, R34, R39-R41, R47-R55, R62-R75, R84	29
69	RESISTOR-6.04K, 1%, 805	DIGI-KEY P6.04KCCT-ND	R25	1
70	RESISTOR-75, 1%, 805	DIGI-KEY P75CCT-ND	R35-R37, R78, R79	5
71	RESISTOR-75, 5%, 805	DIGI-KEY P75ABK-ND	R17, R20, R28, R45, R46, R56-R59, R80, R81	11
72	RESISTOR-93.1, 1%, 805	DIGI-KEY P93.1CCT-ND	R6, R8, R10, R12	4
73	RES_ARRAY_15_SMD-10K	DIGI-KEY 766-161-R1OK-ND	RN27, RN28, RN30	3
74	RES_ARRAY_4_SMD-56	DIGI-KEY Y456-ND	RN2-RN26	25
75	RES_ARRAY_8_SMD-10K	DIGI-KEY 766-163-10KR-ND	RN29	1
76	RES_ARRAY_8_SMD-270	DIGI-KEY 766-163-R270-ND	RN1	1
77	SSI78P7200_PLCC-BASE	SILICON-SYSTEMS SS178P7200-IH	U5	1
78	QUAD T1 TRANSFORMER	PULSE - T1008	T1, T2	2
79	TOCTL (OCTAL T1 FRAMER)	PM4388	U18-U21	4

NOTES

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PMC 970240 Issue date September 1997