APPS MULTI-PHY ADAPTER

SCI-PHY TO MULTI-PHY ADAPTER CARD

REFERENCE DESIGN

RELEASED

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- Direct SCI-PHY to multi-PHY connection.

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- Interconnect 2 SCI-PHY EVMB with dual multi-PHY ATM daughter board.

3 REFERENCES

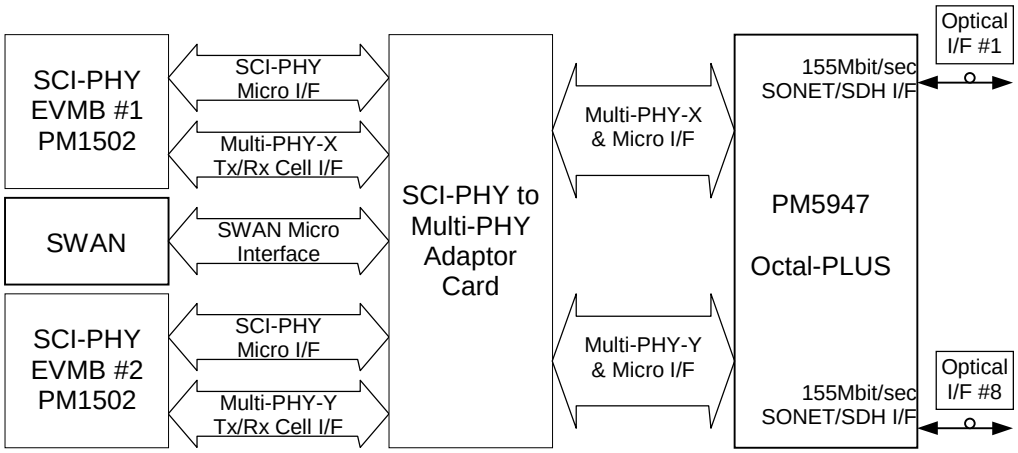
1. PMC-Sierra Inc., Octal S/UNI-PLUS with Automatic Protection Switching Optical Reference Design, Issue 2, February 1998

2. PMC-Sierra Inc., Saturn Compliant Interface for ATM Physical Layer Interconnect Evaluation Motherboard (SCI-PHY EVMB) Specification, Issue 3 June 1995

3. PMC-Sierra Inc., SWAN Timing and Micro Reference Design, Preliminary Issue 1, March 1997

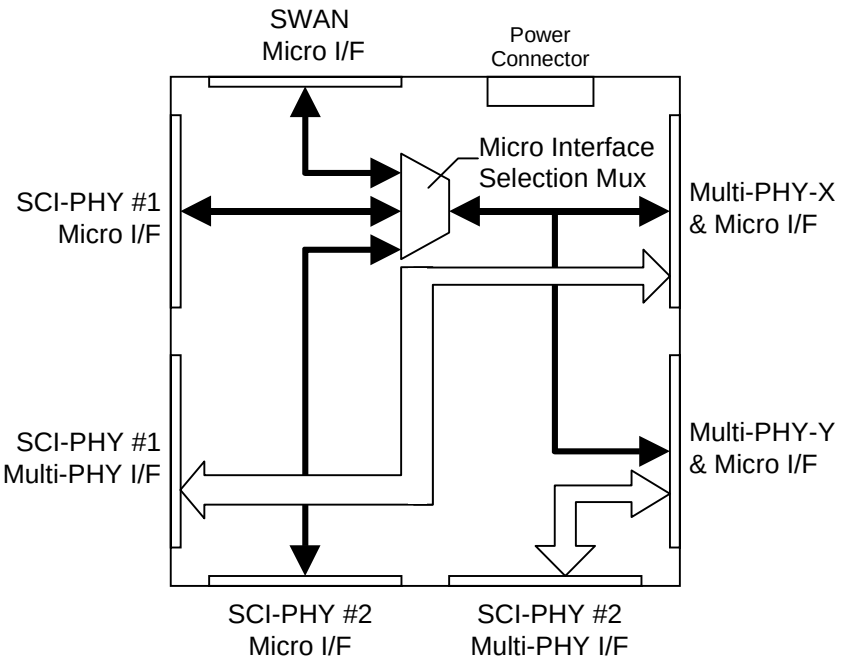
4 APPLICATION EXAMPLES

Figure 1 Multi-PHY adapter card connecting two SCI-PHY EVMBs and a SWAN board to Octal-PLUS Reference design.



The block diagram below is an example of how the SCI-PHY to Multi-PHY Adapter Card can be utilized to test the Octal PLUS reference design.

5 BLOCK DIAGRAM



6 DESCRIPTION

The Multi-PHY Adapter Card (MAC) facilitates the connection of two SCI-PHY EVMBs and a SWAN card to an ATM daughter card with two multi-PHY interfaces. Also, the MAC distributes power and microprocessor control to the SCI-PHY EVMBs, SWAN card and the multi-PHY interfaces.

The microprocessor access to the Multi-PHY-X and Multi-PHY-Y interfaces is multiplexed between the SWAN, SCI-PHY EVMB #1 or SCI-PHY EVMB #2 microprocessor. Selection between these microprocessor interfaces is made with jumpers.

The Multi-PHY-X Interface connects directly to the SCI-PHY #1 multi-PHY interface and the Multi-PHY-Y Interface connects directly to the SCI-PHY #2 multi-PHY interface

The Power Connection block allows connection to an external power supply and includes over-current protection. Therefore, power connections to the other MAC peripheral boards are not required.

7 CONNECTOR DESCRIPTIONS

The adapter board contains the following connectors:

Table 1 Multi-PHY Adapter Card Connectors

Connector	Description
SCI-PHY #1 Micro I/F	96 pin DIN female connector containing micro control signals from SCI-PHY #1 Micro Interface.
SCI-PHY #1 Multi-PHY I/F	96 pin DIN female connector containing multi-PHY signals from SCI-PHY #1 Multi-PHY Interface.
SCI-PHY #2 Micro I/F	96 pin DIN female connector containing micro control signals from SCI-PHY #2 Micro Interface.
SCI-PHY #2 Multi-PHY I/F	96 pin DIN female connector containing multi-PHY signals from SCI-PHY #2 Multi-PHY Interface.
SWAN Interface	96 pin DIN female connector containing micro control signals from SWAN Timing and Micro card.
Micro & Multi-PHY-X Interface	96 pin DIN male connector containing microprocessor address signals and multi-PHY signals to the Multi-PHY-X Interface.
Micro & Multi-PHY-Y Interface	96 pin DIN male connector containing microprocessor data and control signals and multi-PHY signals to the Multi-PHY-X Interface.

The SCI-PHY EVMB connectors are exactly the same and are described in the table below.

Table 2 SCI-PHY #1 and SCI-PHY #2 Micro Interface Connector

Pin Name	Type	Pin #	Function
CSB[0] CSB[1] CSB[2] CSB[3] CSB[4] CSB[5] CSB[6] CSB[7]	Input	A25 A26 A27 A28 A29 A30 A31 A32	Chip Select. CSB[7:0] asserts low to enable reading from and writing to the micro interface of the Multi-PHY interface. CSB[7:0] routes through the Micro Interface Selection mux.
GND	Power	B1- B25	Ground
VCC	Power	B26- B32	+5V Power
RSTB	Input	C2	Reset. RSTB is an active low hardware reset that routes through the Micro Interface Selection mux.
WRB	Input	C3	Write Strobe. WRB is an active low write strobe that routes through the Micro Interface Selection mux.
RDB	Input	C4	Read Enable. RDB is an active low read enable that routes through the Micro Interface Selection mux.
ALE	Input	C5	Address Latch Enable. ALE is an active high address latch enable that routes through the Micro Interface Selection mux.
INTB	Output	C6	Interrupt. INTB is an active low maskable hardware interrupt and routes through the Micro Interface Selection mux.

Pin Name	Type	Pin #	Function
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	C9 C10 C11 C12 C13 C14 C15 C16	Data Bus. D[7:0] is an eight bit microprocessor data bus that routes through the Micro Interface Selection mux.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]	Input	C17 C18 C19 C20 C21 C22 C23 C24	Address Bus. A[7:0] is an eight bit micro processor address bus that routes through the Micro Interface Selection mux.
	N/C	A1-A24, C1, C7, C8, C25-C32	Unconnected pins

The SCI-PHY EVMB #1 Multi-PHY interface is described in the table below. All signals connect directly to the Multi-PHY-X Interface.

Table 3 SCI-PHY #1 Multi-PHY Interface Connector

Pin Name	Type	Pin #	Function
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	Input	A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16	Transmit Data. TDAT[15:0] transfers data to the Multi-PHY-X Interface. TDAT[7:0] corresponds to the least significant byte of the data word and TDAT[15:8] corresponds to the most significant byte of the data word. TDAT[15:0] is synchronous to the rising edge of TFCLK. TDAT[15:0] routes to the Multi-PHY-X Interface.
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Output	A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 A31 A32	Receive Data. RDAT[15:0] transfers data from the Multi-PHY-X Interface. RDAT[7:0] corresponds to the least significant byte of the data word and RDAT[15:8] corresponds to the most significant byte of the data word. RDAT[15:0] is synchronous to the rising edge of RFCLK. RDAT[15:0] originates from the Multi-PHY-X Interface.

Pin Name	Type	Pin #	Function
GND	Power	B1-B23, C2, C16, C18	Ground
PWR +5V	Power	B29 - B32	+5V Power
TFCLK	Input	C1	Transmit FIFO Clock. TFCLK synchronizes TDAT[15:0] to the Multi-PHY Interface. The Multi-PHY Interface updates TCAn and samples TWRENnB, TSOC, TXPRTY[1:0], and TDAT[15:0] on the rising edge of TFCLK. TFCLK routes to the Multi-PHY-X Interface.
TSOC	Input	C3	Transmit Start Of Cell. TSOC marks the start of cell on the TDAT bus. TSOC asserts when the first word of the cell structure is present on the TDAT bus. TSOC is synchronous to the rising edge of TFCLK and routes to the Multi-PHY-X Interface.
TXPRTY[0] TXPRTY[1]	Input	C4 C5	Transmit Parity. TXPRTY[1:0] indicates the parity of the TDAT[15:0] bus. TXPRTY[1] is the parity calculation over the TDAT[15:8] bus. TXPRTY[0] is the parity calculation over the TDAT[7:0] bus. TXPRTY[1:0] is synchronous to the rising edge of TFCLK and routes to the Multi-PHY-X Interface.
TCA1 TCA2 TCA3 TCA4	Output	C6 C7 C8 C9	Transmit Cell Available. TCAn indicates when the nth channel of the Multi-PHY-X Interface can accept data. Four TCA inputs provide support for four channels. TCAn is synchronous to the rising edge of TFCLK and originates from the Multi-PHY-X Interface.

Pin Name	Type	Pin #	Function
TWREN1B TWREN2B TWREN3B TWREN4B	Input	C10 C11 C12 C13	Transmit Write Enable. The active low TWRENnB initiates writes to the nth channel transmit FIFO of the Multi-PHY-X Interface. Data on TDAT[15:0] is written into the nth channel transmit FIFO when the nth Multi-PHY-X Interface channel samples an asserted TWRENnB on the rising edge of TFCLK. No data is written into the transmit FIFO when the nth Multi-PHY-X Interface channel samples a negated TWRENnB on the rising edge of TFCLK. TWRENnB routes to the Multi-PHY-X Interface.
RFCLK	Input	C17	Receive FIFO Clock. RFCLK synchronizes RDAT[15:0] from the Multi-PHY Interface. The Multi-PHY Interface samples RWRENnB and updates RCAn, RSOC, RXPRTY[1:0], and RDAT[15:0] on the rising edge of RFCLK. RFCLK routes to the Multi-PHY-X Interface.
RSOC	Output	C19	Receive Start Of Cell. RSOC marks the start of cell on the RDAT bus. RSOC asserts when the first word of the cell structure is present on the RDAT bus. RSOC is synchronous to the rising edge of RFCLK and originates from the Multi-PHY-X Interface.
RXPRTY[0] RXPRTY[1]	Output	C20 C21	Receive Parity. RXPRTY[1:0] indicates the parity of the RDAT[15:0] bus. RXPRTY[1] is the parity calculation over the RDAT[15:8] bus. RXPRTY[0] is the parity calculation over the RDAT[7:0] bus. RXPRTY[1:0] is synchronous to the rising edge of RFCLK and originates from the Multi-PHY-X Interface.
RCA1 RCA2 RCA3 RCA4	Output	C22 C23 C24 C25	Receive Cell Available. RCAn indicates when the nth channel of the Multi-PHY-X Interface contains valid data. Four RCA inputs provide support for four channels. RCAn is synchronous to the rising edge of RFCLK and originates from the Multi-PHY-X Interface.

Pin Name	Type	Pin #	Function
RRDEN1B RRDEN2B RRDEN3B RRDEN4B	Input	C26 C27 C28 C29	Receive Read Enable. The active low RRDENnB initiates reads from the nth channel receive FIFO of the Multi-PHY-X Interface. Data is read from the nth Multi-PHY-X Interface channel receive FIFO and put on RDAT[15:0] when the nth Multi-PHY-X Interface channel samples an asserted RRDENnB on the rising edge of RFCLK. No data is read from the receive FIFO when the nth Multi-PHY-X Interface channel samples a negated RRDENnB on the rising edge of RFCLK. RRDENnB routes to the Multi-PHY-X Interface.
	N/C	B24-B28, C14, C15, C30-C32	Unconnected

The SCI-PHY EVMB #2 Multi-PHY interface is described in the table below. All signals connect directly to the Multi-PHY-Y Interface.

Table 4 SCI-PHY #2 Multi-PHY Interface

Pin Name	Type	Pin #	Function
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	Input	A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16	Transmit Data. TDAT[15:0] transfers data to the Multi-PHY-Y Interface. TDAT[7:0] corresponds to the least significant byte of the data word and TDAT[15:8] corresponds to the most significant byte of the data word. TDAT[15:0] is synchronous to the rising edge of TFCLK. TDAT[15:0] routes to the Multi-PHY-Y Interface.
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Output	A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 A31 A32	Receive Data. RDAT[15:0] transfers data from the Multi-PHY-Y Interface. RDAT[7:0] corresponds to the least significant byte of the data word and RDAT[15:8] corresponds to the most significant byte of the data word. RDAT[15:0] is synchronous to the rising edge of RFCLK. RDAT[15:0] originates from the Multi-PHY-Y Interface.
GND	Power	B1-B23, C2, C16, C18	Ground

Pin Name	Type	Pin #	Function
PWR +5V	Power	B29 - B32	+5V Power
TFCLK	Input	C1	Transmit FIFO Clock. TFCLK synchronizes TDAT[15:0] to the Multi-PHY Interface. The Multi-PHY Interface updates TCAn and samples TWRENnB, TSOC, TXPRTY[1:0], and TDAT[15:0] on the rising edge of TFCLK. TFCLK routes to the Multi-PHY-Y Interface.
TSOC	Input	C3	Transmit Start Of Cell. TSOC marks the start of cell on the TDAT bus. TSOC asserts when the first word of the cell structure is present on the TDAT bus. TSOC is synchronous to the rising edge of TFCLK and routes to the Multi-PHY-Y Interface.
TXPRTY[0] TXPRTY[1]	Input	C4 C5	Transmit Parity. TXPRTY[1:0] indicates the parity of the TDAT[15:0] bus. TXPRTY[1] is the parity calculation over the TDAT[15:8] bus. TXPRTY[0] is the parity calculation over the TDAT[7:0] bus. TXPRTY[1:0] is synchronous to the rising edge of TFCLK and routes to the Multi-PHY-Y Interface.
TCA1 TCA2 TCA3 TCA4	Output	C6 C7 C8 C9	Transmit Cell Available. TCAn indicates when the nth channel of the Multi-PHY-Y Interface can accept data. Four TCA inputs provide support for four channels. TCAn is synchronous to the rising edge of TFCLK and originates from the Multi-PHY-Y Interface.

Pin Name	Type	Pin #	Function
TWREN1B TWREN2B TWREN3B TWREN4B	Input	C10 C11 C12 C13	Transmit Write Enable. The active low TWRENnB initiates writes to the nth channel transmit FIFO of the Multi-PHY-Y Interface. Data on TDAT[15:0] is written into the nth channel transmit FIFO when the nth Multi-PHY-Y Interface channel samples an asserted TWRENnB on the rising edge of TFCLK. No data is written into the transmit FIFO when the nth Multi-PHY-Y Interface channel samples a negated TWRENnB on the rising edge of TFCLK. TWRENnB routes to the Multi-PHY-Y Interface.
RFCLK	Input	C17	Receive FIFO Clock. RFCLK synchronizes RDAT[15:0] from the Multi-PHY Interface. The Multi-PHY Interface samples RWRENnB and updates RCAn, RSOC, RXPRTY[1:0], and RDAT[15:0] on the rising edge of RFCLK. RFCLK routes to the Multi-PHY-Y Interface.
RSOC	Output	C19	Receive Start Of Cell. RSOC marks the start of cell on the RDAT bus. RSOC asserts when the first word of the cell structure is present on the RDAT bus. RSOC is synchronous to the rising edge of RFCLK and originates from the Multi-PHY-Y Interface.
RXPRTY[0] RXPRTY[1]	Output	C20 C21	Receive Parity. RXPRTY[1:0] indicates the parity of the RDAT[15:0] bus. RXPRTY[1] is the parity calculation over the RDAT[15:8] bus. RXPRTY[0] is the parity calculation over the RDAT[7:0] bus. RXPRTY[1:0] is synchronous to the rising edge of RFCLK and originates from the Multi-PHY-Y Interface.
RCA1 RCA2 RCA3 RCA4	Output	C22 C23 C24 C25	Receive Cell Available. RCAn indicates when the nth channel of the Multi-PHY-Y Interface contains valid data. Four RCA inputs provide support for four channels. RCAn is synchronous to the rising edge of RFCLK and originates from the Multi-PHY-Y Interface.

Pin Name	Type	Pin #	Function
RRDEN1B RRDEN2B RRDEN3B RRDEN4B	Input	C26 C27 C28 C29	Receive Read Enable. The active low RRDENnB initiates reads from the nth channel receive FIFO of the Multi-PHY-Y Interface. Data is read from the nth Multi-PHY-Y Interface channel receive FIFO and put on RDAT[15:0] when the nth Multi-PHY-Y Interface channel samples an asserted RRDENnB on the rising edge of RFCLK. No data is read from the receive FIFO when the nth Multi-PHY-Y Interface channel samples a negated RRDENnB on the rising edge of RFCLK. RRDENnB routes to the Multi-PHY-Y Interface.
	N/C	B24-B28, C14, C15, C30-C32	Unconnected

Table 5 SWAN Connector

Pin Name	Type	Pin #	Function
TXFP+ TXFP-	Output	A1 A2	Transmit Frame Pulse. TXFP+/- is a differential signal pair used for system synchronization feedback. TXFP+/- is synchronous to SRCLK+/- and originates from the Multi-PHY-X Interface connector.
RALM	Output	A4	Receive Alarm. RALM indicates a Multi-PHY Interface channel has a loss of signal condition. RALM asserts high and originates from the Multi-PHY-X Interface connector.
RXFP+ RXFP-	Output	A6 A7	Receive Frame Pulse. RXFP+/- is a differential signal pair used for system synchronization feedback. RXFP+/- is synchronous to SRCLK+/- and originates from the Multi-PHY-Y Interface connector.

Pin Name	Type	Pin #	Function
SRCLK+ SRCLK-	Input	A14 A15	System Reference Clock. SRCLK+/- is a differential system reference clock for the PHY channels of the Multi-PHY Interface. SRCLK+/- routes directly to the Multi-PHY-Y Interface connector.
CSB[0] CSB[1] CSB[2] CSB[3] CSB[4] CSB[5] CSB[6] CSB[7]	Input	A25 A26 A27 A28 A29 A30 A31 A32	Chip Select. CSB[7:0] asserts low to enable reading from and writing to the micro interface of the Multi-PHY interface. CSB[7:0] routes through the Micro Interface Selection mux.
GND	Power	B1- B25	Ground
VCC	Power	B26- B32	+5V Power
RSTB	Input	C2	Reset. RSTB is an active low hardware reset that routes through the Micro Interface Selection mux.
WRB	Input	C3	Write Strobe. WRB is an active low write strobe that routes through the Micro Interface Selection mux.
RDB	Input	C4	Read Enable. RDB is an active low read enable that routes through the Micro Interface Selection mux.
INTB	Output	C6	Interrupt. INTB is an active low maskable hardware interrupt and routes through the Micro Interface Selection mux.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	C9 C10 C11 C12 C13 C14 C15 C16	Data Bus. D[7:0] is an eight bit microprocessor data bus that routes through the Micro Interface Selection mux.

Pin Name	Type	Pin #	Function
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]	Input	C17 C18 C19 C20 C21 C22 C23 C24	Address Bus. A[7:0] is an eight bit micro processor address bus that routes through the Micro Interface Selection mux.
	N/C	A3, A5, A8-A13, A16-A24, C1, C5, C7, C8, C25-C32	Unconnected pins

Table 6 Multi-PHY-X Interface

Pin Name	Type	Pin #	Function
XTFCLK	Output	A1	Multi-PHY-X FIFO Clock. XTFCLK synchronizes data transfer transactions to the Multi-PHY-X Interface. Clock rates up to 52 MHz are supported. The Multi-PHY-X Interface samples XTWRENB[3:0], XTSOC, XTXPRTY[1:0], XTDAT[15:0] and XRRDENB[3:0] on the rising edge of XTFCLK. XTFCLK originates from the SCI-PHY EVMB #1 Interface connector.

XTSOC	Output	A3	Multi-PHY-X Transmit Start Of Cell. XTSOC marks the start of cell on the XTDAT bus. XTSOC asserts high on the rising edge of XTFCLK when the first word of the data structure is present on the XTDAT bus. XTSOC originates from the SCI-PHY EVMB #1 Interface connector.
XTXPRTY[0] XTXPRTY[1]	Output	C1 C3	Multi-PHY-X Transmit Parity. XTXPRTY[1:0] indicates the parity of the XTDAT[15:0] bus. The Multi-PHY-X Interface samples XTXPRTY[1:0] on the rising edge of XTFCLK. XTXPRTY[1] is the parity calculation over the XTDAT[15:8] bus. XTXPRTY[0] is the parity calculation over the XTDAT[7:0] bus. XTXPRTY[1:0] originates from the SCI-PHY EVMB #1 Interface connector.
XTDAT[0] XTDAT[1] XTDAT[2] XTDAT[3] XTDAT[4] XTDAT[5] XTDAT[6] XTDAT[7] XTDAT[8] XTDAT[9] XTDAT[10] XTDAT[11] XTDAT[12] XTDAT[13] XTDAT[14] XTDAT[15]	Output	A11 A10 A9 A8 A7 A6 A5 A4 C11 C10 C9 C8 C7 C6 C5 C4	Multi-PHY-X Transmit Data. XTDAT[15:0] transfers data to the corresponding Multi-PHY-X Interface channel on the rising edge of XTFCLK when one of XTWRENB[3:0] is asserted. XTDAT[7:0] corresponds to the least significant byte of the data word while XTDAT[15:8] corresponds to the most significant byte of the data word. XTDAT[15:0] originates from the SCI-PHY EVMB #1 Interface connector.
XTCA[0] XTCA[1] XTCA[2] XTCA[3]	Input	B5 B4 B2 B1	Multi-PHY-X Transmit Cell Available. XTCA[n] indicates when the nth channel of the Multi-PHY-X Interface can accept data. Four XTCA inputs are provided to support four channels and the Multi-PHY-X Interface updates XTCAn on the rising edge of XTFCLK. XTCA[3:0] routes to the SCI-PHY EVMB #1 Interface connector.

XTWRENB[0] XTWRENB[1] XTWRENB[2] XTWRENB[3]	Output	B11 B10 B8 B7	Multi-PHY-X Transmit Write Enable. The active low XTWRENB[n] initiates writes to the nth channel transmit FIFO of the Multi-PHY-X Interface. Data on XTDAT[15:0] is written into the nth channel transmit FIFO when the nth Multi-PHY-X Interface channel samples an asserted XTWRENB[n] on the rising edge of XTFCLK. No data is written into the transmit FIFO when the nth Multi-PHY-X Interface channel samples a negated XTWRENB[n] on the rising edge of XFCLK. XTWRENB[3:0] originates from the SCI-PHY EVMB #1 Interface connector.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]	Output	A13 A14 A15 A16 A17 A18 A19 A20	Address Bus. A[7:0] is an eight bit micro processor address bus that originates from the Micro Interface Selection mux.
CSB[0] CSB[1] CSB[2] CSB[3] CSB[4] CSB[5] CSB[6] CSB[7]	Output	C13 C14 C15 C16 C17 C18 C19 C20	Chip Select. CSB[7:0] asserts low to enable reading from and writing to the micro interface of the Multi-PHY interface. CSB[7:0] originates from the Micro Interface Selection mux.
TXFP+ (TXFP[1]) TXFP- (TXFP[0])	Input	B15 B16	Transmit Frame Pulse. The differential transmit frame pulse inputs provide the SWAN Micro and Timing card an 8KHz feedback signal for external clock synchronization. TXFP+/- routes directly to the SWAN Micro Interface connector.
RALM	Input	B18	Receive Alarm. Receive Alarm indicates a loss of signal (LOS) condition has occurred at the PHY channel selected to provide the TXFP+/- signals. RALM routes directly to the SWAN Micro Interface connector.

XRFCLK	Output	A32	Multi-PHY-X Receive FIFO Clock. XRFCLK synchronizes data transfer transactions to the Multi-PHY-X Receive Interface. Clock rates up to 52 MHz are supported. The Multi-PHY-X Interface updates XRCA[3:0], XRSOC, XRXPRTY[1:0], XRDAT[15:0] and XTCA[3:0] on the rising edge of XRFCLK.
XRSOC	Input	A30	Multi-PHY-X Receive Start Of Cell. XRSOC marks the start of cell on the XRDAT bus. XRSOC asserts high on the rising edge of XRFCLK when the first word of the data structure is present on the XRDAT bus. XRSOC routes to the SCI-PHY EVMB #1 Interface connector.
XRXPRTY[0] XRXPRTY[1]	Input	C32 C30	Multi-PHY-X Receive Parity. XRXPRTY[1:0] indicates the parity of the XRDAT[15:0] bus. XRXPRTY[1] is the parity calculation over the XRDAT[15:8] bus. XRXPRTY[0] is the parity calculation over the XRDAT[7:0] bus. XRXPRTY[1:0] routes to the SCI-PHY EVMB #1 Interface connector.
XRDAT[0] XRDAT[1] XRDAT[2] XRDAT[3] XRDAT[4] XRDAT[5] XRDAT[6] XRDAT[7] XRDAT[8] XRDAT[9] XRDAT[10] XRDAT[11] XRDAT[12] XRDAT[13] XRDAT[14] XRDAT[15]	Input	A29 A28 A27 A26 A25 A24 A23 A22 C29 C28 C27 C26 C25 C24 C23 C22	Multi-PHY-X Receive Data. XRDAT[15:0] transfers data from the Multi-PHY-X Interface channel on the rising edge of XRFCLK when one of XRRDENB[3:0] is asserted. XRDAT[7:0] corresponds to the least significant byte of the data word while XRDAT[15:8] corresponds to the most significant byte of the data word. XRDAT[15:0] routes to the SCI-PHY EVMB #1 Interface connector.

XRCA[0] XRCA[1] XRCA[2] XRCA[3]	Input	B32 B31 B29 B28	Multi-PHY-X Receive Cell Available. XRCA[n] indicates when the nth channel of the Multi-PHY-X Interface contains valid data. Four XRCA inputs are provided to support four Multi-PHY-X channels. The nth Multi-PHY-X Interface channel asserts XRCA[n] when data can be read from its receive FIFO. The nth Multi-PHY-X Interface channel negates XRCA[n] when its receive FIFO is empty. XRCA[3:0] routes to the SCI-PHY EVMB #1 Interface connector.
XRRDENB[0] XRRDENB[1] XRRDENB[2] XRRDENB[3]	Output	B26 B25 B23 B22	Multi-PHY-X Receive Write Enable. The active low XRRDENB[n] initiates reads from the nth channel receive FIFO of the Multi-PHY-X Interface. Data is read from the nth Multi-PHY-X Interface channel receive FIFO and put on XRDAT[15:0] when the nth Multi-PHY-X Interface channel samples an asserted XRRDENB[n] on the rising edge of XRFCLK. No data is read from the nth Multi-PHY-X Interface channel receive FIFO when the nth Multi-PHY-X Interface channel samples a negated XRRDENB[n] on the rising edge of XRFCLK. XRRDENB[3:0] originates from the SCI-PHY EVMB #1 Interface connector.
GND	Power	B3 B6 B9 B12 B13 B14 B17 B19 B21 B24 B27 B30	Ground

PWR +5V	Power	A2 A12 A21 A31 C2 C12 C21 C31	+5V Power

Table 7 Multi-PHY-Y Interface Connector

Pin Name	Type	Pin #	Function
YTFCLK	Output	A1	Multi-PHY-Y FIFO Clock. YTFCLK synchronizes data transfer transactions to the Multi-PHY-Y Interface. Clock rates up to 52 MHz are supported. The Multi-PHY-Y Interface samples YTWRENB[3:0], YTSOC, YTXPRTY[1:0] YTDAT[15:0] and YRRDENB[3:0] on the rising edge of YTFCLK. YTFCLK originates from the SCI-PHY EVMB #2 Interface connector.
YTSOC	Output	A3	Multi-PHY-Y Transmit Start Of Cell. YTSOC marks the start of cell on the YTDAT bus. YTSOC asserts high on the rising edge of YTFCLK when the first word of the data structure is present on the YTDAT bus. YTSOC originates from the SCI-PHY EVMB #2 Interface connector.
YTXPRTY[0] YTXPRTY[1]	Output	C3 C1	Multi-PHY-Y Transmit Parity. YTXPRTY[1:0] indicates the parity of the YTDAT[15:0] bus. The Multi-PHY-Y Interface samples YTXPRTY[1:0] on the rising edge of YTFCLK. YTXPRTY[1] is the parity calculation over the YTDAT[15:8] bus. YTXPRTY[0] is the parity calculation over the YTDAT[7:0] bus. YTXPRTY[1:0] originates from the SCI-PHY EVMB #2 Interface connector.

YTDAT[0] YTDAT[1] YTDAT[2] YTDAT[3] YTDAT[4] YTDAT[5] YTDAT[6] YTDAT[7] YTDAT[8] YTDAT[9] YTDAT[10] YTDAT[11] YTDAT[12] YTDAT[13] YTDAT[14] YTDAT[15]	Output	A11 A10 A9 A8 A7 A6 A5 A4 C11 C10 C9 C8 C7 C6 C5 C4	Multi-PHY-Y Transmit Data. YTDAT[15:0] transfers data to the corresponding Multi-PHY-Y Interface channel on the rising edge of YTFCLK when one of YTWRENB[3:0] is asserted. YTDAT[7:0] corresponds to the least significant byte of the data word while YTDAT[15:8] corresponds to the most significant byte of the data word. YTDAT[15:0] originates from the SCI-PHY EVMB #2 Interface connector.
YTCA[0] YTCA[1] YTCA[2] YTCA[3]	Input	B5 B4 B2 B1	Multi-PHY-Y Transmit Cell Available. YTCA[n] indicates when the nth channel of the Multi-PHY-Y Interface can accept data. Four YTCA inputs are provided to support four channels and the Multi-PHY-Y Interface updates YTCAn on the rising edge of YTFCLK. YTCA[3:0] routes to the SCI-PHY EVMB #2 Interface connector.
YTWRENB[0] YTWRENB[1] YTWRENB[2] YTWRENB[3]	Output	B11 B10 B8 B7	Multi-PHY-Y Transmit Write Enable. The active low YTWRENB[n] initiates writes to the nth channel transmit FIFO of the Multi-PHY-Y Interface. Data on YTDAT[15:0] is written into the nth channel transmit FIFO when the nth Multi-PHY-Y Interface channel samples an asserted YTWRENB[n] on the rising edge of YTFCLK. No data is written into the transmit FIFO when the nth Multi-PHY-Y Interface channel samples a negated YTWRENB[n] on the rising edge of YTFCLK. YTWRENB[3:0] originates from the SCI-PHY EVMB #2 Interface connector.

D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	Output	A13 A14 A15 A16 A17 A18 A19 A20	Data Bus. D[7:0] is an eight bit microprocessor data bus that routes through the Micro Interface Selection mux.
RSTB	Output	C13	Reset. RSTB is an active low hardware reset that routes through the Micro Interface Selection mux.
INTB	Input	C14	Interrupt. INTB is an active low maskable hardware interrupt and routes through the Micro Interface Selection mux.
ALE	Output	C15	Address Latch Enable. ALE is an active high address latch enable that routes through the Micro Interface Selection mux.
BSB	Output	C16	Board Select. BSB is an active low board select that enables microprocessor access to the Multi-PHY Interface. BSB originates from the Micro Interface Selection mux.
RDB	Output	C18	Read Enable. RDB is an active low read enable that routes through the Micro Interface Selection mux.
WRB	Output	C20	Write Strobe. WRB is an active low write strobe that routes through the Micro Interface Selection mux.
SRCLK+ (SRCLK[1]) SRCLK- (SRCLK[0])	Output	B14 B15	System Reference Clock. SRCLK+/- is a jitter free 19.44MHz differential system reference clock for the PHY channels of the Multi-PHY Interface. SRCLK+/- originates from the SWAN Micro Interface connector.
RXFP+ RXFP-	Input	B18 B19	Receive Frame Pulse. RXFP+/- is a differential signal pair used for system synchronization feedback. RXFP+/- is synchronous to SRCLK+/- and connects directly to the SWAN Micro Interface.

YRFCLK	Output	A32	Multi-PHY-Y Receive FIFO Clock. YRFCLK synchronizes data transfer transactions to the Multi-PHY-Y Interface. Clock rates up to 52 MHz are supported. The Multi-PHY-Y Interface updates YRCA[3:0], YRSOC, YRXPRTY[1:0], YRDAT[15:0] and YTCA[3:0] on the rising edge of YRFCLK. YRFCLK originates from the SCI-PHY EVMB #2 Interface connector.
YRSOC	Input	A30	Multi-PHY-Y Receive Start Of Cell. YRSOC marks the start of cell on the YRDAT bus. YRSOC asserts high on the rising edge of YRFCLK when the first word of the data structure is present on the YRDAT bus. YRSOC routes to the SCI-PHY EVMB #2 Interface connector.
YRXPRTY[0] YRXPRTY[1]	Input	C32 C30	Multi-PHY-Y Receive Parity. YRXPRTY[1:0] indicates the parity of the YRDAT[15:0] bus. YRXPRTY[1] is the parity calculation over the YRDAT[15:8] bus. YRXPRTY[0] is the parity calculation over the YRDAT[7:0] bus. YRXPRTY[1:0] routes to the SCI-PHY EVMB #2 Interface connector.
YRDAT[0] YRDAT[1] YRDAT[2] YRDAT[3] YRDAT[4] YRDAT[5] YRDAT[6] YRDAT[7] YRDAT[8] YRDAT[9] YRDAT[10] YRDAT[11] YRDAT[12] YRDAT[13] YRDAT[14] YRDAT[15]	Input	A29 A28 A27 A26 A25 A24 A23 A22 C29 C28 C27 C26 C25 C24 C23 C22	Multi-PHY-Y Receive Data. YRDAT[15:0] transfers data from the Multi-PHY-Y Interface channel on the rising edge of YRFCLK when one of YRRDENB[3:0] is asserted. YRDAT[7:0] corresponds to the least significant byte of the data word while YRDAT[15:8] corresponds to the most significant byte of the data word. YRDAT[15:0] routes to the SCI-PHY EVMB #2 Interface connector.

YRCA[0] YRCA[1] YRCA[2] YRCA[3]	Input	B32 B31 B29 B28	Multi-PHY-Y Receive Cell Available. YRCA[n] indicates when the nth channel of the Multi-PHY-Y Interface contains valid data. Four YRCA inputs are provided to support four Multi-PHY-Y channels. The nth Multi-PHY-Y Interface channel asserts YRCA[n] when data can be read from its receive FIFO. The nth Multi-PHY-Y Interface channel negates YRCA[n] when its receive FIFO is empty. YRCA[3:0] routes to the SCI-PHY EVMB #2 Interface connector.
YRRDENB[0] YRRDENB[1] YRRDENB[2] YRRDENB[3]	Output	B26 B25 B23 B22	Multi-PHY-Y Receive Write Enable. The active low YRRDENB[n] initiates reads from the nth channel receive FIFO of the Multi-PHY-Y Interface. Data is read from the nth Multi-PHY-Y Interface channel receive FIFO and put on YRDAT[15:0] when the nth Multi-PHY-Y Interface channel samples an asserted YRRDENB[n] on the rising edge of YRFCLK. No data is read from the nth Multi-PHY-Y Interface channel receive FIFO when the nth Multi-PHY-Y Interface channel samples a negated YRRDENB[n] on the rising edge of YFCLK. YRRDENB[3:0] originates from the SCI-PHY EVMB #2 Interface connector.
GND	Power	B3 B6 B9 B13 B16 B17 B20 B21 B24 B27 B30	Ground

PWR +5V	Power	A2 A12 A21 A31 C2 C12 C21 C31	+5V Power

8 IMPLEMENTATION

8.1 Root Drawing, Sheet 1

Function:

1. Provides an overview of the major functional blocks of the SCI-PHY to Multi-PHY Adapter board circuitry.
2. Illustrates the interconnecting data paths.
3. Shows power connection and protection.

Implementation

This sheet interconnects the SCIPHY_X, SCIPHY_Y, SWAN, MICRO_MUX, MULTIPHY_X and MULTIPHY_Y blocks. It also shows the power connections and related power circuitry.

+5V and GND power connections to the board are made via a screw-down type terminal block J3. The +5V routes through four identical networks that consist of a 5A fuse current protection, power indication LED with current limiting resistor, current feedback prevention diode, zener diode over-voltage protection and filtering capacitor.

8.2 SCIPHY_X, Sheet 2

Function:

1. Provides the electrical interface to the SCI-PHY #1 Evaluation Motherboard microprocessor interface and the SCI-PHY ATM cell interface.

Implementation:

This sheet shows two DIN-96 edge connectors. P1 provides the complete microprocessor interface which includes control signals, 8-bit data bus, 8-bit address bus and eight chip select signals. P2 provides the complete multi-PHY interface for the Multi-PHY-X Interface. This interface includes 16-bit data buses, parity, start-of-cell, cell available and read/write enable signals for the receive and transmit directions respectively. Power and ground connections are made in both connectors. Place the decoupling capacitors near to the connector for filtering VCC.

8.3 SCIPHY_Y, Sheet 3

Function:

1. Provides the electrical interface to the SCI-PHY #2 Evaluation Motherboard microprocessor interface and the SCI-PHY ATM cell interface.

Implementation:

This sheet shows two DIN-96 edge connectors. P4 provides the complete microprocessor interface which includes control signals, 8-bit data bus, 8-bit address bus and eight chip select signals. P5 provides the complete multi-PHY interface for the Multi-PHY-Y Interface. This interface includes 16-bit data buses, parity, start-of-cell, cell available and read/write enable signals for the receive and transmit directions respectively. Power and ground connections are made in both connectors. Place the decoupling capacitors near to the connector for filtering VCC.

8.4 SWAN, Sheet 4

Function:

1. Provides the electrical interface to the SWAN Microprocessor and Reference Timing Card.

Implementation:

This sheet shows one DIN-96 edge connector that provides a portion of the electrical connections to the SCI-PHY to Multi-PHY Adapter board. Connector P3 has the complete microprocessor interface which includes control signals, 8-bit data bus, 8-bit address bus and eight chip select signals. P3, also has the Transmit Frame Pulse (TXFP+/-), Receive Frame Pulse (RXFP+/-) and System Reference Clock (SRCLK+/) signals for the system reference clock card. Also, power and ground connections are made in connector P3. Place the decoupling capacitors near to the connector for filtering VCC.

8.5 MICRO_MUX, Sheet 5

Function:

1. Provides manual selection of the Multi-PHY Interface microprocessor control between either the SWAN microprocessor or the SCI-PHY EVMB #1 microprocessor.
2. Incorporates 3 sources of reset for the Multi-PHY Interface.
3. Provides logic for the board select signal (BSB).

Implementation:

This sheet shows the multiplexing between the SCI-PHY #1, SCI-PHY #2 or the SWAN microprocessor signals U1, U2, U3 and U4 multiplex the microprocessor signals to the Multi-PHY Interface. Jumpers J1 and J2 correctly select which multiplex path is active. When the jumper is in place (closed), the SWAN microprocessor path is selected. When the jumper is removed (open), the SCI-PHY microprocessor path is selected.

Figure 2 Micro Interface Selection Jumper Positions

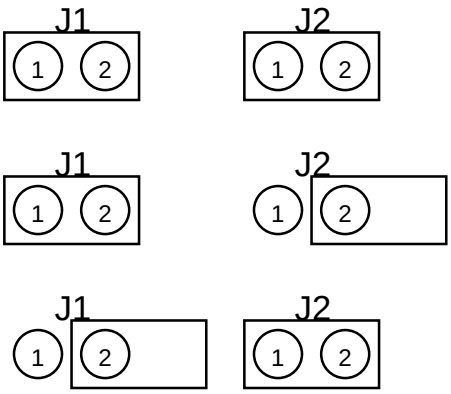


Table 8 Micro Interface Selection Jumper Positions

J1	J2	Description
Pin 1-2 Closed	Pin 1-2 Closed	Selects the SCI-PHY #1 Micro Interface to control the Multi-PHY Interface microprocessor.
Pin 1-2 Closed	Pin 1-2 Open	Selects the SCI-PHY #2 Micro Interface to control the Multi-PHY Interface microprocessor.
Pin 1-2 Open	Pin 1-2 Closed	Selects the SWAN Micro Interface to control the Multi-PHY Interface microprocessor.

An external hardware reset, an external software reset and a local hardware reset are the three sources for the Multi-PHY reset. The SCI-PHY #1, SCI-PHY #2 and the SWAN microprocessors provide the external reset signals dependent on the micro multiplexer selection. The normally open push button switch and capacitor C28 provide the local hardware reset. The two AND gates of U6 provide a logical OR function of these signals since they are active low.

4-input AND gates of U7 and the 2-input AND gate of U6 combine to assert BSB low when any of the CSB signals are asserted low.

The inputs of the unused gates of U6 are connected to ground (logic 0). Capacitors for decoupling power pins are also provided.

8.6 MULTIPHY _X, Sheet 6

Function:

1. Provides the electrical interface for the address bus of a microprocessor to Octal PLUS board.
2. Provides the electrical interface for the Multi-PHY-X Interface of the Octal PLUS board.
3. Provides the external system reference clock feedback signal interface (TXFP+/-).
4. Provides VCC and GND connections to the Octal PLUS board.

Implementation:

This sheet shows one DIN-96 edge connector that provides a portion of the electrical connections to the Octal PLUS board. Connector P6 has the complete Multi-PHY-X and the 16 bit microprocessor address bus. Connector P6, also has the Transmit Frame Pulse (TXFP+/-) feedback signals for an external system reference clock card. Place the decoupling capacitors near to the connector for filtering the incoming VCC.

8.7 MULTIPHY_Y, Sheet 7

Function:

1. Provides the electrical interface for the data bus and control signals of a microprocessor to Octal PLUS board.
2. Provides the electrical interface for the Multi-PHY Multi-PHY-Ys to the Octal PLUS board.
3. Provides the external system reference clock feedback signal interface (RXFP+/-), alarm signal interface (RALM) and the reference clock signal (SRCLK+/-).
4. Provides VCC and GND connections to the Octal PLUS board.

Implementation:

This sheet shows one DIN-96 edge connector that provides a portion of the electrical connections to the Octal PLUS board. Connector P7 has the complete Multi-PHY-Y, the 8 bit microprocessor data bus and the microprocessor control signals. Connector P7, also, has the differential System Reference Clock signals (SRCLK+/-), the differential feedback signals (RXFP+/-), and the single ended

alarm signal interface (RALM). Place the de coupling capacitors near to the connector to provide clean power to the Octal PLUS board.

9 SCHEMATICS

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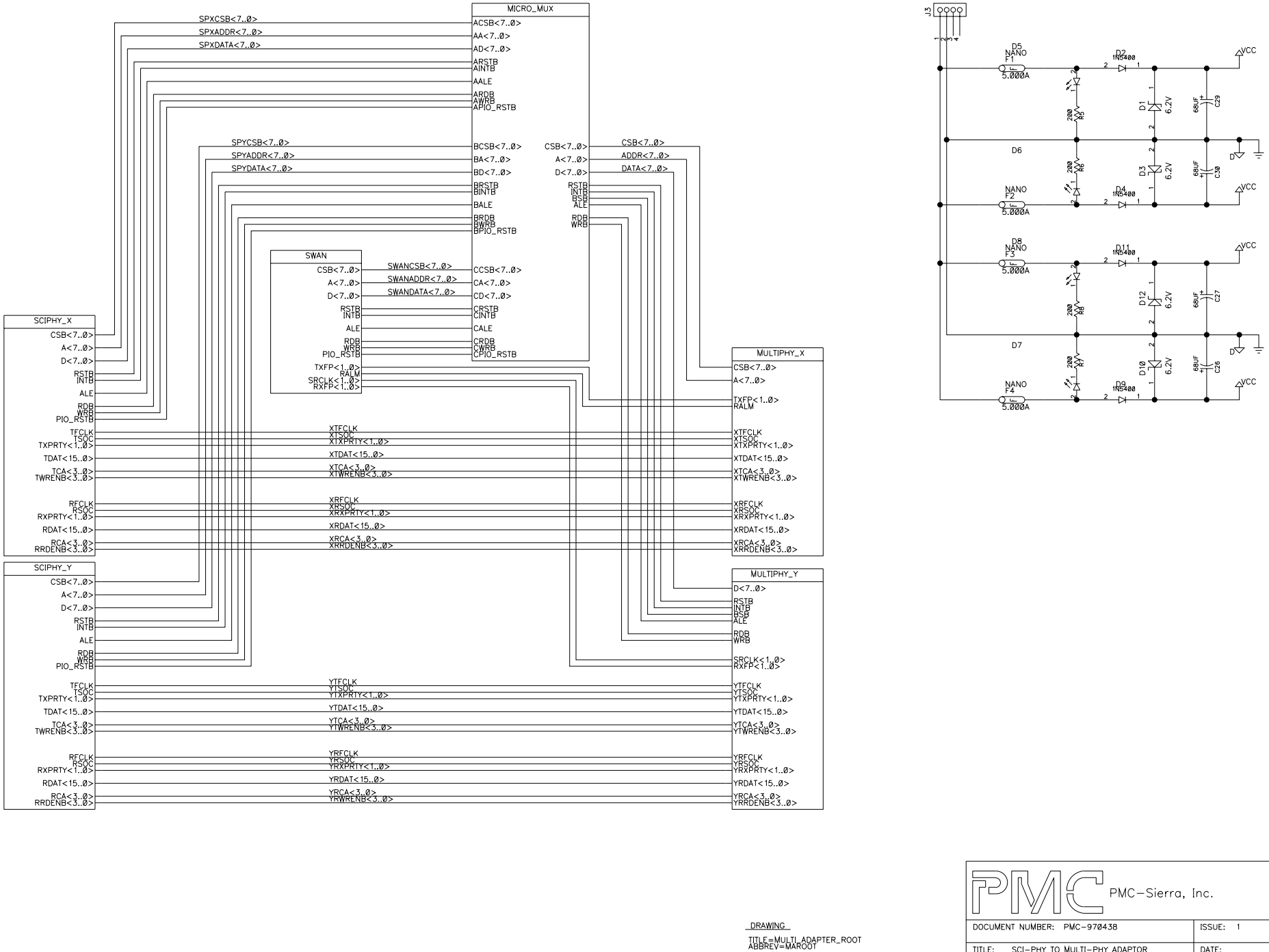

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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970438	ISSUE: 1
TITLE: SCI-PHY TO MULTI-PHY ADAPTOR ROOT DRAWING	DATE: FEB. 27 1998
ENGINEER: A.B. HOWES	PAGE: 1 OF 7

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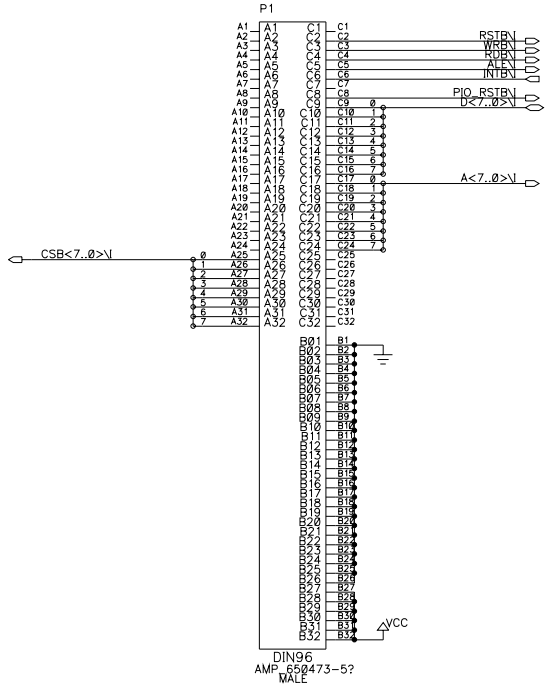

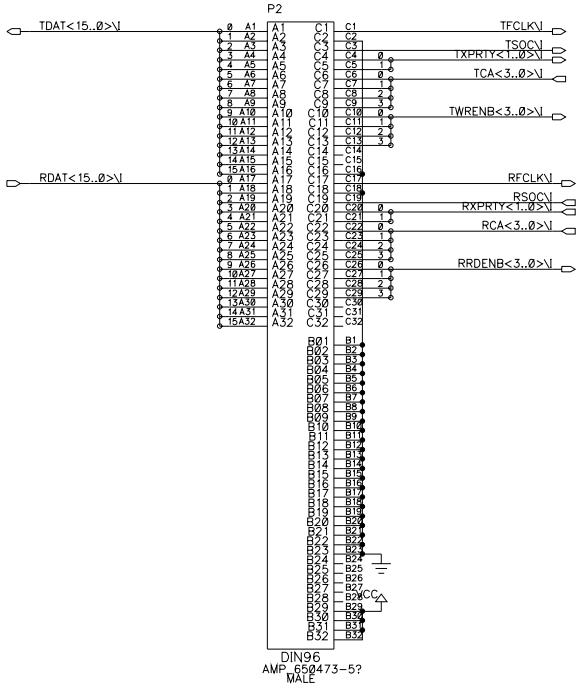

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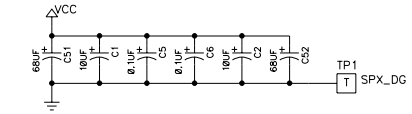

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TITLE: SCI-PHY TO MULTI-PHY ADAPTOR SCIPHY_X	DATE: FEB. 27 1998
ENGINEER: A.B. HOWES	PAGE: 2 OF 7

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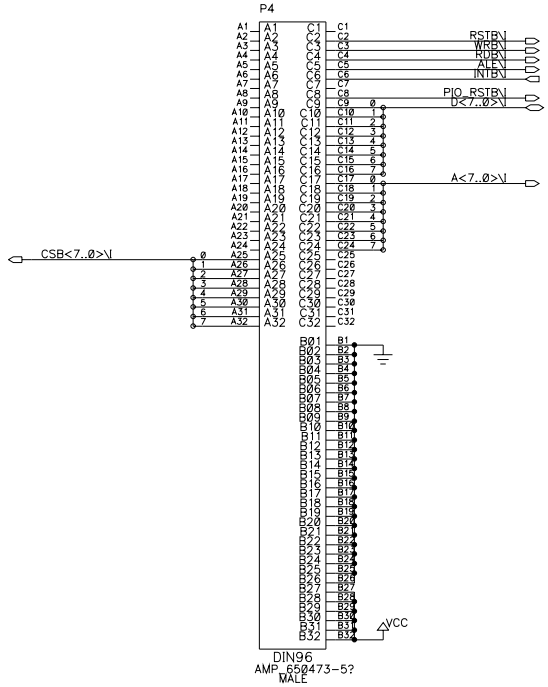

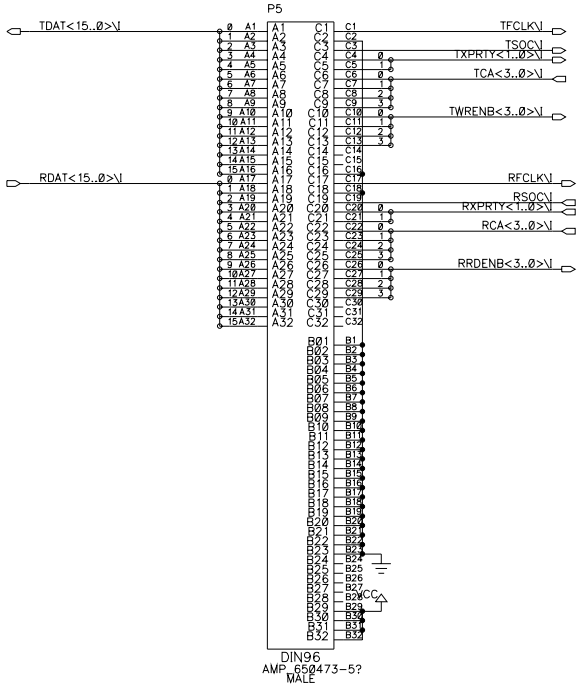

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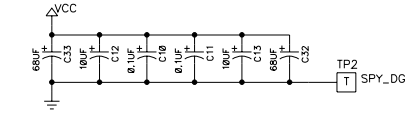

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ENGINEER: A.B. HOWES	PAGE: 3 OF 7

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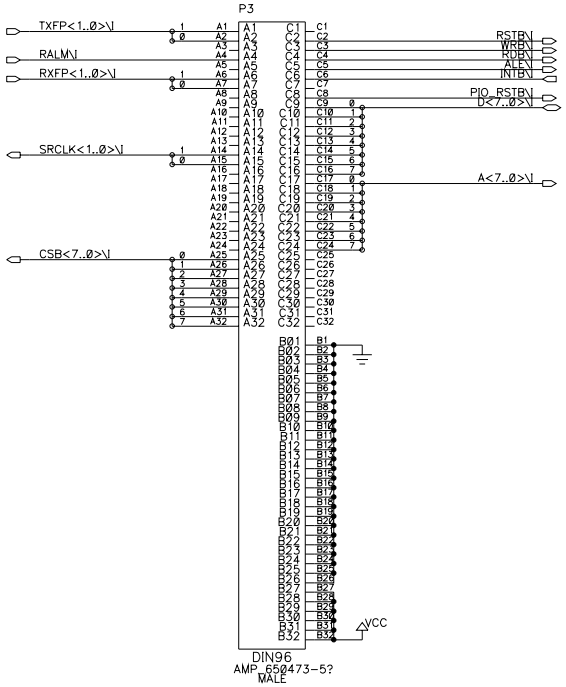

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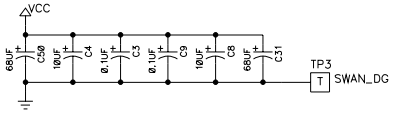

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ENGINEER: A.B. HOWES	PAGE: 4 OF 7

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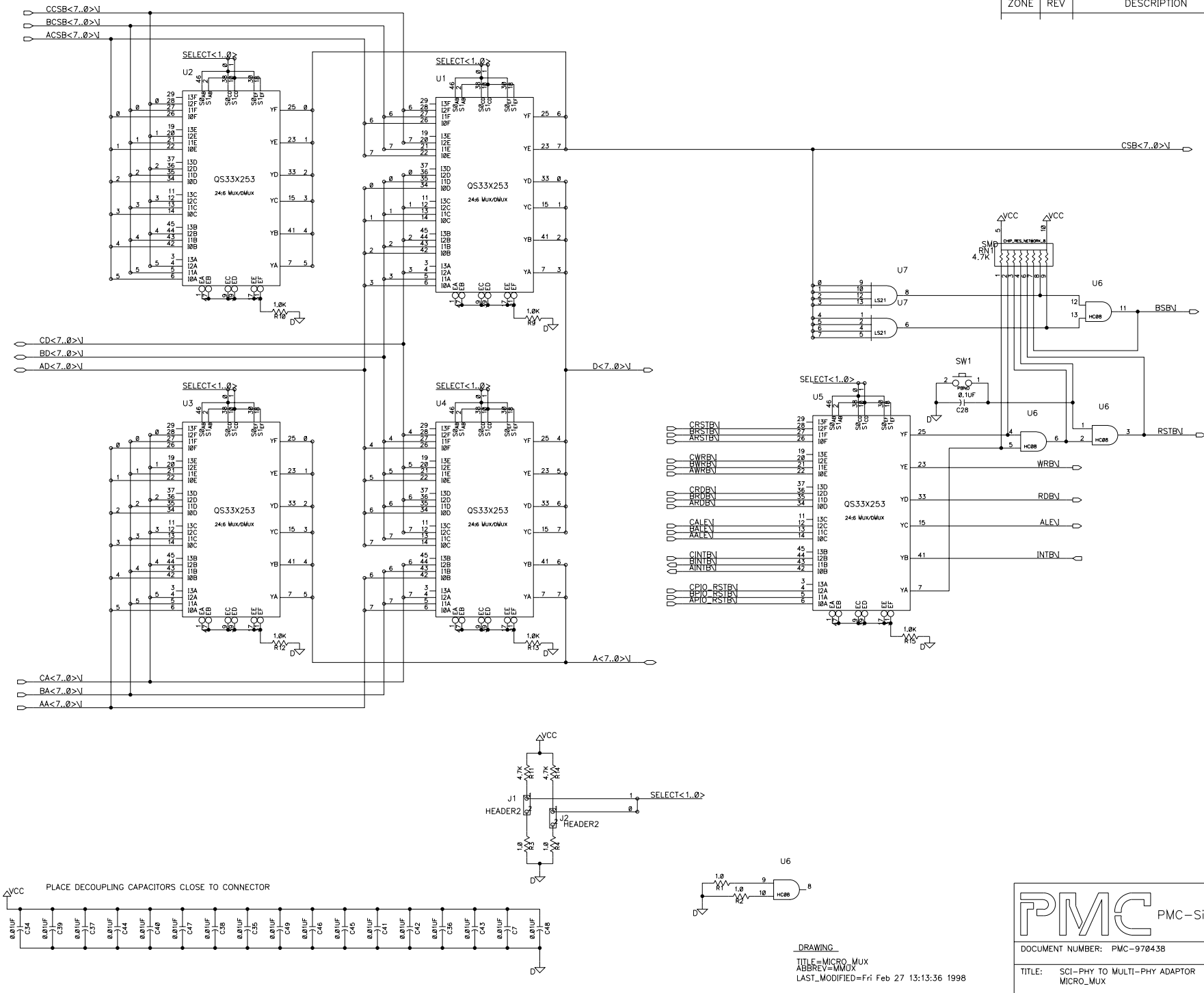

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ENGINEER: A.B. HOWES	PAGE: 5 OF 7

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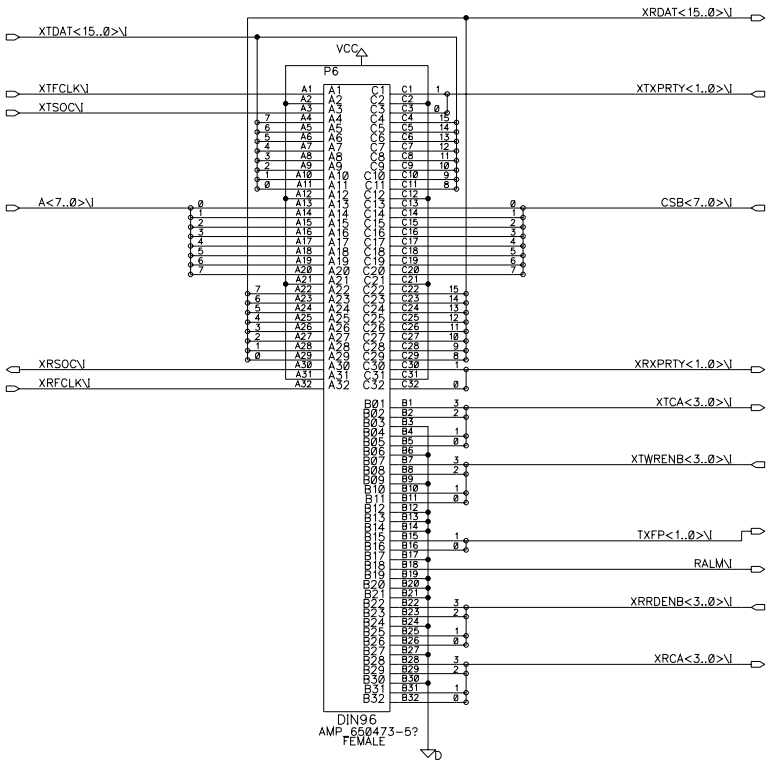

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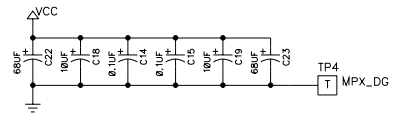

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TITLE: SCI-PHY TO MULTI-PHY ADAPTOR MULTIPHY_X	DATE: FEB. 27 1998
ENGINEER: A.B. HOWES	PAGE: 6 OF 7

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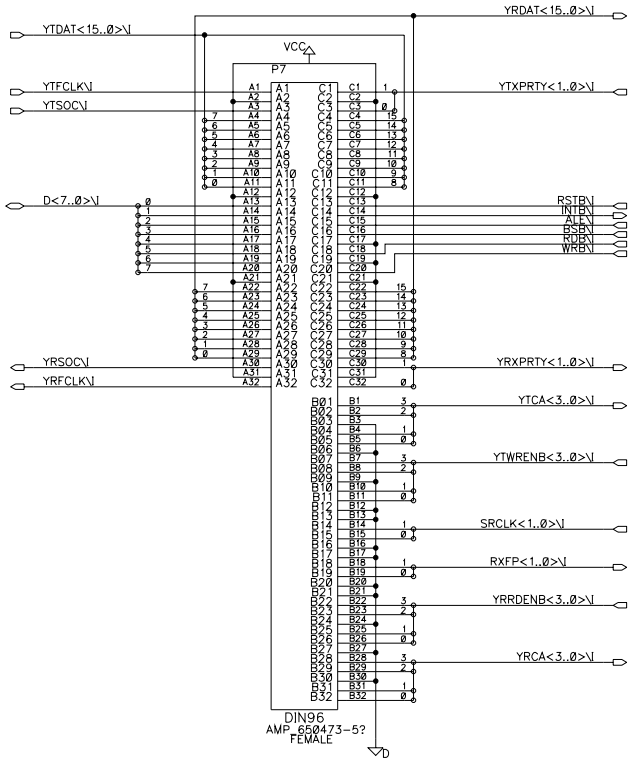

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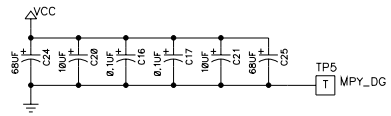

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TITLE: SCI-PHY TO MULTI-PHY ADAPTOR MULTIPHY_Y	DATE: FEB. 27 1998
ENGINEER: A.B. HOWES	PAGE: 7 OF 7

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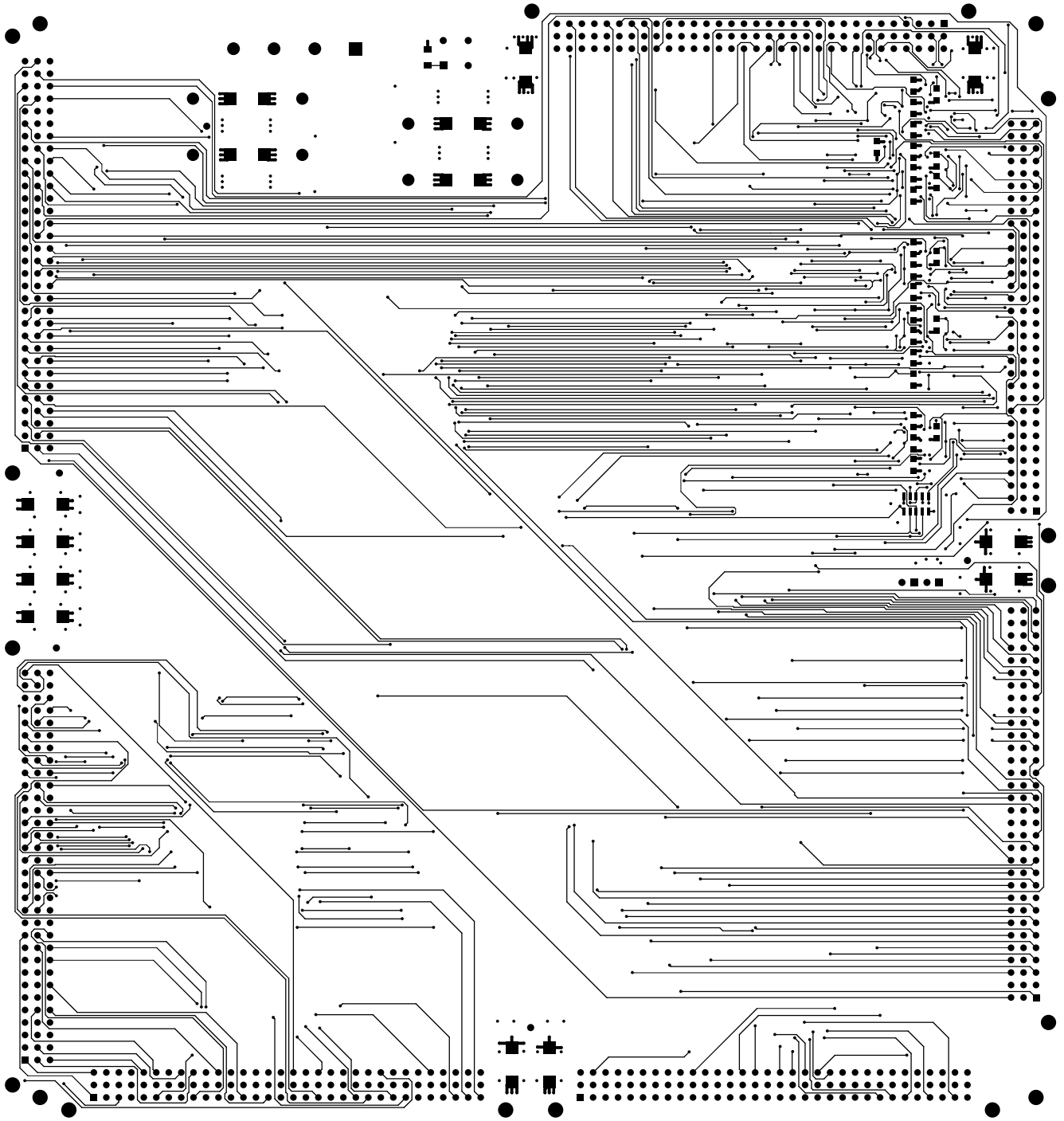
10 MATERIAL LIST

Table 9 Bill of Material

Item	Reference	Qty	Description
1	D2, D4, D9, D11	4	1N5400 Rectifier Diode, 3A
2	U6	1	Quad 2-input AND 74HC08
3	U7	1	Dual 4-input AND 74LS21
4	C7, C34-C49	17	0.01UF Capacitor, 50V, X7R-805
5	C3, C5, C6, C9-C11, C14-C17, C28	11	0.1UF Capacitor , 50V, X7R-1206
6	C1, C2, C4, C8, C12, C13, C18-C21	10	10UF Capacitor, 10V, SMD Tantalum TEH
7	C22-C27, C29-C33, C50-C52	14	68UF Capacitor, 6.3V, SMD Tantalum TEH
8	RN1	1	4.7K Resistor Network SMD SOIC16
9	P6, P7	2	96pin Right Angle DIN Connector Socket (female), AMP 650462-5
10	P1-P5	5	96pin Right Angle DIN Connector Plug (Male), AMP 650473-5
11	D1, D3, D10, D12	4	6.2V Zener Diode 1W SMD
12	F1-F4	4	5A Nano Fuse SMD
13	J1, J2	2	Headers, 0.025" square pins, 0.1" spacing
14	D5-D8	4	LED, Super Red SMD
15	SW1	1	Normally Open Push Button Switch
16	J3	1	Screw down Terminal Block

Item	Reference	Qty	Description
17	U1-U5	5	24:6 Mux/Demux High Speed CMOS QuickSwitch QS33X253, QVSOP48
18	R1-R4	4	1.0 Resistor, 5%, 805
19	R9, R10, R12, R13, R15	5	1.0K Resistor, 5%, 805
20	R5-R8	4	200 Resistor, 5%, 805
21	R11, R14	2	4.7K Resistor, 5%, 805
22	TP1-TP5	5	Headers, 0.025" square pins, 0.1" spacing

11 LAYOUT

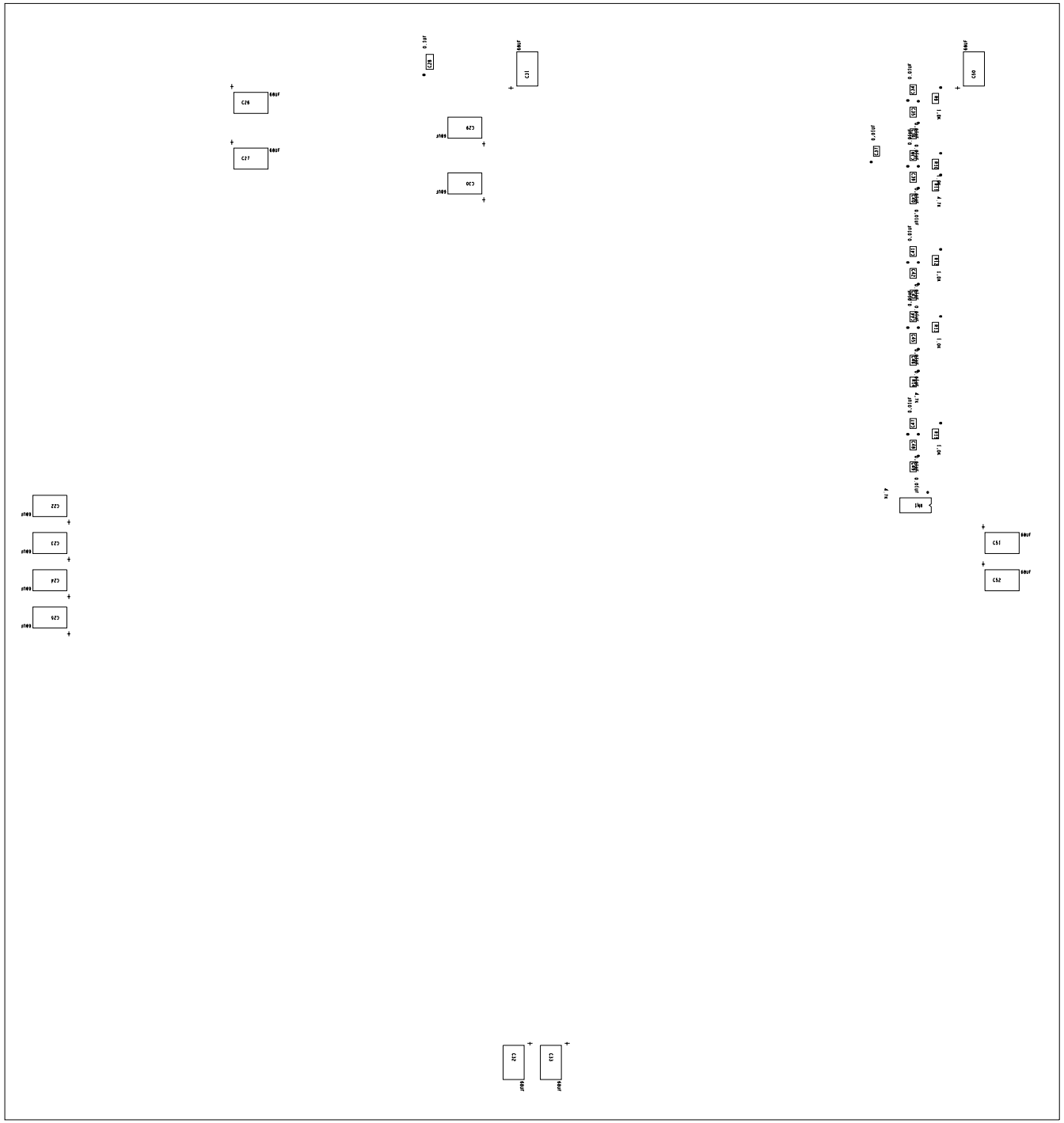


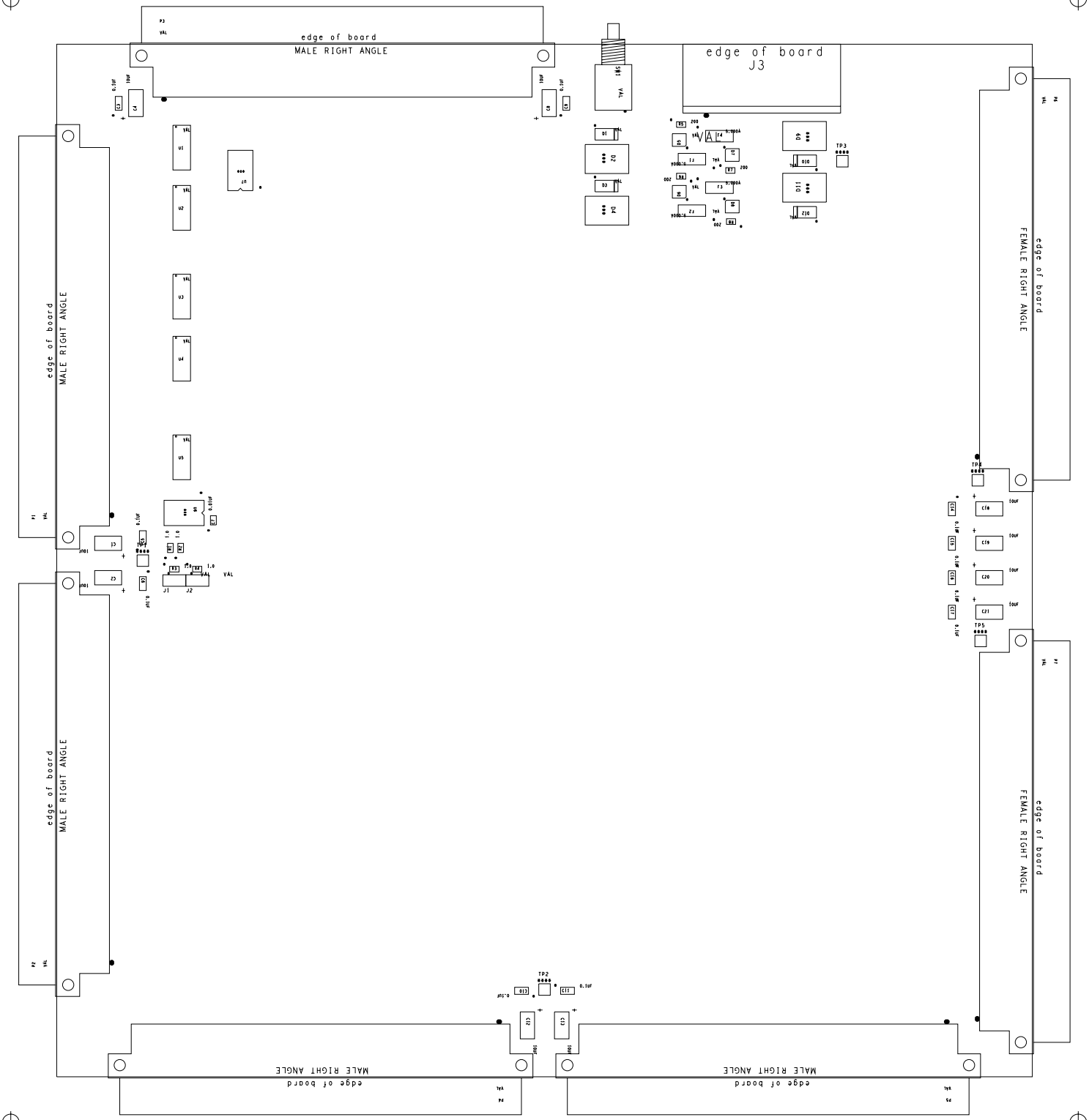
VCC PLANE BOTTOM LAYER

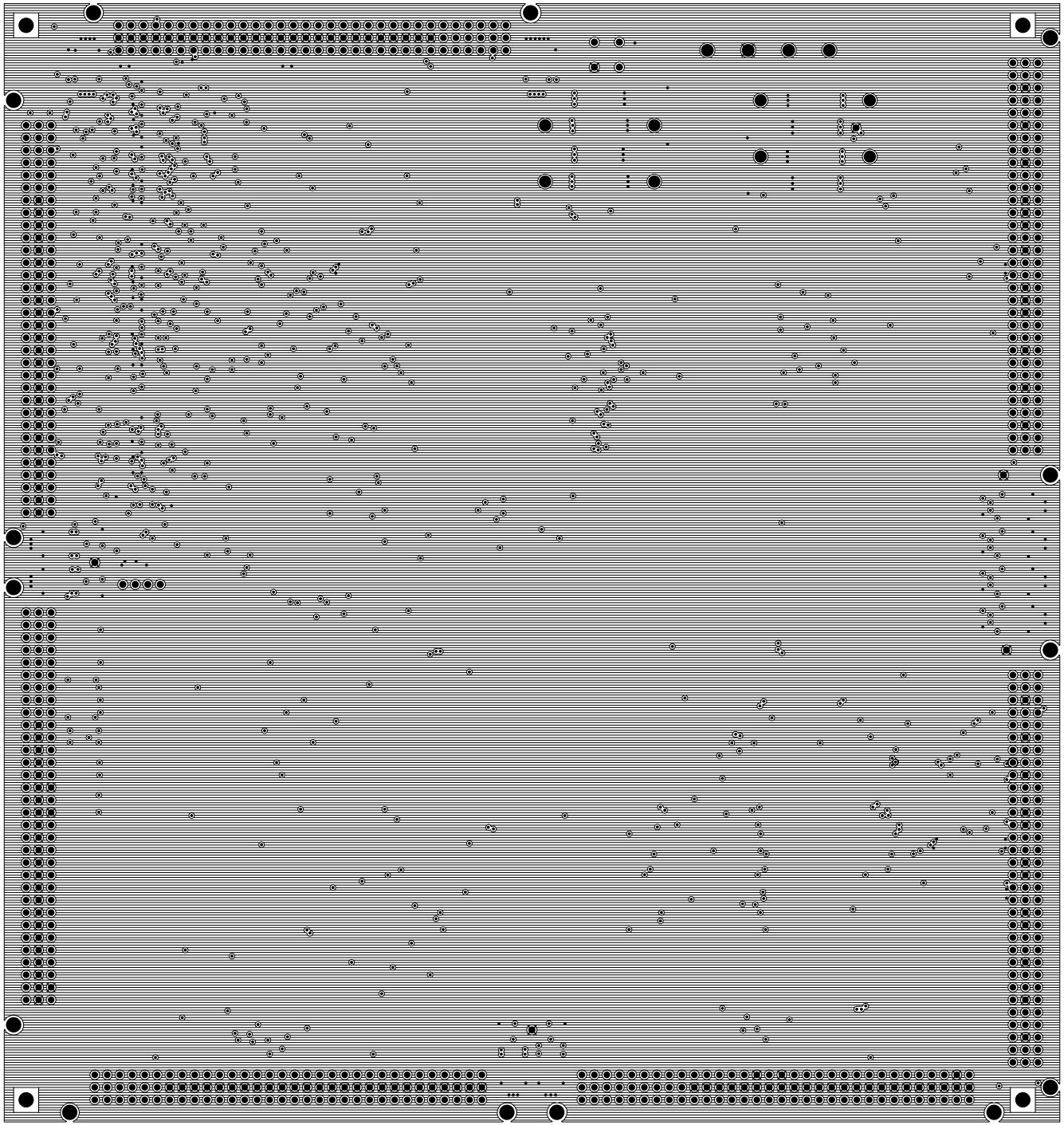
COMP TOP BOTTOM COMP

PMC-SIERRA MULTI PHY INTERFACE REV.2.0 1997

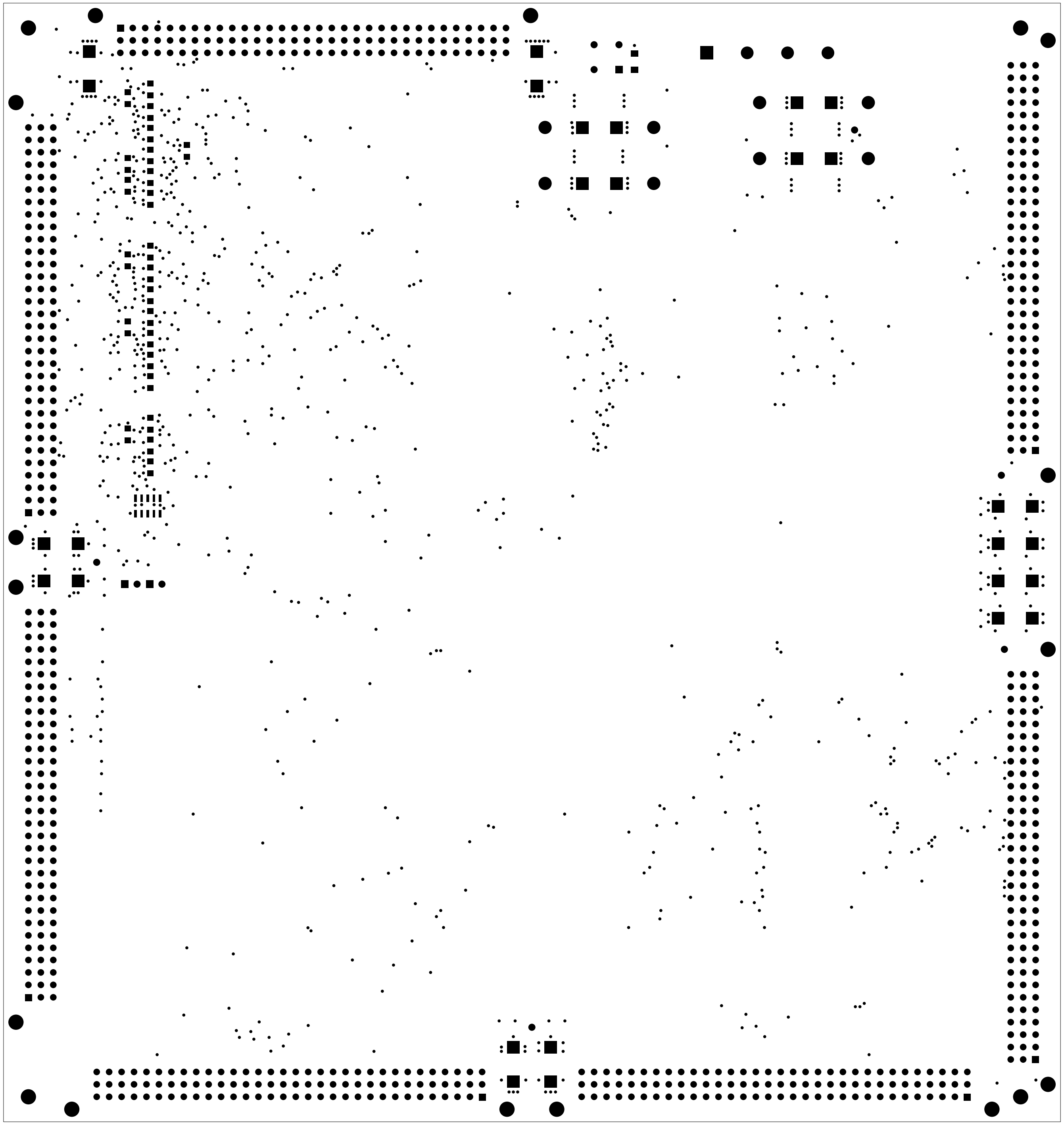
PMC-SIERRA MULTI PHY INTERFACE REV.2.0 1997



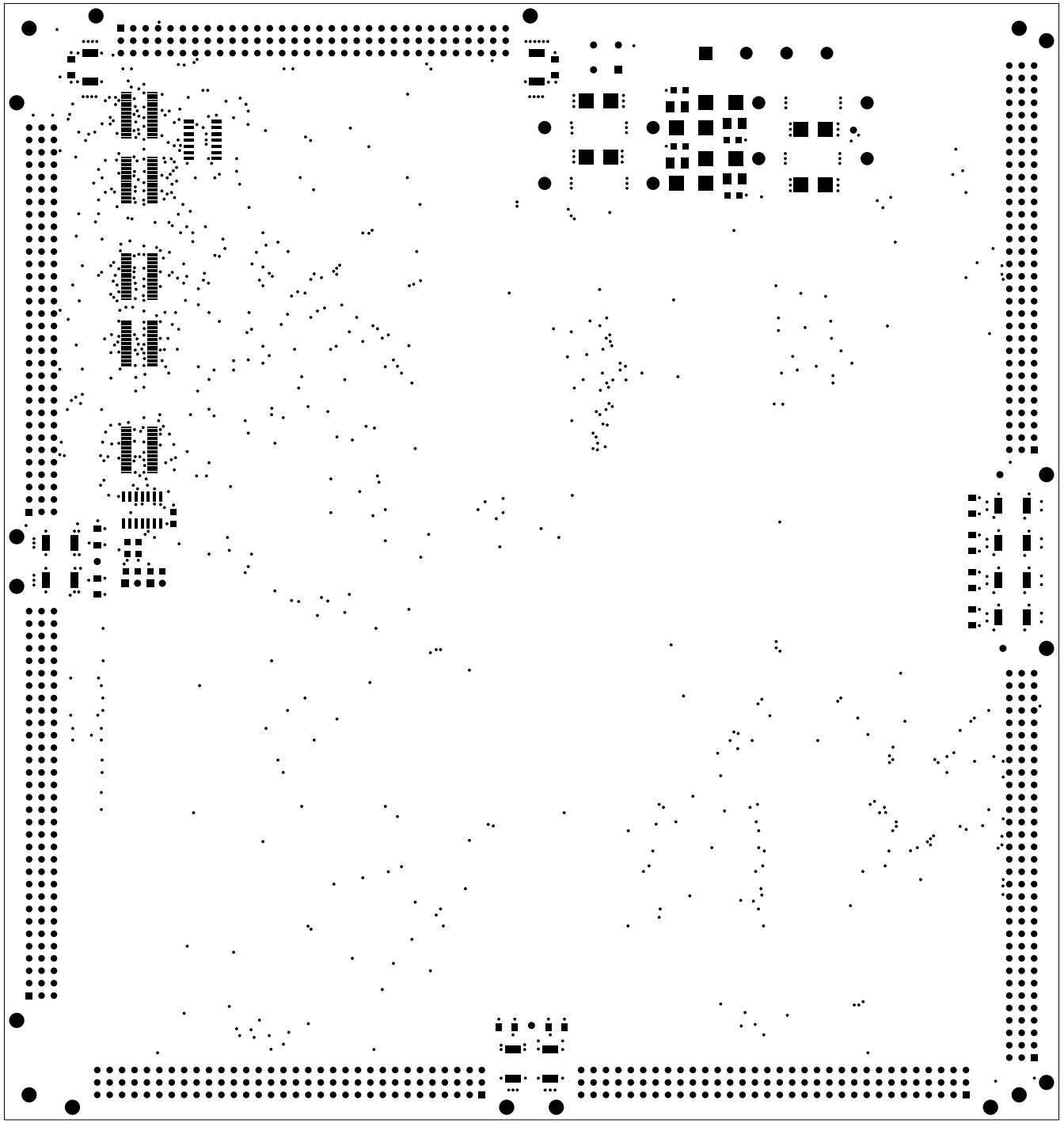

edge of board
MALE RIGHT ANGLE
edge of board
J3
edge of board
MALE RIGHT ANGLE
edge of board
MALE RIGHT ANGLE
edge of board
FEMALE RIGHT ANGLE
edge of board
FEMALE RIGHT ANGLE
MALE RIGHT ANGLE
edge of board
MALE RIGHT ANGLE
edge of board
TP1
TP2
TP3
TP5



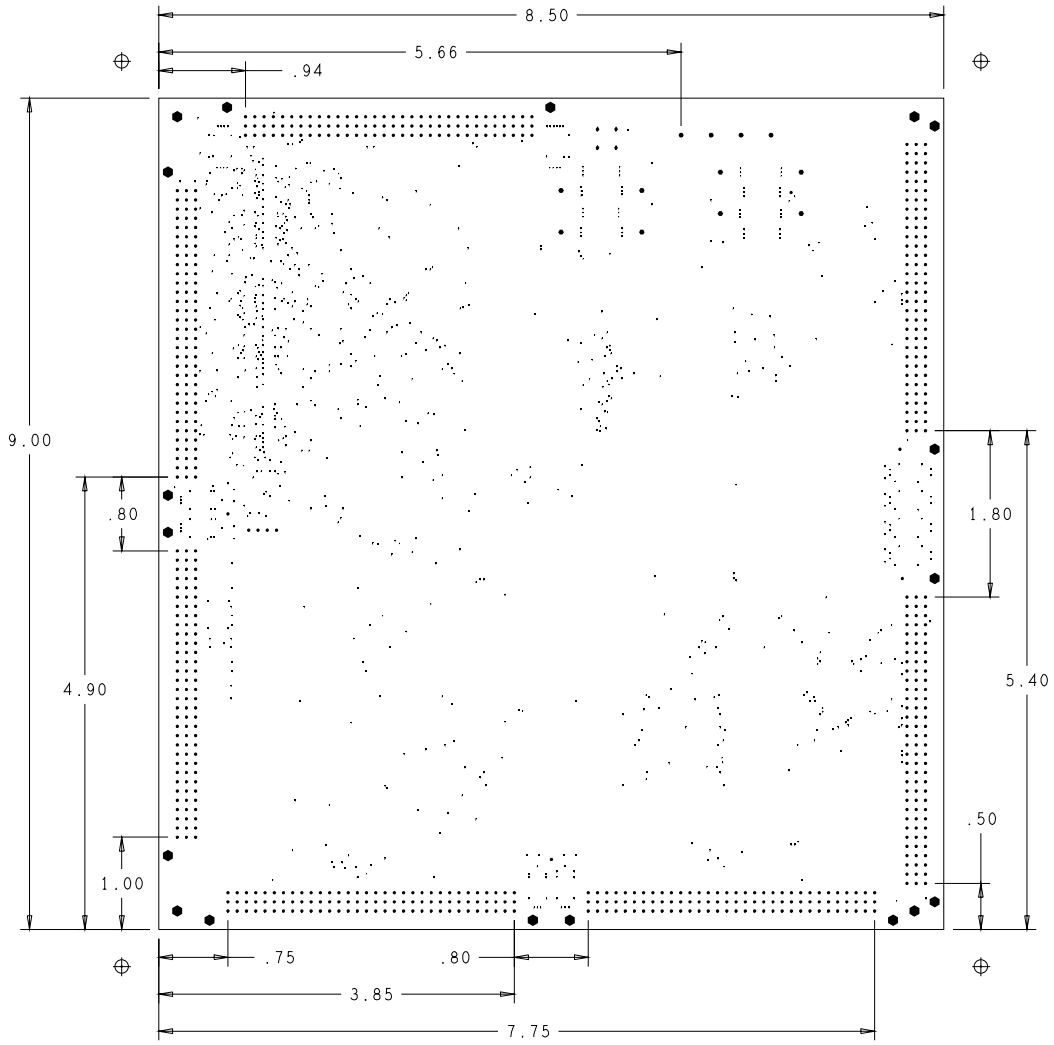
SOLDERMASK BOTTOM



PMC-SIERRA MULTI PHY INTERFACE REV.2.0 1997



REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED



	Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
#	COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
	FR-4	DIELECTRIC	-------	-------	10.0 mil	4.2
	COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	37.68 mil	4.2
	COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	10.0 mil	4.2
#	COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------

Note: 75 ohm controlled impedance traces with trace width of 8 mil are on Top and Bottom layers.

Notes:

1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers.
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are spedified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

DRILL CHART			
FIGURE	SIZE	PLATED	QTY
·	13.0	PLATED	915
•	36.0	PLATED	681
•	42.0	PLATED	4
•	55.0	PLATED	4
•	60.0	PLATED	8
⬢	125.0	NOT PLATED	18

ARTWORK FILM
TOP LAYER
GROUND PLANE
VCC PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
SOLDER PASTE TOP
SOLDER PASTE BOTTOM
MECH DRAWING

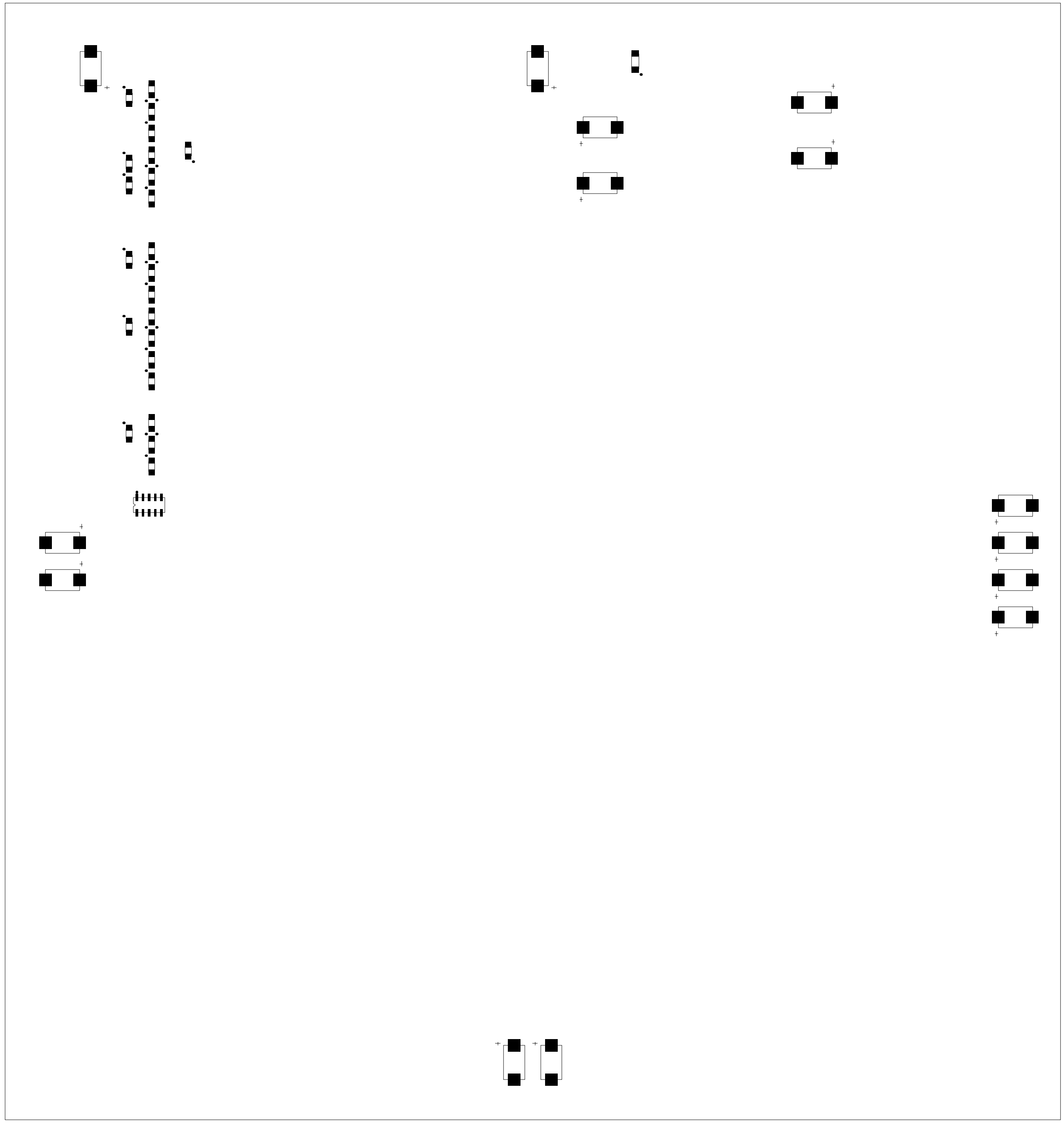
PMC-SIERRA SCI PHY MULTI PHY INTERFACE CARD REV.2.0 1997

UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN			
TOLERANCES ON;				
2 PL DECIMALS ·	CHECKED			
3 PL DECIMALS ·	ENGRG			
ANGLES ·	ISSUED			
FRACTIONS ·				

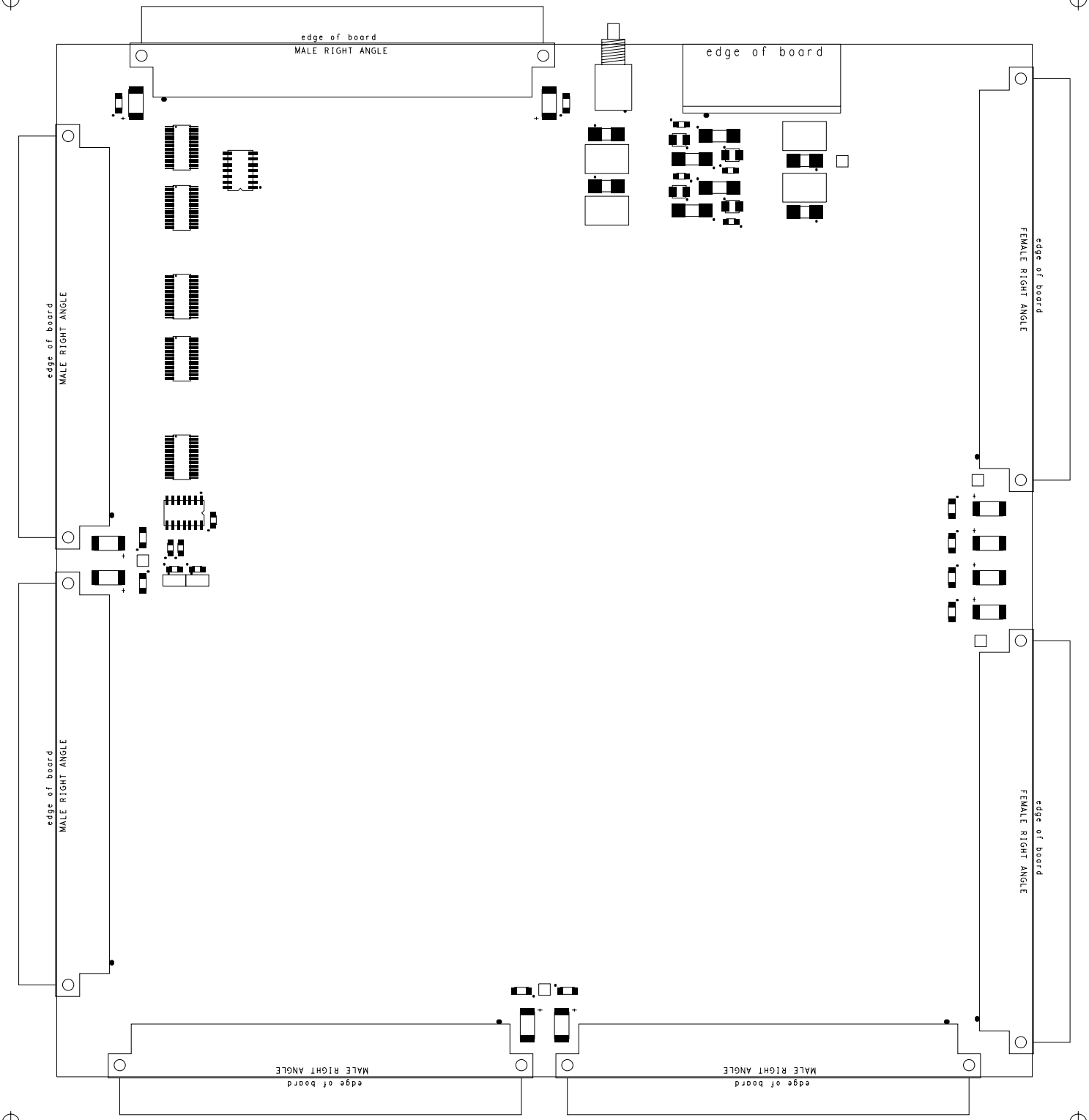
PMC-Sierra, Inc.
105-8555 Baxter Place, Burnaby B.C.
Canada, V5A 4V7
Tel: 604 415 6000 Fax: 604 415 6200

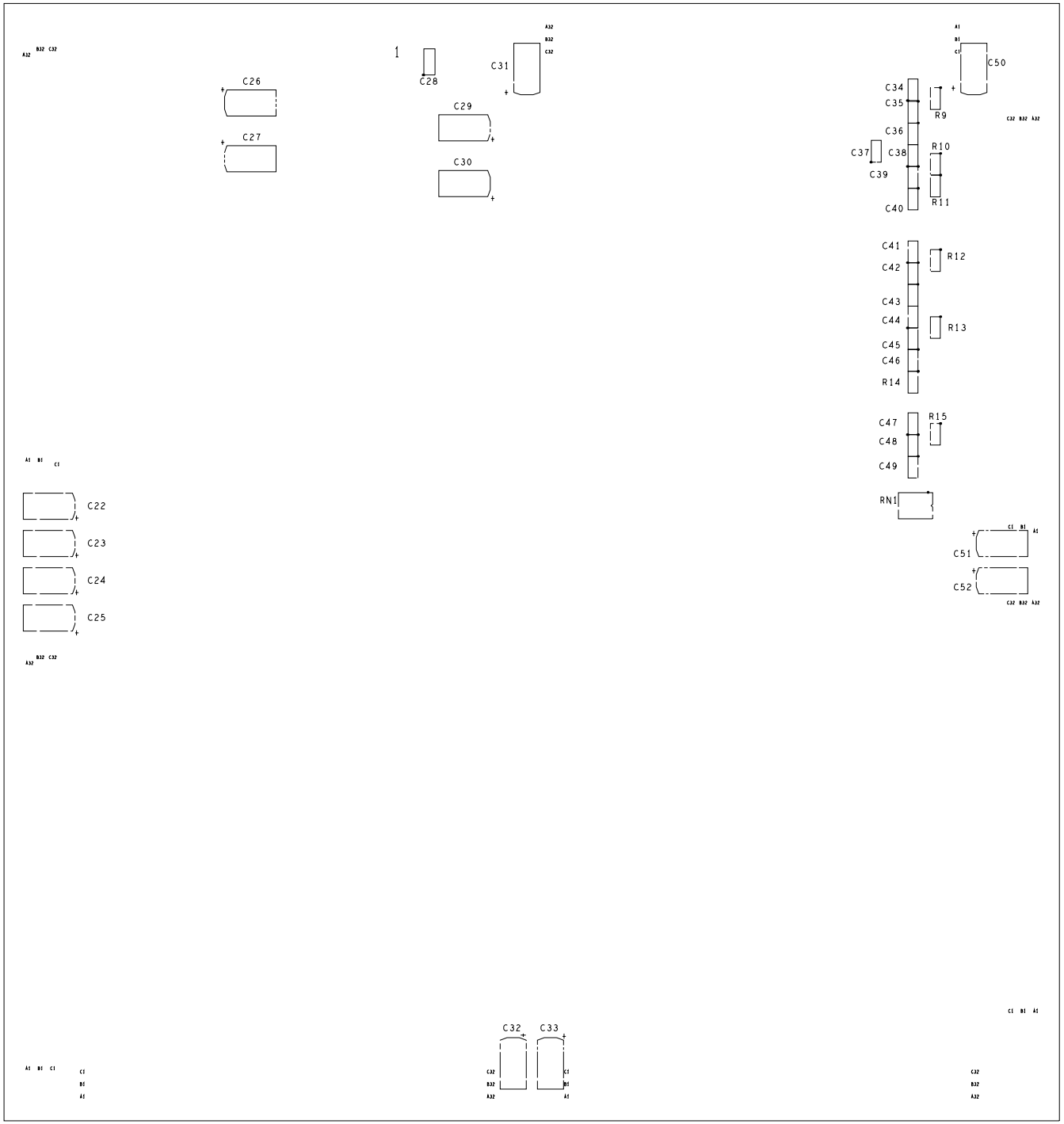
SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF

COMP BOTTOM



PMC-SIERRA MULTI PHY INTERFACE REV.2.0 1997


COMP TOP
edge of board
MALE RIGHT ANGLE
edge of board
edge of board
MALE RIGHT ANGLE
edge of board
FEMALE RIGHT ANGLE
edge of board
MALE RIGHT ANGLE
edge of board
FEMALE RIGHT ANGLE
edge of board
MALE RIGHT ANGLE
edge of board
MALE RIGHT ANGLE


C26
C27
C28
C29
C30
C31
C22
C23
C24
C25
C32
C33
C34
C35
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C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
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C49
C50
C51
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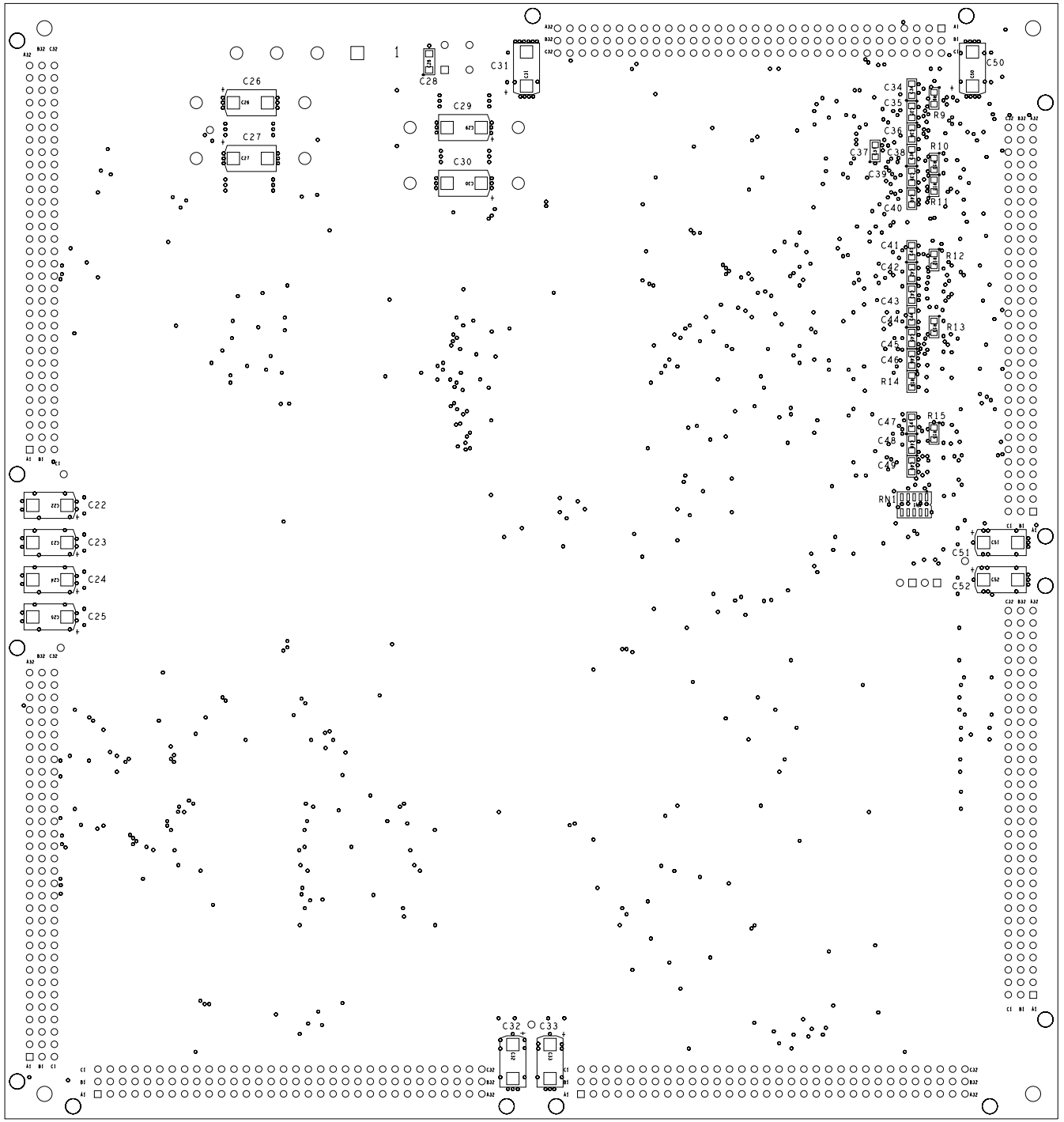
R9
R10
R11
R12
R13
R14
R15
RN1


C22
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C26
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C35
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C37
C38
C39
C40
C41
C42
C43
C44
C45
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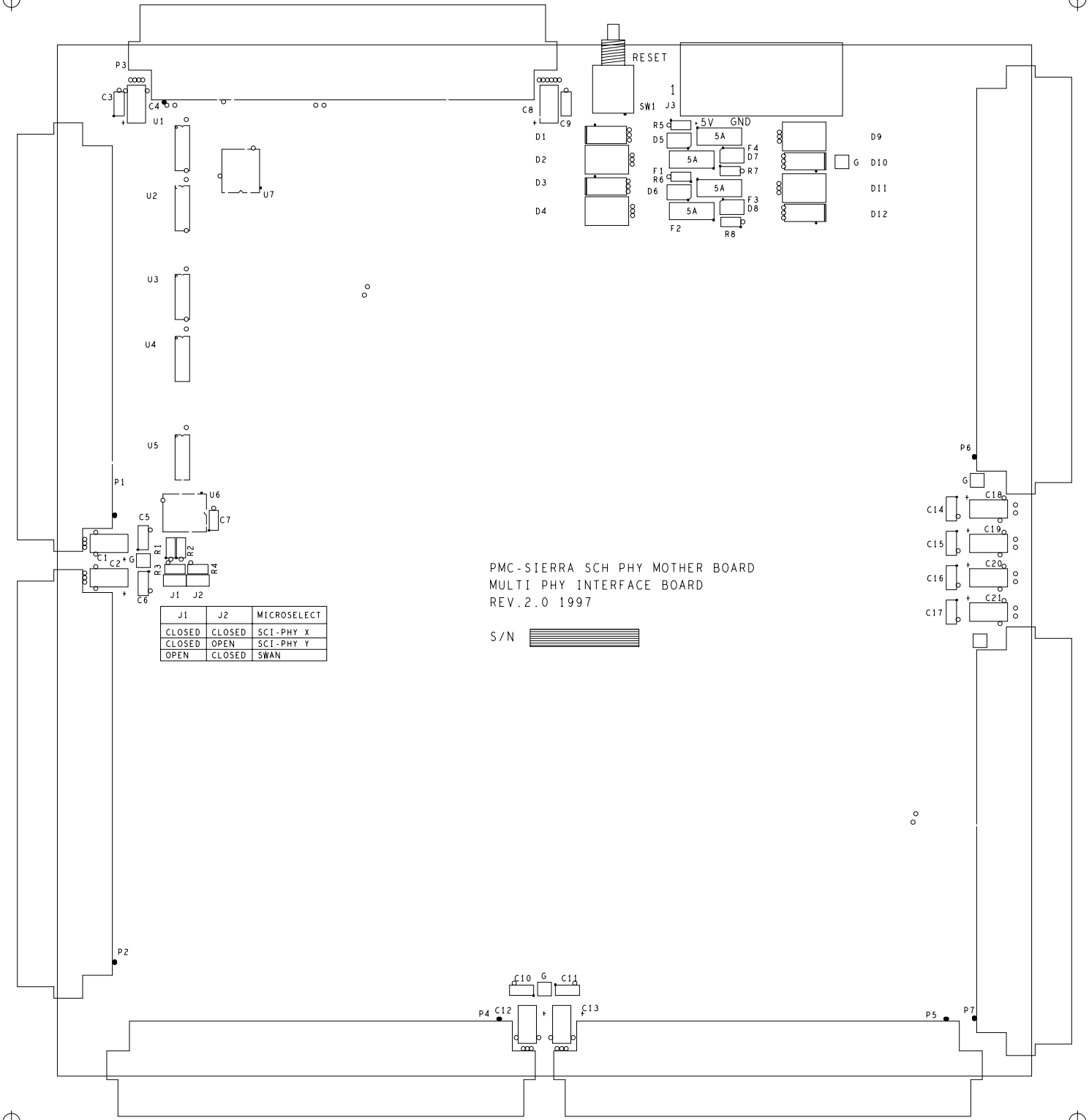
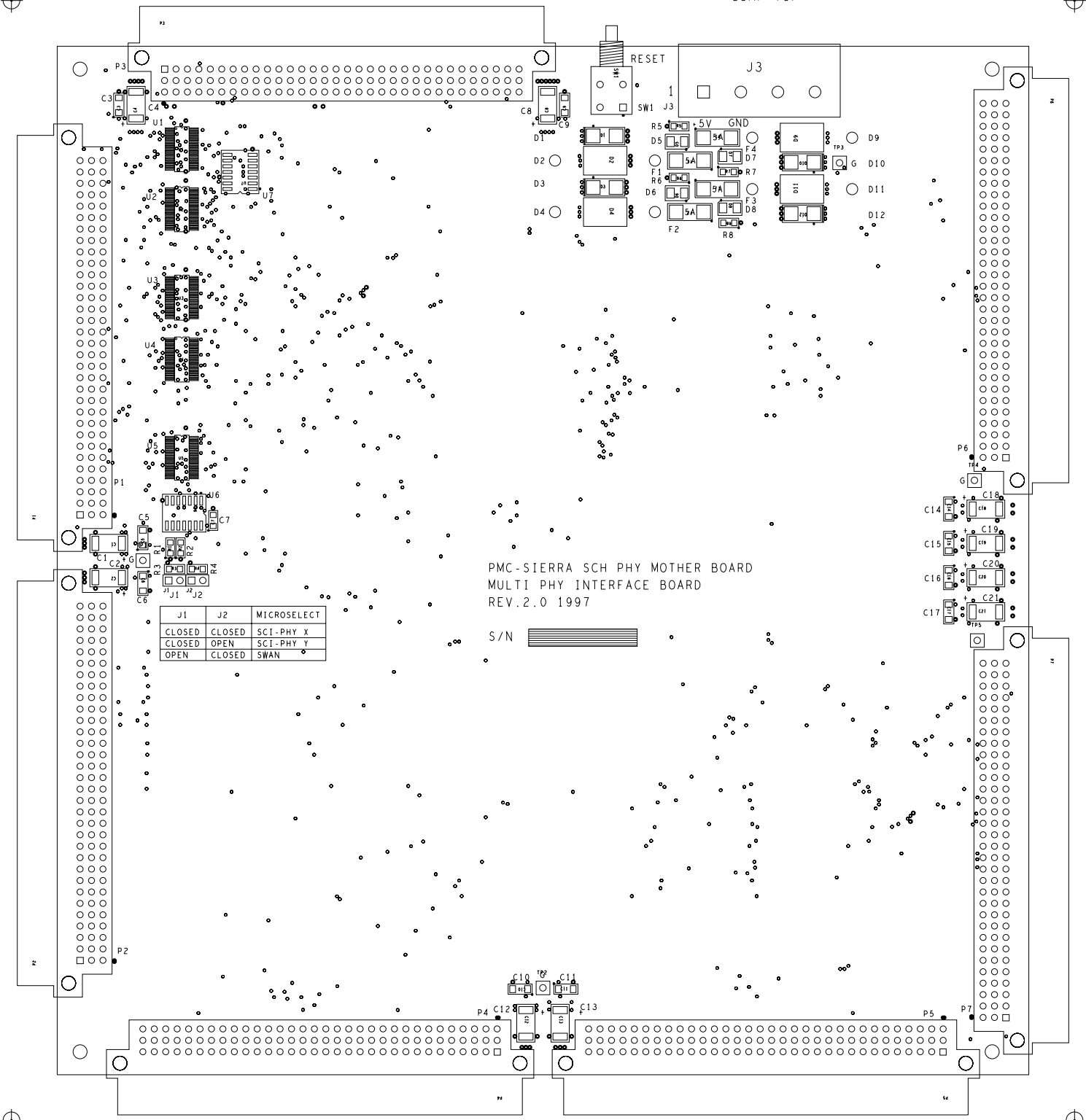
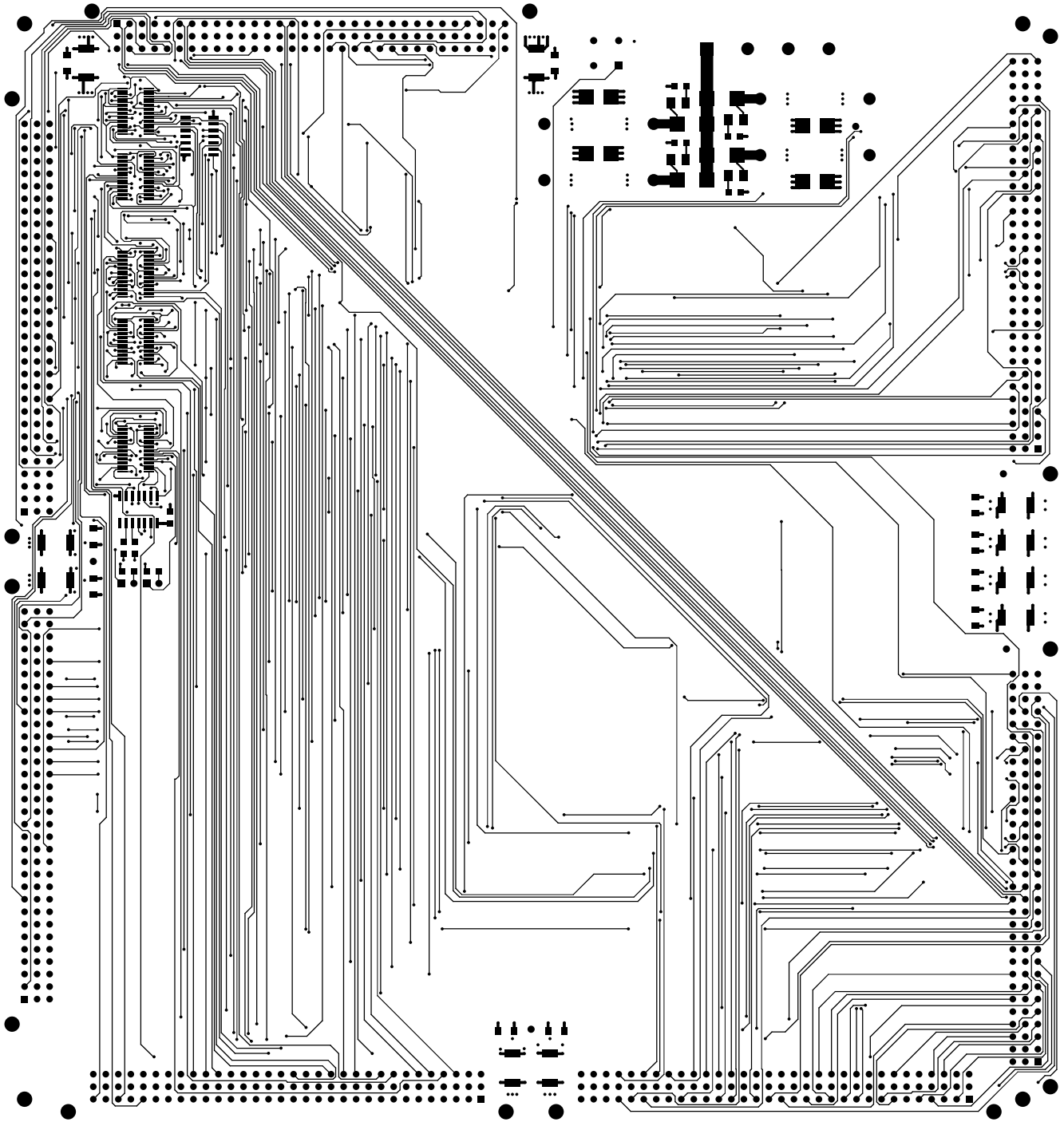
C51
C52
R9
R10
R11
R12
R13
R14
R15
RN1

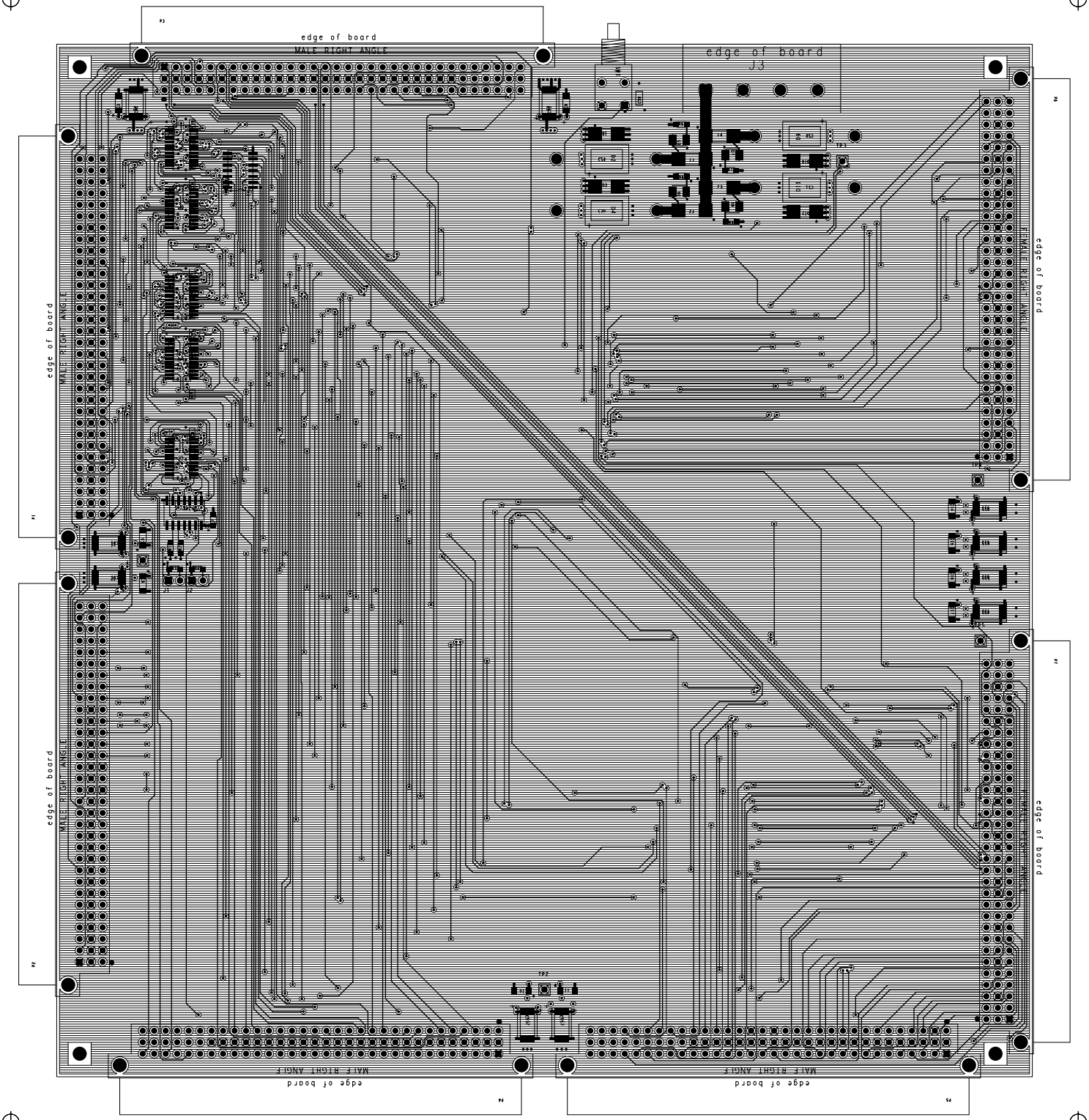


J1	J2	MICROSELECT
CLOSED	CLOSED	SCI-PHY X
CLOSED	OPEN	SCI-PHY Y
OPEN	CLOSED	SWAN

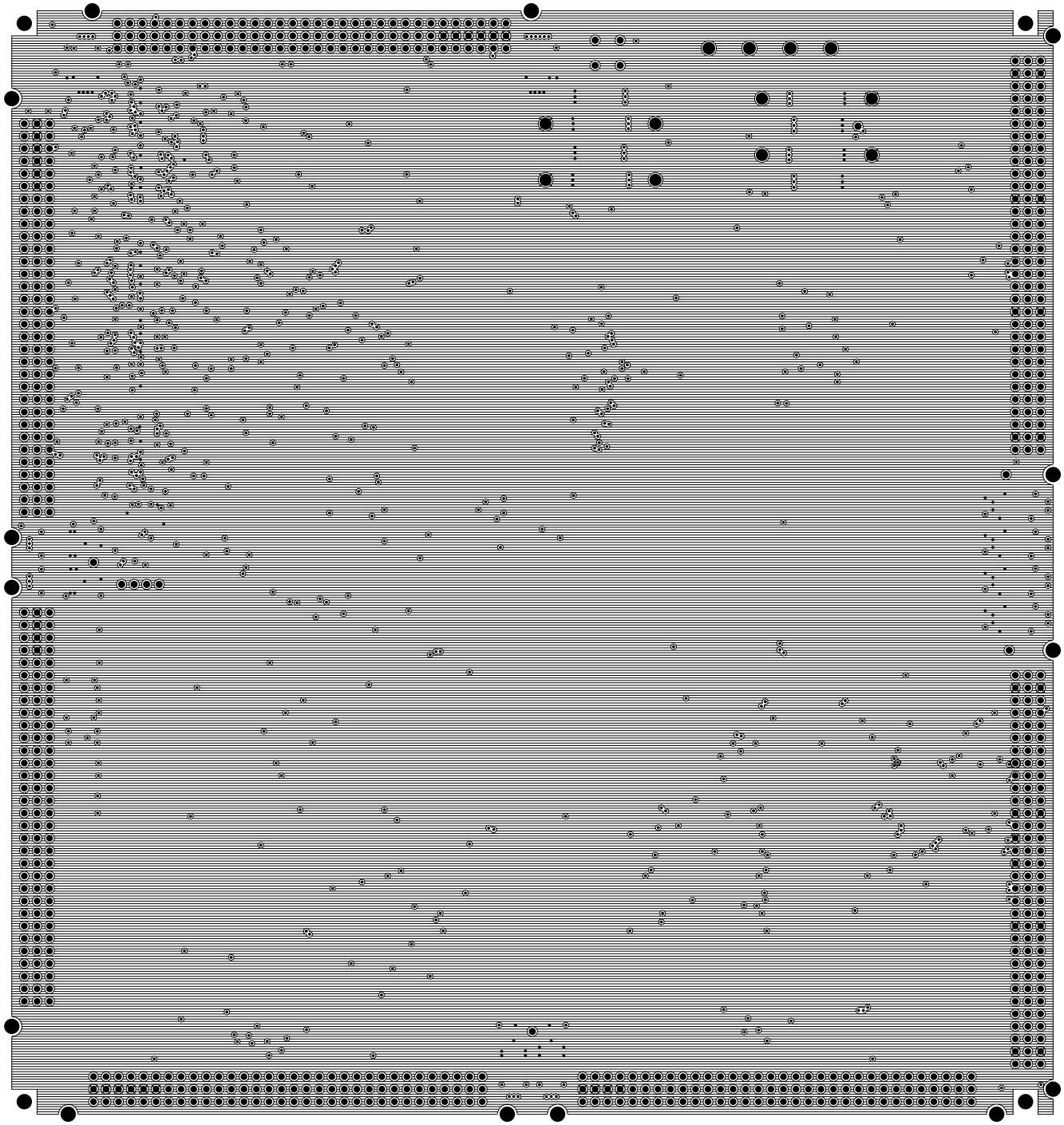


J1	J2	MICROSELECT
CLOSED	CLOSED	SCI-PHY X
CLOSED	OPEN	SCI-PHY Y
OPEN	CLOSED	SWAN




edge of board
MALE RIGHT ANGLE
edge of board
J3
edge of board
MALE RIGHT ANGLE
edge of board
MALE RIGHT ANGLE
edge of board
MALE RIGHT ANGLE
edge of board
MALE RIGHT ANGLE
edge of board
MALE RIGHT ANGLE

VCC PLANE



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NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

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