PM7346

S/UNI™ QJET

S/UNI-QJET

REFERENCE DESIGN

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1 OVERVIEW

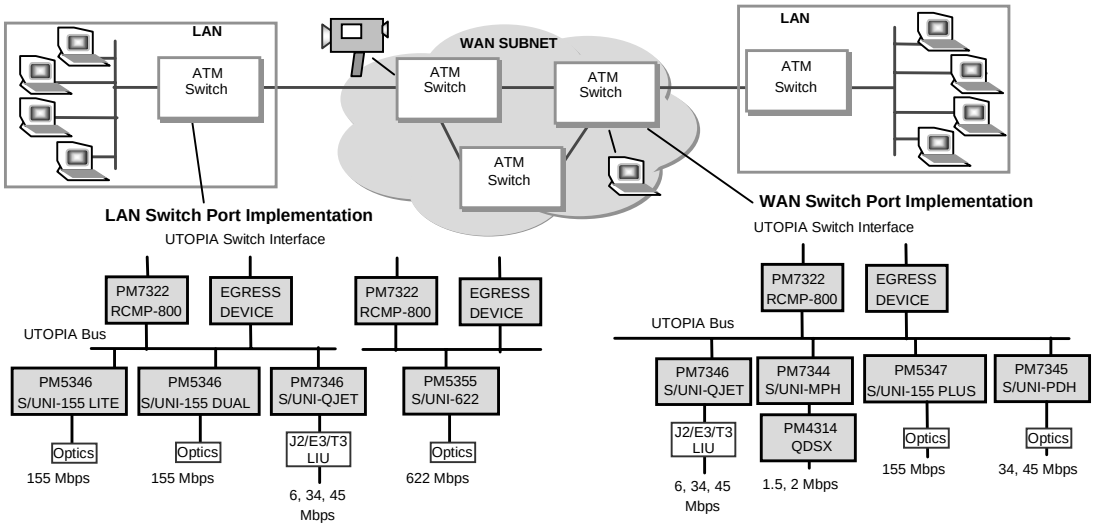
1.1 Application Perspective

The S/UNI-QJET standard product is a Quad ATM User Network Interface with on chip J2, E3, and DS-3 framers and Utopia Level 2 interface. The S/UNI-QJET provides ATM cell mapping to J2, E1, E3, DS-1, and DS-3 frame formats. The S/UNI-QJET may be interfaced to an ATM layer device such as the RCMP-800 using the Utopia Level 2 interface to create the ingress circuitry for an ATM switch port card.

ATM is a high performance networking technology that supports data transfer over connection oriented virtual paths. Data is transmitted in fixed sized cells containing header data used for switching, cell priority, flow control and header error control. It is capable of mixing various rates and types of traffic with minimal loss of service to users.

The versatility of ATM allows it to be used in nearly any data networking environment including internet backplanes, wide area networks, and local area networks. Typical line options include SONET/SDH, DS-1/E1, DS-3/E3, and J2. Figure 1 below illustrates the possible configurations for WAN and LAN ATM switch ports.

Figure 1 - ATM Overview



2 REFERENCES

[1] PMC-960835, PMC-Sierra Inc., PM7346 S/UNI-QJET Data Sheet, Issue 4, December 1997

[2] PMC-940904, PMC-Sierra Inc., PM7322 RCMP-800 Data Sheet, Issue 6, August 1997

[3] PMC-940212, PMC-Sierra Inc., SCI-PHY Level 2, Issue 3, November 1995

[4] PMC-960148, PMC-Sierra Inc., PM7322 RCMP-800 Reference Design, Issue 2, August 1997

[5] ATM Forum - Utopia, An ATM PHY Interface Specification, Level 2, Version 1", June 1995

[6] PMC-950946, PMC-Sierra Inc., Interfacing the D3MX to the SSI 78P7200 T3 LIU, Issue 1, September 1995

[7] PMC-971136, PMC-Sierra Inc., Channelizing J2 Data Streams with S/UNI-QJET and FREEDM-8, Issue 2, February 1998

3 FEATURE OVERVIEW

This reference design provides the following features:

- PLCP and direct mapping of ATM cells to DS-3, E3, and J2 frame formats.
- Two DS-3, one E3, and one J2 line interfaces.
- Line performance monitoring performed by PM7346 S/UNI-QJET.
- 8 or 16 bit, 50 MHz Utopia interface for ATM cell transfer.
- FPGA for terminal side loopback.
- Reference design provides an aggregate bandwidth of 130 Mbit/s.

4 FUNCTIONAL DESCRIPTION

4.1 Overview

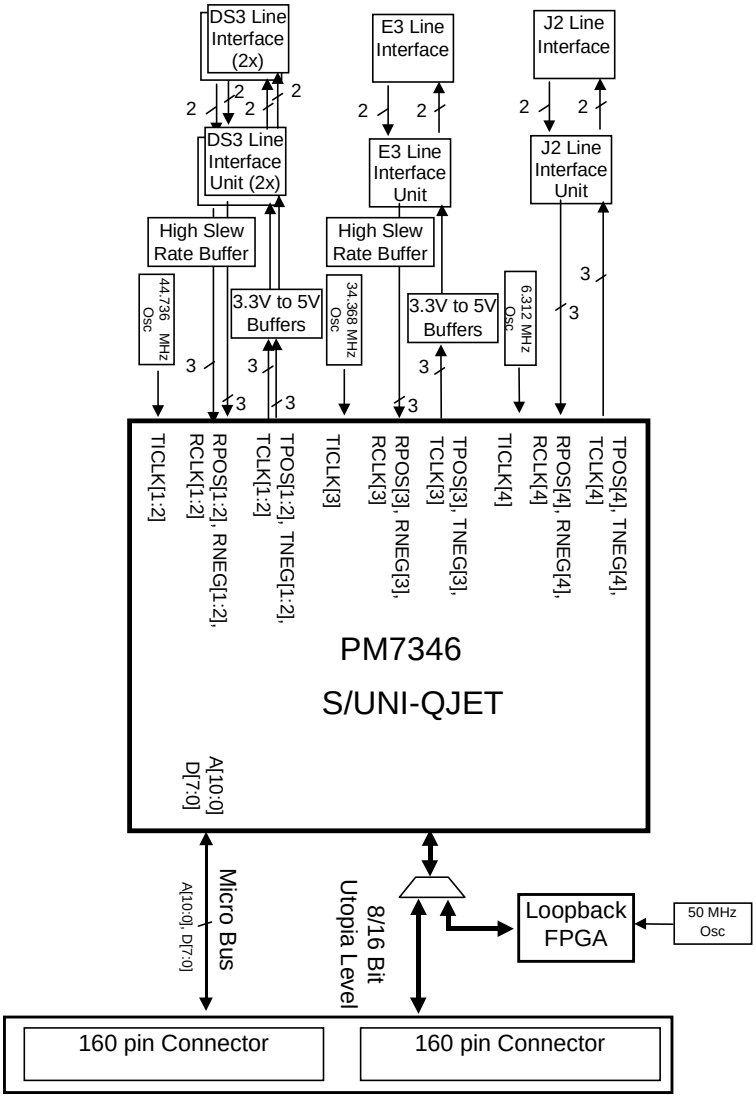
The S/UNI-QJET reference design is an ATM line card that implements ATM physical layer circuitry for J2, E3, and DS-3 lines. The line interface to this reference design is capable of interfacing to either one of the J2, E3, or DS-3 Plesiochronous Digital Hierarchy transport systems.

This reference design consists of one S/UNI-QJET with an FPGA for loopback and circuitry to interface line signals to the S/UNI-QJET. The card interfaces to two DS-3 lines, one E3 line, and one J2 line. There is also a Utopia Level 2 interface for cell transfer and a host access port to monitor and configure the board.

A block diagram of the reference design is shown in Figure 2.

4.2 Block Diagram

Figure 2 - Reference Design Card Block Diagram



Utopia 2 with Microcontroller Interface

4.3 Data Flow

Data flowing to the host is received on one of the J2, E3, or DS-3 line interfaces. LIU units for each line decode the analog signals on the line to digital signals indicating negative and positive line pulses. Clock information is also recovered and converted to a digital signal. These signals are then passed to the line side link interfaces of the S/UNI-QJET device. Each line side link interface consists of

two data pins to receive the negative and positive pulse signals, and a clock signal corresponding to pins RNEG, RPOS, and RCLK respectively.

The data is framed by the S/UNI-QJET units and ATM cells are delineated from the payload of the J2, E3, and DS-3 data streams. Received cells are stored in a four cell FIFO which outputs the data via the Utopia Level 2 interface. Each channel has a separate 4 cell FIFO. Data transferred from the S/UNI-QJET over the Utopia interface is controlled by an external ingress ATM layer device such as the PM7322 RCMP-200.

ATM cells to be transmitted over the J2, E3, and DS-3 lines are transferred to the card via the Utopia Level 2 interface, from an external egress ATM layer device. Cells are then mapped to the frame format for each channel and the resulting positive and negative pulse, and clock information are sent to the LIU's. Transmit clock information is derived from external crystal oscillators running at the transmit line rates. LIU units for each link encode the digital signals to J2, E3, or DS-3 analog signals.

4.4 S/UNI-QJET

The PM7346 S/UNI-QJET is a quad ATM physical layer processor with integrated DS3 E3, and J2 framers. PLCP sublayer DS1, DS3, E1, and E3 processing is supported as is ATM cell delineation.

The S/UNI-QJET contains integral DS3 framers, which provide DS3 framing and error accumulation in accordance with ANSI T1.107, and T1.107a, integral E3 framers, which provide E3 framing in accordance with ITU-T Recommendations G.832 and G.751, and integral J2 framers, which provide J2 framing in accordance with ITU-T Recommendation G.704.

When configured for DS3 transmission system sublayer processing, the S/UNI-QJET accepts and outputs either or both digital B3ZS-encoded bipolar and unipolar signals compatible with M23 and C-bit parity applications.

When configured for E3 transmission system sublayer processing, the S/UNI-QJET accepts and outputs either or both HDB3-encoded bipolars or unipolar signals compatible with G.751 and G.832 applications.

When configured for J2 transmission system sublayer processing, the S/UNI-QJET accepts and outputs either or both B8ZS-encoded bipolar or unipolar signals compliant with G.704 and NTT 6.312 Mbit/s applications.

In the DS3 receive direction, the S/UNI-QJET frames to DS3 signals with a maximum average reframe time of 1.5 ms and detects line code violations, loss

of signal, framing bit errors, parity errors, path parity errors, AIS, far end receive failure and idle code. The DS3 overhead bits are extracted and presented on serial outputs. When in C-bit parity mode, the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channels are extracted. HDLC receivers are provided for Path Maintenance Data Link support. In addition, valid bit-oriented codes in the FEAC channels are detected and are available through the microcontroller port.

In the E3 receive direction, the S/UNI-QJET frames to G.751 and G.832 E3 signals with a maximum average reframe times of 135µs for G.751 frames and 250µs for G.832 frames. Line code violations, loss of signal, framing bit errors, AIS, and remote alarm indication are detected. Further, when processing G.832 formatted data, parity errors, far end receive failure, and far end block errors are also detected; and the Trail Trace message may be extracted and made available through the microcontroller port. HDLC receivers are provided for either the G.832 Network Requirement or the G.832 General Purpose Data Link support.

In the J2 receive direction, the S/UNI-QJET frames to G.704 6.312 Mbit/sec signals with a maximum average reframe time of 5.07ms. An alternate framing algorithm which uses the CRC-5 bits to rule out 99.9% of all static mimic framing patterns is available with a maximum average reframe time of 10.22ms when operating with a 10^{-4} bit error rate. Line code violations, loss of signal, loss of frame, framing bit errors, physical layer AIS, payload AIS, CRC-5 errors, Remote End Alarm, and Remote Alarm Indication are detected. HDLC receivers are provided for Data Link support.

Error event accumulation is also provided by the S/UNI-QJET. Framing bit errors, line code violations, parity errors, path parity errors and far end block errors are accumulated, when appropriate, in saturating counters for DS3, E3, and J2 frames. Loss of Frame detection for DS3, E3, and J2 is provided as recommended by ITU-T G.783 with integration times of 1ms, 2ms, and 3ms.

In the DS3 transmit direction, the S/UNI-QJET inserts DS3 framing, X and P bits. When enabled for C-bit parity operation, bit-oriented code transmitters and HDLC transmitters are provided for insertion of the FEAC channels and the Path Maintenance Data Links into the appropriate overhead bits. Alarm Indication Signals can be inserted by using internal register bits; other status signals such as the idle signal can be inserted when enabled by internal register bits. When M23 operation is selected, the C-bit Parity ID bit (the first C-bit of the first M sub-frame) is forced to toggle so that downstream equipment will not confuse an M23-formatted stream with stuck-at 1 C-bits for C-bit Parity application.

In the E3 transmit direction, the S/UNI-QJET inserts E3 framing in either G.832 or G.751 format. When enabled for G.832 operation, an HDLC transmitter is

provided for insertion of either the Network Requirement or General Purpose Data Link into the appropriate overhead bits. The Alarm Indication Signal and other status signals can be inserted by internal register bits.

In the J2 transmit direction, the S/UNI-QJET inserts J2 6.312 Mbit/s G.704 framing. HDLC transmitters are provided for insertion of the Data Channels. CRC-5 check bits are calculated and inserted into the J2 multiframe. External pins are provided to enable overwriting of any of the overhead bits within the J2 frame.

The S/UNI-QJET also supports diagnostic options which allow it to insert, when appropriate for the transmit framing format, parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, all-zeros, AIS, Remote Alarm Indications, and Remote End Alarms.

The S/UNI-QJET provides cell delineation for ATM cells using the PLCP framing format, or by using the header check sequence octet in the ATM cell header as specified by ITU-T Recommendation I.432. DS1, DS3, E1 and E3 based PLCP frame formats can be processed. Non-PLCP-based cell delineation is accomplished with either bit, nibble, or byte-wide search algorithms, depending on the line interface used. An interface consistent with the generic physical interface defined by ITU-T Recommendation I.432 is provided for arbitrary rates up to 52 Mbit/s. This interface is used to provide physical layer support for transmission systems that do not have an associated PLCP sublayer, or to provide an efficient means of directly mapping ATM cells to existing transmission system formats (such as DS3 and DS1).

In the PLCP receive direction, framing, path overhead extraction and cell extraction is provided. BIP-8 error events, frame octet error events and far end block error events are accumulated.

In the PLCP transmit direction, the S/UNI-QJET provides overhead insertion using inputs or internal registers, DS3 nibble and E3 byte stuffing, automatic BIP-8 octet generation and insertion and automatic far end block error insertion. Diagnostic features for BIP-8 error, framing error and far end block error insertion are also supported.

In the cell receive path, idle cells may be dropped according to a programmable filter. By default, incoming cells with single bit HCS errors are corrected and written to the FIFO buffer. Optionally, cells can be dropped upon detection of a HCS error. Cell delineation may optionally be disabled to allow passing of all cells, regardless of cell delineation status. Assigned cells containing no detectable HCS errors are written to a FIFO buffer. Cells data is read from the FIFO using a synchronous 50 MHz 8-bit wide or 16-bit wide Utopia Level 2

compatible interface. Cell data parity is also provided. Counts of error-free assigned cells, and cells containing HCS errors are accumulated independently for performance monitoring purposes.

In the cell transmit path, cell data is written to a FIFO buffer using a synchronous 50 MHz 8-bit wide or 16-bit wide Utopia Level 2 interface. Cell data parity is also examined for errors. Idle cells are automatically inserted when the FIFO contains less than one full cell. HCS generation, cell payload scrambling, and cell header scrambling (for use with PPP packets) are optionally provided. Counts of transmitted cells are accumulated for performance monitoring purposes.

Both receive and transmit cell FIFOs provide buffering for four cells. The FIFOs provide the rate matching interface between the higher layer ATM entity and the S/UNI-QJET.

The S/UNI-QJET is configured, controlled and monitored via a generic 8-bit microcontroller bus through which all internal registers are accessed. All sources of interrupts can be identified, acknowledged, or masked via this interface.

4.5 Loopback FPGA

A single FPGA is used to perform loopback on the Utopia bus. This loops back the cells received by the S/UNI-QJET. The FPGA acts as a Utopia master in both transmit and receive directions. The FPGA uses direct cell indication and a round robin scheme to select input PHY sources for each cell transmission. Received data is transmitted through the same port from which it was received. Loopback is enabled by writing a ‘1’ to bit 4 of the onboard configuration register and asserting the “REG_OEB” signal low or closing jumper J3 (refer to schematics).

The FPGA also implements channelized J2 functionality for the J2 port of the reference design. This is included to verify the logic design presented in [7] PMC-971136, “Channelizing J2 Data Streams with S/UNI-QJET and FREEDM-8”.

4.6 J2 Line Interface

One Transwitch MRT TXC02050 J2 LIU is used to provide the J2 line interface to the S/UNI-QJET device. The LIU converts the digital B8ZS encoded data to its analog equivalent and converts analog B8ZS to it’s digital equivalent.

In the receive direction, the LIU provides TTL level receive clock, and positive and negative receive data. In the transmit direction the LIU receives TTL level transmit clock, and positive and negative transmit data. The TTL input and output

levels are directly compatible with the S/UNI-QJET. Buffers are required on the line side to drive the line transformers.

4.7 DS-3 Line Interface

Two TDK TSC 78P7200 LIUs are used to provide two DS-3 interfaces to ports 1, and 2 of the S/UNI-QJET device. The LIU converts transmit digital B8ZS encoded data to its analog equivalent and converts receive analog B8ZS to its digital equivalent.

In the receive direction, the LIU provides a CMOS level receive clock, and positive and negative receive data. In the transmit direction the LIU receives a CMOS level transmit clock, and positive and negative transmit data. CMOS level signals are compatible with the S/UNI-QJET's inputs, however, as the S/UNI-QJET is a 3.3 V device, a voltage buffer is required to boost the output signals of the S/UNI-QJET to match the levels required by the 78P7200. Also, because of the low slew rate of the TDK TSC 78P7200 device, buffers are used to increase the slew rate of the signals sent to the S/UNI-QJET.

4.8 E3 Line Interface

One TDK TSC 78P7200 LIU is used to provide an E3 interface to port 3 of the S/UNI-QJET device. The LIU converts transmit digital HDB3 encoded data to its analog equivalent and converts receive analog HDB3 to its digital equivalent. Note that although this is the same LIU as used for the DS-3 line interface, the surrounding circuitry is different.

In the receive direction, the LIU provides a CMOS level receive clock, and positive and negative receive data. In the transmit direction the LIU receives a CMOS level transmit clock, and positive and negative transmit data. CMOS level signals are compatible with the S/UNI-QJET's inputs, however, as the S/UNI-QJET is a 3.3 V device, a voltage buffer is required to boost the output signals of the S/UNI-QJET to match the levels required by the 78P7200. Also, because of the low slew rate of the TDK TSC 78P7200 device, buffers should be used to increase the slew rate of the signal sent to the S/UNI-QJET.

4.9 3.3 Volt to 5 Volt Converter

The S/UNI-QJET uses a 5 volt reference pin to allow inputs to tolerate 5 volt input signals. However, the S/UNI-QJET can only produce a guaranteed output high voltage of 2.4 volts. In this design, 74ACT125, advanced TTL compatible CMOS buffers, are used to convert the 2.4 volt output high voltage to the required 3.5 volt level required by the E3/DS-3 LIU units. Note that the J2 LIU

used in this design is voltage compatible with the S/UNI-QJET and thus does not require a buffer. **Note that the Utopia clock signals TFCLK and RFCLK are not 5 volt tolerant**.

4.10 High Slew Rate Buffers

High slew rate buffers are required to correct possible problems caused by the slow slew rate of the E3 and DS-3 LIU's combined with the TTL logic levels expected by the S/UNI-QJET. Without this buffer the duty cycle of signals sent from the E3 and DS-3 LIU's to the S/UNI-QJET will suffer duty cycle distortion. A detailed explanation of this problem is found in [6] PMC-950946, "Interfacing the D3MX to the SSI 78P7200 T3 LIU". Note that the SSI 78P7200 has an identical slew rate to the TDK TSC 78P7200 used in this design.

4.11 Utopia Level 2 with Microprocessor Interface

Two 160 pin male connectors provide necessary connections for Utopia operation and microprocessor access. The first 160 pin connector is used to carry 5V and 3V power, microprocessor and Utopia clock signals. The second carries the Utopia bus signals.

5 EXTERNAL INTERFACE SIGNAL DESCRIPTION

This board has a 160 pin male Utopia Level 2 compliant interface for data transfer to and from the board. The 160 pin microprocessor interface provides a user interface for configuration and monitoring of the board as well as the receive and transmit clock signals for the Utopia bus. The Utopia interface connects the board to ATM layer devices. The 160 pin Utopia interface provides a large number of ground connections physically distributed along the connector to reduce interference between circuits and provide a similar characteristic impedance across the connector for critical signals.

5.1 Utopia with Microprocessor Interface

The table below indicates the use of each pin in the 160 pin microprocessor and Utopia clock connector of the Utopia with Microprocessor interface.

Table 1 - Microprocessor with Utopia Clock Connector Definition

Pin Name	Type	Pin No.	Function
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	INPUT / OUTPUT	D1 C1 D2 C2 D3 C3 D4 C4	Data Bus. D[7:0] is a eight bit bi-directional data used for microprocessor read and write access
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	INPUT	D9 D10 D11 D12 D13 D14 D15 D16 C9 C10 C11	Address Bus. A[10:0] is an eleven bit address bus that selects specific registers in the S/UNI-QJET during microprocessor access

Pin Name	Type	Pin No.	Function
REG_OEB	INPUT	B17	Register output enable signal. This active low signal enables the output of the configuration register
REG_CSB	INPUT	C23	Active Low Chip select for onboard configuration register.
PHY_ADR[0] PHY_ADR[1] PHY_ADR[2]	INPUT	A14 A15 A16	PHY Address select signals for external selection of board PHY address.
RSTB	INPUT	B18	Active Low Reset for the board.
ALE	INPUT	A22	Address Latch Enable
RDB	INPUT	B22	Read Enable. Active low signal
WRB	INPUT	C22	Write Enable. Active low signal
CSB	INPUT	D23	Chip Select for S/UNI-QJET. The active-low chip select is low during S/UNI-QJET register accesses
INTB	OUTPUT	D27	Active low interrupt from S/UNI-QJET.
RXLCK-	OUTPUT	D35	Negative differential receive clock signal. This signal, along with RFCLK+ comprise the differential RFCLK clock signal sent across the connector. RFCLK is to be used as a reference to sample RDAT.
RXCLK+	OUTPUT	D36	Positive differential receive clock signal. This signal, along with RFCLK- comprise the differential RFCLK clock signal sent across the connector. RFCLK is to be used as a reference to sample RDAT.
TXCLK+	INPUT	D39	Positive differential receive clock signal. This signal, along with TFCLK- comprise the differential TFCLK clock signal sent across the connector. TFCLK is used as a reference to sample TDAT.

Pin Name	Type	Pin No.	Function
TXCLK-	INPUT	D40	Negative differential receive clock signal. This signal, along with TFCLK+ comprise the differential TFCLK clock signal sent across the connector. TFCLK is used as a reference to sample TDAT.
TCK	INPUT	B28	Test port clock. Provides timing for test operations.
TMS	INPUT	A28	This signal controls the operations that can be carried out using the test access port
TDI	INPUT	C28	Test Data Input. This signal carries test data into the S/UNI-QJET.
TDO	OUTPUT	D28	Test Data Output. This signal carries test data out of the S/UNI-QJET.
NC	NC	A20 - A21 A23 - A40 B19 - B21 B23 - B30 C5 - C8 C12 - C17 C19 - C21 C24 - C30 D5 - D8 D20 - D22 D24 - D26 D28 - D34 D37 - D38	Not Connected.
+ 5V	POWER	A1 - A2 B1 - B2	+ 5 Volt supply
+ 3.3V	POWER	A3 - A9 B3 - B9	+ 3.3 Volt supply
GND	GND	A10 - A13 A17 - A19 B10 - B16 B31 - B40 C31 - C40	Ground

Table 2 below indicates the use of each pin in the 160 pin Utopia Data and Control portion of the Utopia with Microprocessor interface.

Table 2 - Utopia Connector Definition

Pin Name	Type	Pin No.	Function
RXDAT[0] RXDAT[1] RXDAT[2] RXDAT[3] RXDAT[4] RXDAT[5] RXDAT[6] RXDAT[7] RXDAT[8] RXDAT[9] RXDAT[10] RXDAT[11] RXDAT[12] RXDAT[13] RXDAT[14] RXDAT[15]	OUTPUT	A1 D1 A2 D2 A3 D3 A4 D4 A5 D5 A6 D6 A7 D7 A8 D8	Receive Cell Data Bus. This bus carries the ATM cell octets that are read from the selected receive FIFO.
RXPRTY	OUTPUT	A9	Receive bus parity. The receive parity signal indicates the parity of the RXDAT bus.
DXRCA[1] DXRCA[2] DXRCA[3] DXRCA[4]	OUTPUT	A10 A11 A12 A13	Direct Receive Cell Available. These signals indicate available cells to be transferred across the Utopia bus for each of the four PHY ports of the S/UNI-QJET.
RXADDR[0] RXADDR[1] RXADDR[2] RXADDR[3] RXADDR[4]	INPUT	D9 D10 D11 D12 D13	Receive Address. The RXADDR[4:0] bus is used to select the port that is to be read from or being polled.
RXENB	INPUT	A14	Receive Multi-PHY Read Enable. The RXENB signal is an active low input which is used to initiate reads from the receive FIFOs of the S/UNI-QJET.
RXCLAV	OUTPUT	A15	Receive Multi-PHY Cell Available signal. This signal is used to indicate an available cell during receive PHY port polling

Pin Name	Type	Pin No.	Function
RXSOC	OUTPUT	D14	Receive Start of Cell. The Receive start of cell signal marks the start of cell on the RXDAT bus.
TXENB	INPUT	A27	Transmit Multi-PHY Write Enable. The TXENB signal is an active low input which is used to initiate writes to the transmit FIFOs of the S/UNI-QJET.
TXCLAV	OUTPUT	D26	Transmit cell available signal. This signal is used to indicate available cell FIFO space by polled PHY ports.
TXSOC	INPUT	A28	Transmit Start of Cell. The transmit start of cell signal marks the start of cell on the TXDAT bus.
TXADDR[0] TXADDR[1] TXADDR[2] TXADDR[3] TXADDR[4]	INPUT	D27 D28 D29 D30 D31	Transmit Address. The TXADDR[4:0] bus is used to select the port that is to be written to or being polled.
DTCA[1] DTCA[2] DTCA[3] DTCA[4]	OUTPUT	A29 A30 A31 A32	Direct Receive Cell Available. These signals indicate available cells to be transferred across the Utopia bus for each of the four PHY ports of the S/UNI-QJET
TXPRTY	INPUT	D32	Transmit bus parity. The transmit parity signal indicates the parity of the TDAT bus.

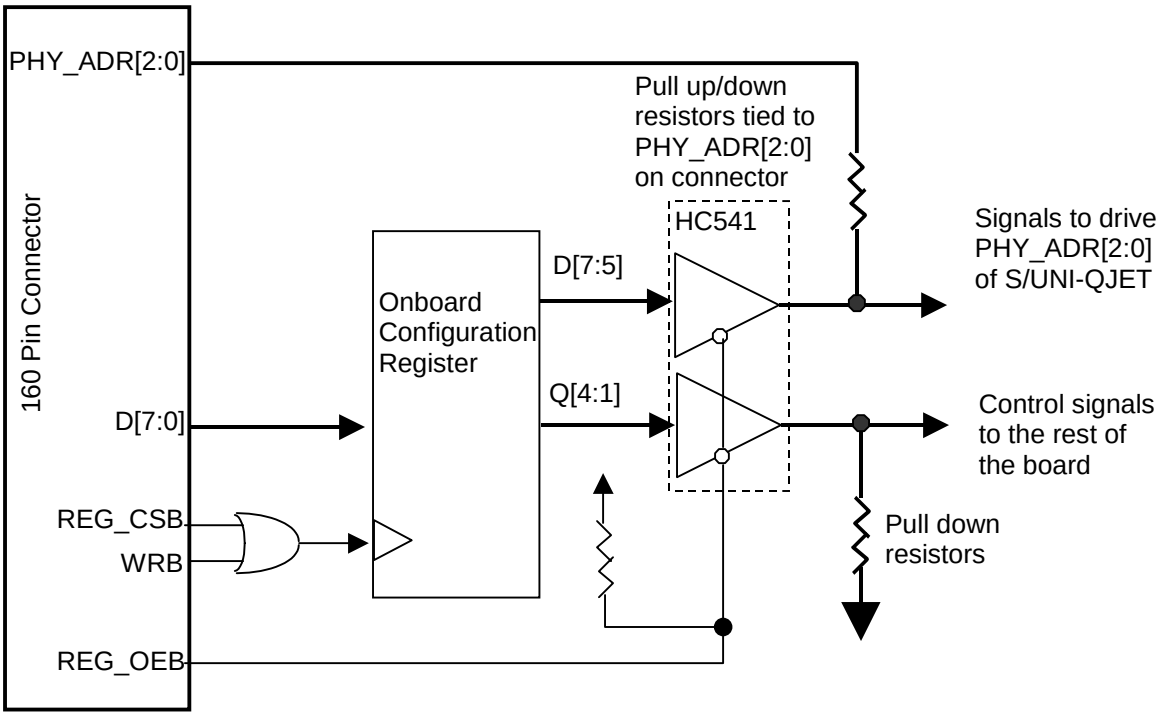
Pin Name	Type	Pin No.	Function
TXDAT[0] TXDAT[1] TXDAT[2] TXDAT[3] TXDAT[4] TXDAT[5] TXDAT[6] TXDAT[7] TXDAT[8] TXDAT[9] TXDAT[10] TXDAT[11] TXDAT[12] TXDAT[13] TXDAT[14] TXDAT[15]	INPUT	A40 D40 A39 D39 A38 D38 A37 D37 A36 D36 A35 D35 A34 D34 A33 D33	Transmit Cell Data Bus. This bus carries the ATM cell octets that are written to the selected transmit FIFO.
GND	GND	B1 - B40 C1 - C40	Ground pins.
NC	NC	A16 - A26 D15 - D25	No Connection

6 SOFTWARE INTERFACE

Software configuration for the S/UNI-QJET Reference design requires microprocessor access to the S/UNI-QJET configuration registers and the onboard configuration register. Access to the registers of the S/UNI-QJET registers requires an eight bit data, eleven bit address microprocessor interface with chip select, read enable and write enable signals.

The outputs of the on board configuration register drive control signals through an HC541 buffer to the rest of the board. These control signals include signals to that uniquely identify the Utopia PHY address of the board. This is illustrated in Figure 3 below.

Figure 3 - Onboard Register Hardware



Pull up and pull down resistors are placed on the outputs of the buffer to put the board into a default state when the buffer is tri-stated. The output enable of the buffer is controlled by the REG_OEB signal on the Utopia with Microprocessor connector. By default the buffer is tri-stated (REG_OEB is '1'). When the buffer is tri-stated, the Utopia PHY address is set by the value of the PHY_ADR[2:0] signals present on the connector. This allows multiple S/UNI-QJET boards to be

plugged into a single host board since different PHY addresses using these hardwired values can be automatically set by the host board after power up. This prevents contention on the Utopia bus before the microprocessor has a chance to set the PHY address by software.

After the value of the configuration register is set, the REG_OEB signal is driven low by the microprocessor of the host board to enable the outputs of the buffer. When REG_OEB is '1' and the buffer is not driving, the control signals LB_EN, LBO1, LBO2, and J2_EN are pulled low.

To write to the onboard configuration register, the register must be selected using REG_CSB. New values for the register are latched on the rising edge of WRB+REG_CSB. For more details on the S/UNI-QJET register space, refer to [1] PMC-960835 "PM7346 S/UNI-QJET Data Sheet".

Table 3 below describes the bits of the onboard configuration register.

Table 3 - Onboard Configuration Register

Bit	Type	Function	Default
7	W	PHY_ADR[2]	X
6	W	PHY_ADR[1]	X
5	W	PHY_ADR[0]	X
4	W	LB_EN	X
3	W	LBO[1]	X
2	W	LBO[2]	X
1	W	J2_EN	X
0		Unused	

Note that the value of the onboard register has no effect unless the REG_OEB signal is low.

PHY_ADR[2:0]

The PHY_ADR bits set the Utopia PHY address of the S/UNI-QJET device.

LB_EN

When a '1' is written to the LB_EN bit and the J2_EN bit is a '0', the board is placed into loopback mode. If the J2_EN bit is also a '1' then the board is put in channelized J2 mode.

LBO[2:1]

These bits set the line build out for the two DS-3 ports (ports 1 and 2) of the reference design. Line build out for port 1 is set by the LBO[1] bit and line build out for port 2 is set by the LBO[2] bit. When a '1' is written to either of the LBO bits, the LBO for the corresponding port will be configured for transmission distances less than 225 feet. When a '0' is written to either of the LBO bits, the LBO for the corresponding port will be configured for transmission distances greater than 225 feet.

J2_EN

The J2_EN bit, together with the LB_EN bit, configure the board for channelized J2 operation. When the value of both bits is '1', then the board is put into channelized J2 mode. When the LB_EN bit is '0' the J2_EN bit has no effect.

7 IMPLEMENTATION DESCRIPTION

7.1 Sheet 1: Root Drawing

This sheet gives a simplified overview of the design, dividing it into it's major components. These are the line interfaces, the S/UNI-QJET, the loopback FPGA, and the Utopia with microprocessor interface.

7.2 Sheet 2: Loopback FPGA Block

- An ACTEL 42MX09 is used to implement Utopia loopback and channelized J2.
- PI5C16212 Bus switches U3, U4, U15, U17, and U18 connect the Utopia signals from the S/UNI-QJET to either the Loopback FPGA or the board connectors. These switches are controlled by the LB_EN signal. When in loopback, the signals driving the board connector are tied low by resistor arrays connected through the bus switches.
- The receive Utopia clock of the S/UNI-QJET may be driven from a board interfaced to the Utopia with Microprocessor Interface or from the 74FCT3807 3.3V clock driver U2. To drive the clock from U2, resistors R16 and R20 are populated while jumper JP1 is left open. To drive the clock from a board connected through the Utopia with Microprocessor Interface, R16 and R20 should be left unpopulated and JP1 should be set.
- The transmit clock is supplied from the board connector. During loopback, transmit and receive clocks are both supplied by the 74FCT3807 clock driver.
- Headers are provided to allow access to signals to verify the channelized J2 logic.

7.3 Sheet 3: QJET Block

- A diode D3 is used to ensure that the voltage applied to the BIAS pins on the S/UNI-QJET is always greater or equal to that on the 3.3v power pins.
- Three oscillators provide clocks for the three line rates used in this reference design. Y2 provides clocks for the two DS-3 quadrant of the S/UNI-QJET, Y3 provides a clock for the E3 quadrant of the S/UNI-QJET, and Y4 provides clocks for the J2 quadrant of the S/UNI-QJET, and the J2 LIU.

- A configuration register U24 allows software configuration of the board through microprocessor access. The register controls loopback, channelized J2 operation, line build out for the DS-3 LIU's, and the PHY address for the board. A tri-state buffer is used to drive control signals with the corresponding register output. Placing the buffer in tri-state leaves the board in it's default configuration of no loopback, no channelized J2, line build out for 225' or longer DS-3 transmission, and PHY address of "000".

- 74ACT125 buffers are used to translate the 3v CMOS level outputs of the S/UNI-QJET to the 5v CMOS levels required by the TDK72P7800 LIU units U16, U19, and U20.

7.4 Sheet 4: J2 Line Interface

- 74ACT125 buffers are used to drive the line transformer, ensuring that the output capability of the LIU U28 is not exceeded.

7.5 Sheets 5 and 6: E3 Line Interface and T3 Line Interface

- Analog receive and transmit power are separated by ferrite beads to prevent interference between the two power planes.

- 74ACT08 AND gates U26 are used to increase the slew rate of the signals output from the LIU U16. When the signal received by the LIU is too low, the LOWSIGB signal of the LIU disables the data and clock output from the device to avoid erroneous data being passed to the S/UNI-QJET device.

- Component values are chosen according to manufacturer specification for the line rate used (E3 or DS-3)

7.6 Sheet 7: Utopia and Micro Interface

- Balun transformer T8 is used to transform the differential Utopia transmit clock signal from the Micro and Utopia Clock connector to a single ended signal for the S/UNI-QJET. Balun transformer T7 is used to transform the single ended Utopia receive clock from the board to a differential clock for the Micro and Utopia Clock connector.

- LED's are used driven by the S/UNI-QJET FRMSTAT pins to indicate various framing status conditions according to the contents of the STATSEL bits in the S/UNI-QJET's Configuration Register 2.

- The reset signal RSTB may be activated from either the push button on board or an external signal from the connector. An AND gate U38 is used to drive RSTB from either of these two sources.

7.7 Sheet 8: Power Supply and Decoupling

- Power may be supplied through the Microprocessor with Utopia Clock connector or through a separate 4 pin Molex connector, but not both. Solder bridges are used to select the desired power source.

- De-coupling capacitors for the S/UNI-QJET are placed such that each power pin has a capacitor nearby.

8 OPERATIONS

8.1 System Setup

The S/UNI-QJET reference board is designed to transmit and receive data at DS-3, E3, and J2 data rates on the line side while transferring ATM cells across the 50 MHz Utopia Level 2 bus. The board is controlled through the microprocessor portion of the Utopia with Microprocessor interface.

The PHY address of the board is configured using pins also residing on the Utopia with Microprocessor interface. These pins should be tied low by the ATM layer board if only one PHY board is interfaced to the Utopia bus. If more than one board is to reside on the Utopia bus, each PHY board connector must have it's own default PHY address set by tying the PHY_ADR pins of the connector to a unique value. However, if the value is "111" the fourth quadrant of the PHY device would have the same address as the Utopia null address "11111" and will not be used.

8.2 Board Configuration

Before data can be transmitted or received, each quadrant of the S/UNI-QJET must be configured for the correct line rate. Other options may be modified as desired, see [1] "PM7346 S/UNI-QJET Data Sheet" for more information.

The onboard register may be written to configure the board for loopback, enable channelized J2, change the PHY address, and line build out for the DS-3 LIU's. Writing to the register requires clocking data in using REG_CSB + WRB. Bits 5 to 7 of the register set the PHY address of the board, bit 4 puts the board into loopback, bits 2 and 3 determine the line build out of the DS-3 LIU's and bit 1 with bit 4, sets the board to perform channelized J2. After writing to the register, the REG_OEB signal must be held low to drive the appropriate control signals and PHY_ADR pins of the S/UNI-QJET. Otherwise, the PHY_ADR signals from the connector determine the PHY address, and the other control signals are pulled low (normal operation).

The DS-3 line interfaces have a default line build out for transmission length greater than 225 feet. Setting the LBO signals of either DS-3 interface to 1 will set the line build out for transmission distance less than 225 feet.

Setting the board to loopback mode requires that the S/UNI-QJET be set to de-assert DRCA 5 cycles early at the end of cells. Bit 4 should be set to one to enable loopback.

To enable the channelized J2 operation, the S/UNI-QJET should be put in framer only mode and bits 4 and 1 of the register should also be set to '1'.

8.3 Jitter Attenuation for E3

This reference design does not provide circuitry to attenuate output jitter as required by E3 related standards. Jitter attenuation circuitry for the TDK72P7800 line interface units are available directly from TDK semiconductor for TDK customers. To contact TDK semiconductor please visit their web page at www.tsc.tdk.com.

9 BILL OF MATERIALS

Table 4 - Bill of Materials

NO.	Description	Part Number	Reference Description	Qty
1	1N4148	1N4148W	D6	1
2	1N5817	1N5817M	D3	1
3	42MX09_PL84	42MX09_PL84	U21	1
4	74F32	SN74F32D	U22	1
5	74FCT3807	PI49FCT3807	U2	1
6	74HC08	SN74HC08D	U38	1
7	74HC541	SN74HC541DW	U25	1
8	74HCT377	SN74HCT377DW	U24	1
9	74AC08	74AC08D	U26, U27, U29	3
10	74ACT125	74ACT125D	U8, U10-U13	5
11	74LPT541	PI74LPT541CS	U9	1
12	78P7200	TSC78P7200-IH TDK	U16, U19, U20	3
13	BALUN-BASE	Toko 617DB-1024	T7, T8	2
14	BNC_AMPHENOL-BASE	DIGI-KEY - ARF1065-ND	J4-J11	8
15	CAPACITOR-0.01UF, 50V, X7R_805	NEWARK - 499-225	C34, C35, C38-C40, C51-C55, C59, C64, C69, C72, C73, C77, C80, C88, C90, C104, C107, C108, C127	23
16	CAPACITOR-0.022UF, 50V, X7R_805	NEWARK - 578-198	C61, C82, C84	3
17	CAPACITOR-0.1UF, 25V, Y5V_805	NEWARK - 52F020	C1-C28, C30, C31, C37, C41-C44, C48-C50, C56, C58, C63, C65, C68, C76, C78, C86, C87, C91, C92, C94, C95, C98, C101-C103, C105, C106, C111, C112, C115-C119, C122, C125	66
18	CAPACITOR-0.22UF, 16V, Y5V_805	NEWARK - 52F022	C60, C79, C81	3
19	CAPACITOR-1000PF, 50V, X7R_805	NEWARK - 499-201	C36, C45-C47, C71, C110, C114	7
20	CAPACITOR-10PF, 50V, NPO_805	NEWARK – 499-158	C66, C93, C97, C99, C100	5
21	CAPACITOR-10UF, 6.3V, TANT TE	DIGI-KEY - PCS1106CT-ND	C29, C32, C57, C62, C74, C75, C83, C85, C89, C96, C121, C124	12
22	CAPACITOR-3PF, 50V, NPO_805	DIGI-KEY - PCC030CNCT-ND	C67	1
23	CAPACITOR-68UF, 6.3V, TANT TEH	DIGI-KEY - PCT1686CT-ND	C120, C123	2

NO.	Description	Part Number	Reference Description	Qty
24	CAPACITOR-82PF, 50V, NPO_805	DIGI-KEY - PCC820CGCT-ND	C70, C109, C113	3
25	CONN160_MALE_71624-2000-BASE	51-24-1040	U1, U6	2
26	DIODEZENER_SMD-4.7V, 1W	DIGI-KEY - ZM4732ACT-ND	D5	1
27	DIODEZENER_SMD-6.2V, 1W	DIGI-KEY - ZM4735ACT-ND	D4	1
28	FUSE__SMD-1.500A, NANO	DIGIKEY -- F1144TR-ND	F1	1
29	FUSE__SMD-2.500A, NANO	DIGIKEY -- F1146TR-ND	F2	1
30	HEADER2_100 MIL-BASE	DIGI-KEY S1011-36-ND	J3	1
31	HEADER2_JUMPER-BASE	DIGI-KEY S1011-36-ND	JP1	1
32	HEADER_10X2-BASE	DIGI-KEY S2012-36-ND	J2	1
33	INDUCTOR-FAIR RITE	FAIR RITE 2743019447	L1, L2, L4, L5, L8-L15, L20-L22	15
34	INDUCTOR-470NH, , PANASONIC	DIGI-KEY PCD1216CT-ND	L6, L16, L18	3
35	INDUCTOR-6.8UH, , PANASONIC	DIGI-KEY – PCD1071CT-ND	L7, L17, L19	3
36	INDUCTOR-FB, 133_100MHZ, FAIR RIA	FAIR RITE - 2743002112	L3	1
37	LED-RED, PCB RIGHT ANGLE	DIGI-KEY - LU20091-ND	D1, D2	2
38	LED10-RED, 25MA, 2.1V	DIGI-KEY - LT1066-ND	U7	1
39	MOLEX_8981_4R-BASE	MOLEX 8981_4R	J1	1
40	MRT_PLCC-BASE	TXC-02050-AIPL	U28	1
41	OSC_TTL_DIP-34.368MHZ, 25 PPM	MMD Components MA025H-34.368MHZ	Y3	1
42	OSC_TTL_DIP-44.736MHZ, 20 PPM	MMD Components MA020H-44.736MHZ	Y2	1
43	OSC_TTL_DIP-50.0000MHZ, 100 PPM	MMD Components MA100H-50.000MHZ	Y1	1
44	OSC_TTL_DIP-6.312MHZ , 25 PPM	MMD Components MA025H-6.312MHZ	Y4	1
45	Push Button Normally Open-BASE	DIGIKEY - CKN4002-ND	SW2	1
46	PE65969-BASE	PE65969	T1-T6	6
47	PI5C16212	Pericom PI5C16212A	U3, U4, U15, U17, U18	5
48	RESISTOR-1.0K, 5%, 805	DIGI-KEY - P1,0KACT-ND	R59, R70, R71, R75, R99-R102	8

NO.	Description	Part Number	Reference Description	Qty
49	RESISTOR-100, 5%, 805	DIGI-KEY - P100ACT-ND	R34	1
50	RESISTOR-100K, 1%, 805	DIGI-KEY - P100KCCT-ND	R57, R79, R81	3
51	RESISTOR-10K, 5%, 805	DIGI-KEY - P10KACT-ND	R10	1
52	RESISTOR-270, 5%, 805	DIGI-KEY - P270ACT-ND	R23	1
53	RESISTOR-120,5%,805	DIGI-KEY - P120ACT-ND	R15,R18	2
54	RESISTOR-180,5%,805	DIGI-KEY - P180ACT-ND	R14,R17	2
55	RESISTOR-301, 1%, 805	DIGI-KEY -- P301CCT-ND	R92, R94	2
56	RESISTOR-36, 5%, 805	DIGI-KEY - P36ACT-ND	R67, R68	2
57	RESISTOR-51,5%,805	DIGI-KEY - P51ACT-ND	R19,R21,R22, R24-R33, R35-R43,R83, R104, R111, R151-R153	28
58	RESISTOR-4.7K, 5%, 805	DIGI-KEY - P4.7KACT-ND	R1, R3-R6, R11-R13, R49, R61, R87-R90, R103, R108-R110, R134-R140, R142-R150, R180-R182	37
59	RESISTOR-422, 1%, 805	DIGI-KEY - P422CCT-ND	R62, R91, R93	3
60	RESISTOR-470, 5%, 805	DIGI-KEY - P470ACT-ND	R65	1
61	RESISTOR-5.23K, 1%, 805	DIGI-KEY - P5.23KCCT-ND	R84, R86	2
62	RESISTOR-6.04K, 1%, 805	DIGI-KEY -- P6.04KCCT-ND	R58, R80, R82	3
63	RESISTOR-604, 1%, 805	DIGI-KEY - P604CCT-ND	R64	1
64	RESISTOR-6K81, 1%, 805	DIGI-KEY -- P6.81KCCT-ND	R60	1
65	RESISTOR-75, 5%, 805	DIGI-KEY - P75ACT-ND	R2,R7-R9,R16, R20,R44-R48, R50-R56,R63, R72-R74, R76-R78,R85, R112-R117,R162, R163,R176	35
66	RESISTOR-75.0, 1%, 805	DIGI-KEY -- P75.0CCT-ND	R66, R69, R95-R98	6
67	RES_ARRAY_15_SMD-10K	DIGI-KEY -- 766-161-R10KND	RN1, RN2	2
68	RES_ARRAY_8_SMD-270	DIGI-KEY -- 766-163-R270-ND	RN4	1
69	RES_ARRAY_8_SMD-4.7K	DIGI-KEY -- 766-163-R4.7K-ND	RN3	1
70	RES_ARRAY_8_SMD-68	DIGI-KEY-- 66-163-R68-ND	RN17-RN20	4
71	SUNI_QJET_SBGA-BASE	PM7346	U14	1
72	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP1-TP9, TP87-TP95	18
73	WB1010-BASE	Coilcraft WB1010SM	U23, U32	2

10 SCHEMATICS

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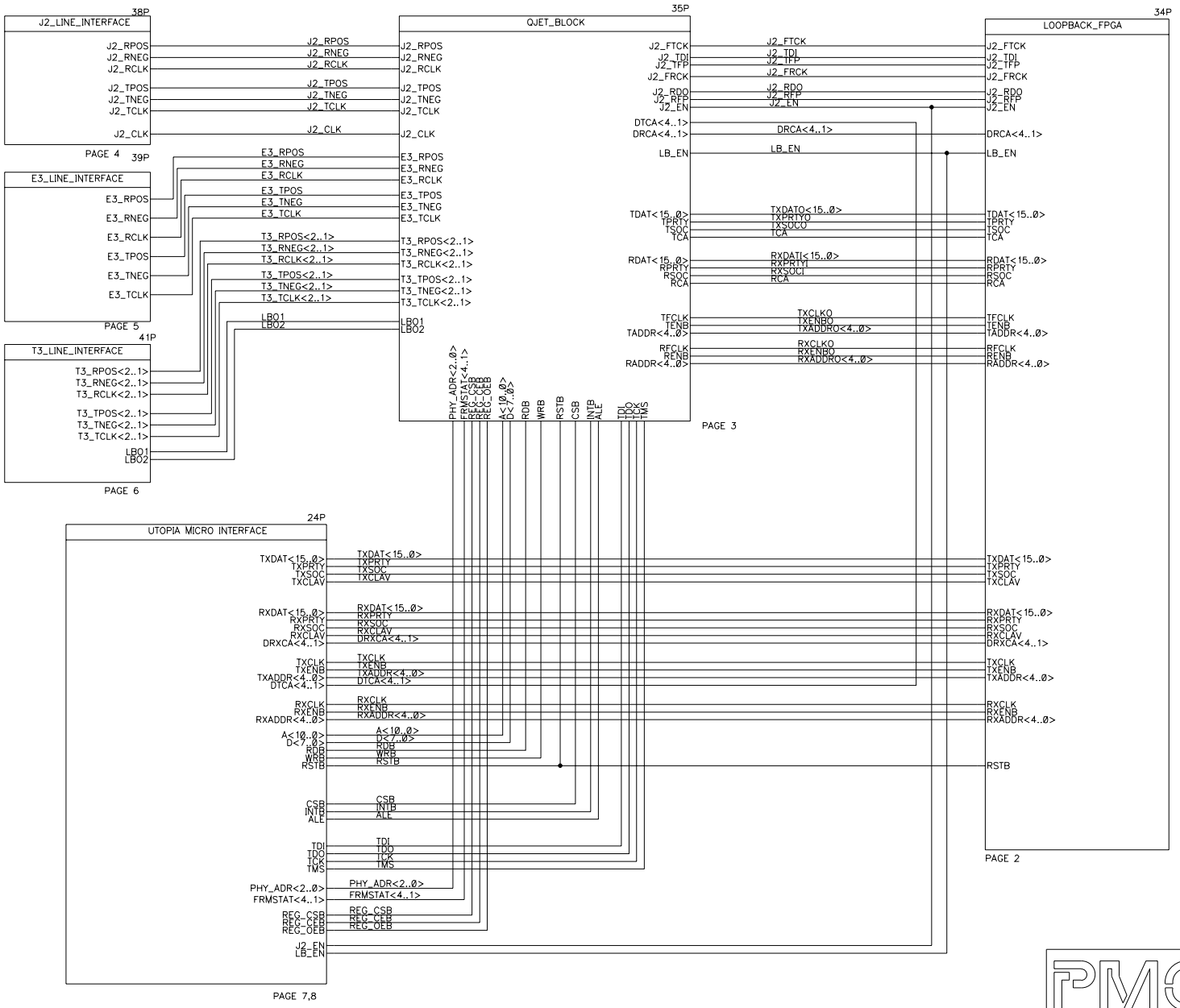

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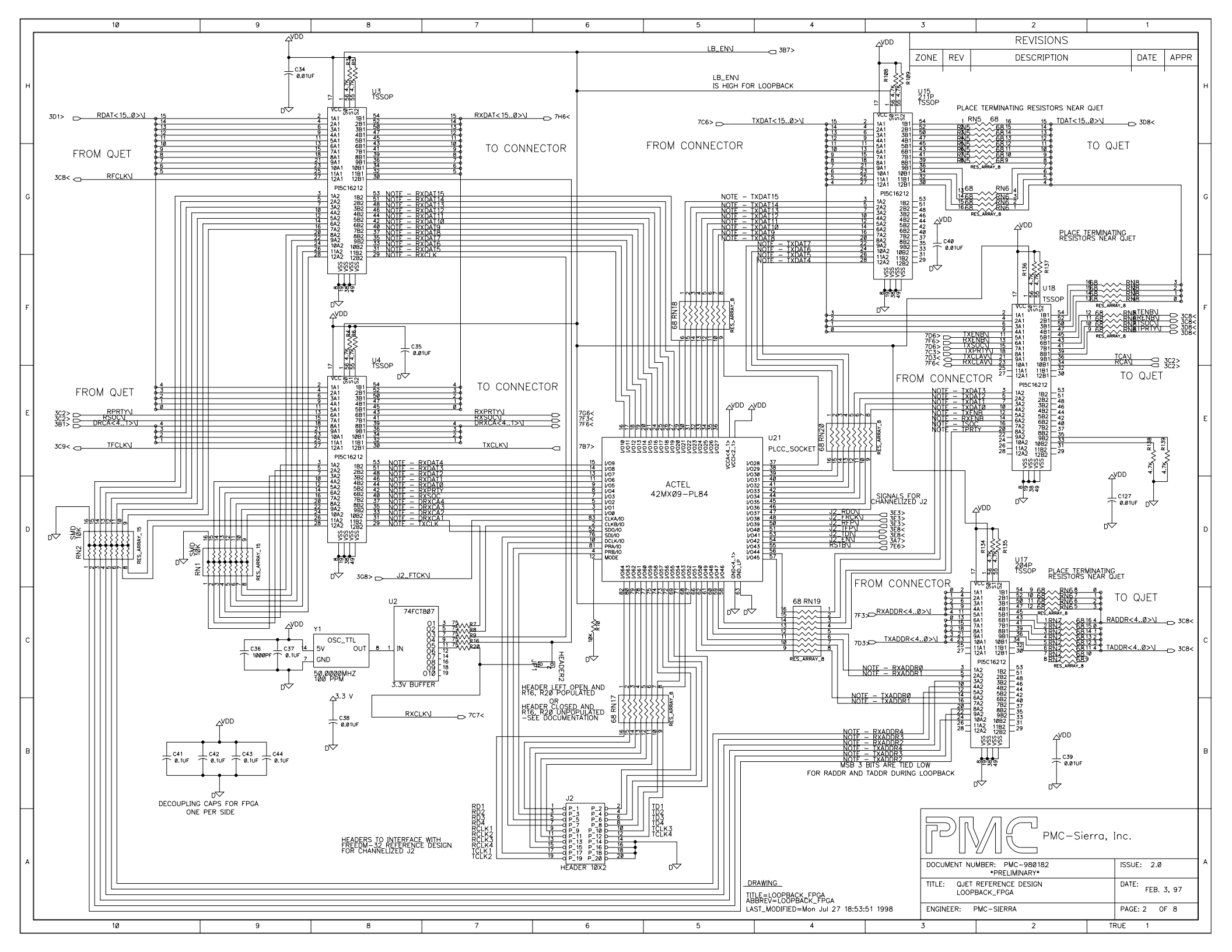
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LB_ENV
IS HIGH FOR LOOPBACK
FROM QJET
TO CONNECTOR
FROM CONNECTOR
TO QJET
PLACE TERMINATING RESISTORS NEAR QJET
ACTEL
42MX09-PL84
PLCC_SOCKET
SIGNALS FOR CHANNELIZED J2
OSC_TTL
50.0000MHZ
100 PPM
74FCT807
3.3V BUFFER
HEADER LEFT OPEN AND
R16, R20 POPULATED
OR
HEADER CLOSED AND
R16, R20 UNPOPULATED
-SEE DOCUMENTATION
DECOUPLING CAPS FOR FPGA
ONE PER SIDE
HEADERS TO INTERFACE WITH
FREEDM-32 REFERENCE DESIGN
FOR CHANNELIZED J2
HEADER 10X2
MSB 3 BITS ARE TIED LOW
FOR RADDR AND TADDR DURING LOOPBACK
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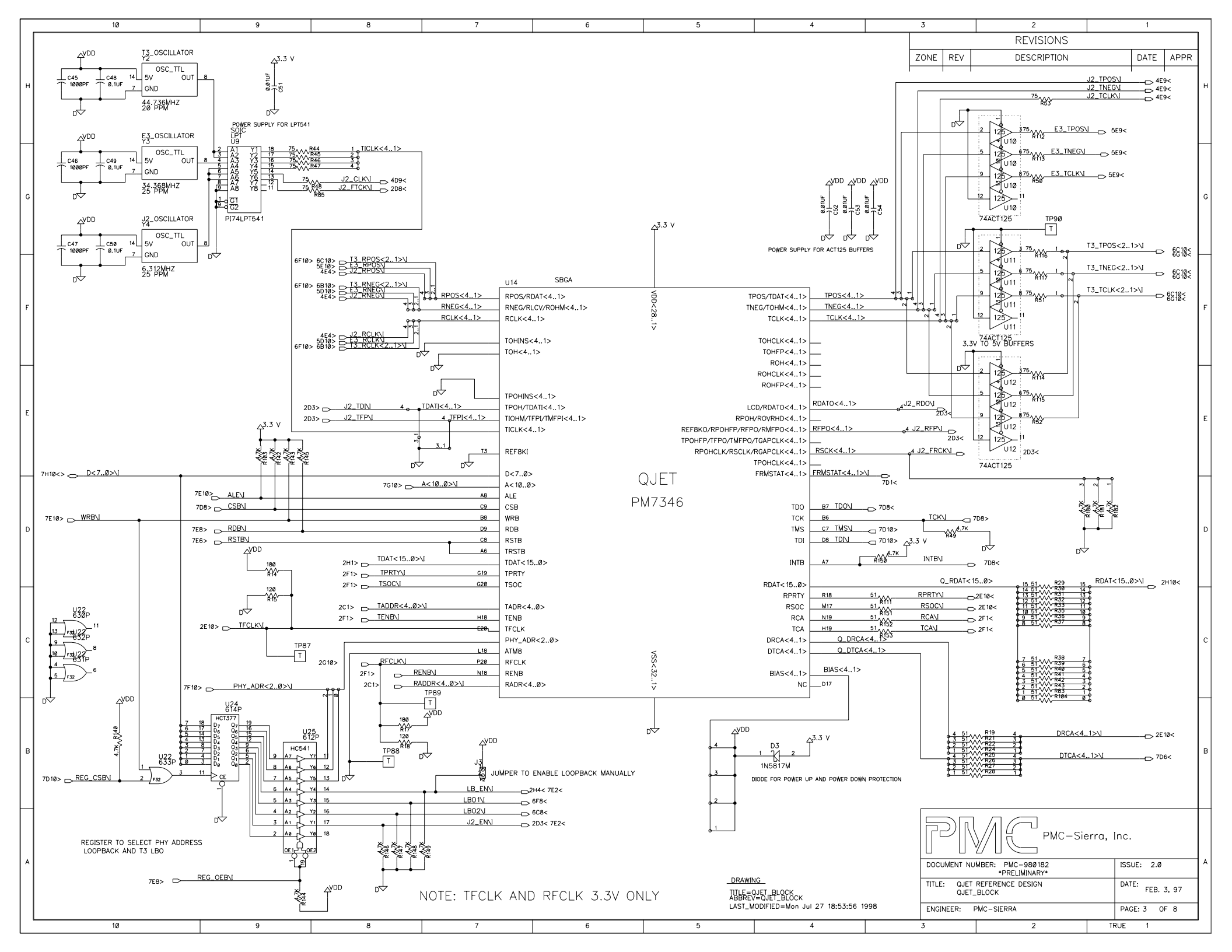
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Y3
34.368MHZ
25 PPM
J2_OSCILLATOR
Y4
6.312MHZ
25 PPM
POWER SUPPLY FOR LPT541
SOIC
LPT
U9
PI74LPT541
POWER SUPPLY FOR ACT125 BUFFERS
74ACT125
3.3V TO 5V BUFFERS
SBGA
U14
QJET
PM7346
JUMPER TO ENABLE LOOPBACK MANUALLY
DIODE FOR POWER UP AND POWER DOWN PROTECTION
REGISTER TO SELECT PHY ADDRESS
LOOPBACK AND T3 LBO
NOTE: TFCLK AND RFCLK 3.3V ONLY
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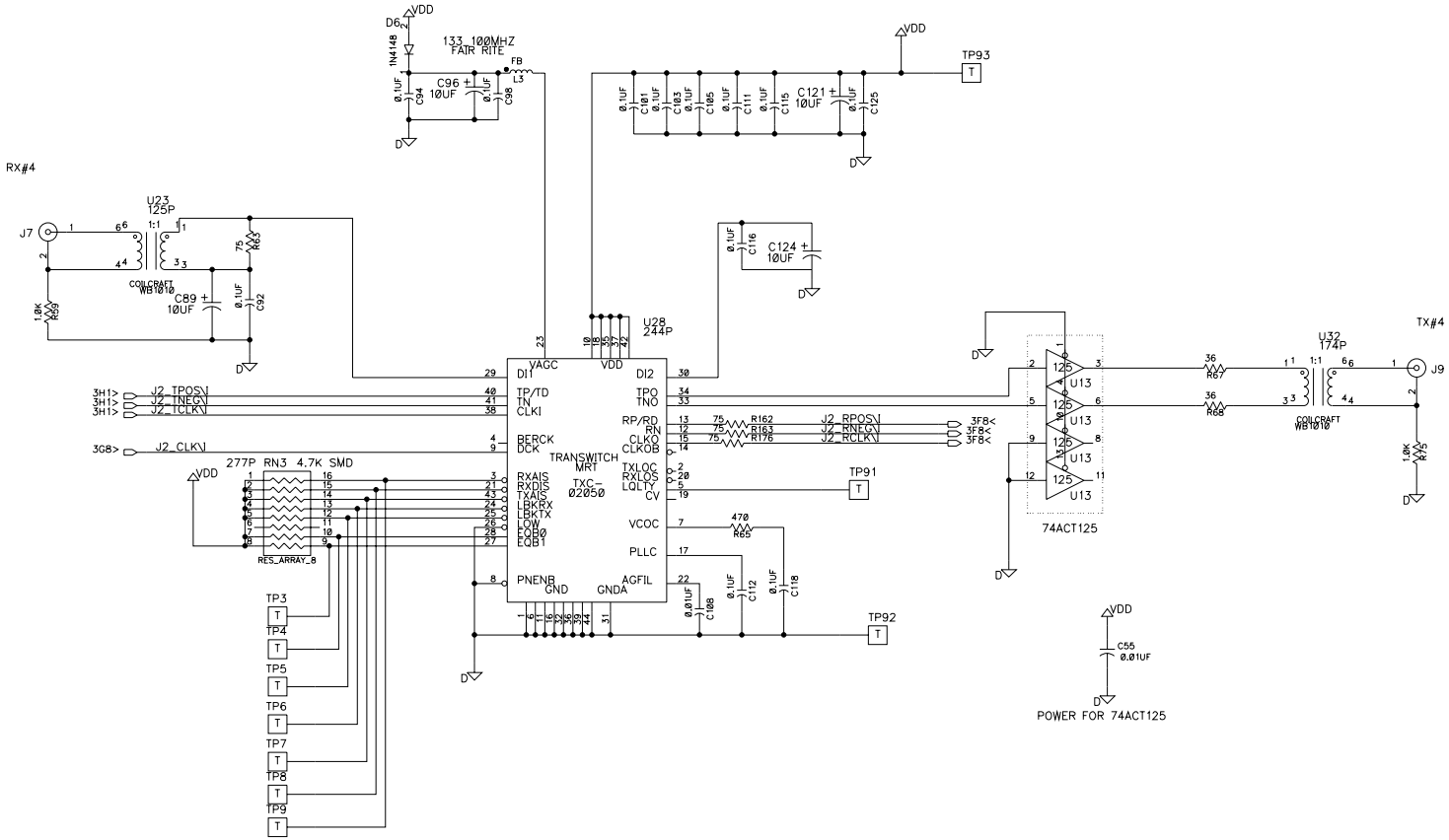

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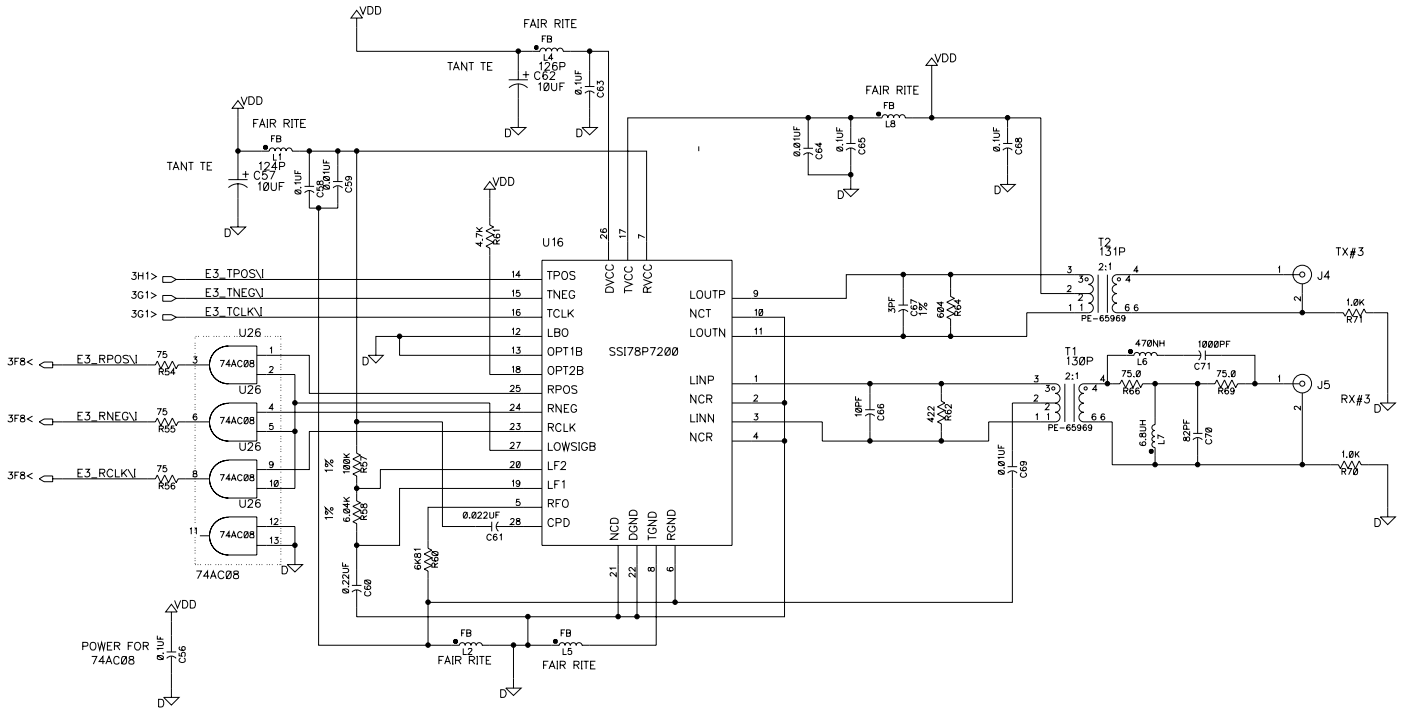
E3_LINE_INTERFACE



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ENGINEER: PMC-SIERRA	PAGE: 5 OF 8

T3 LINE INTERFACE

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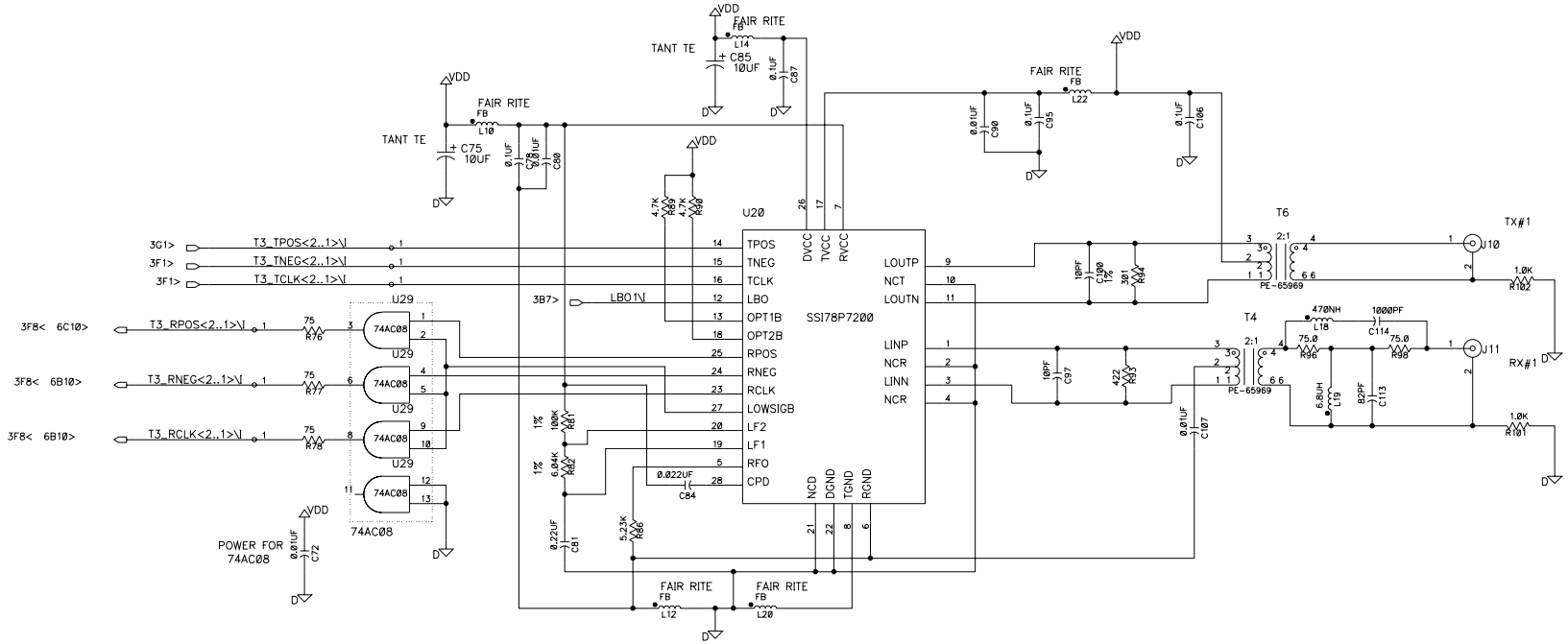

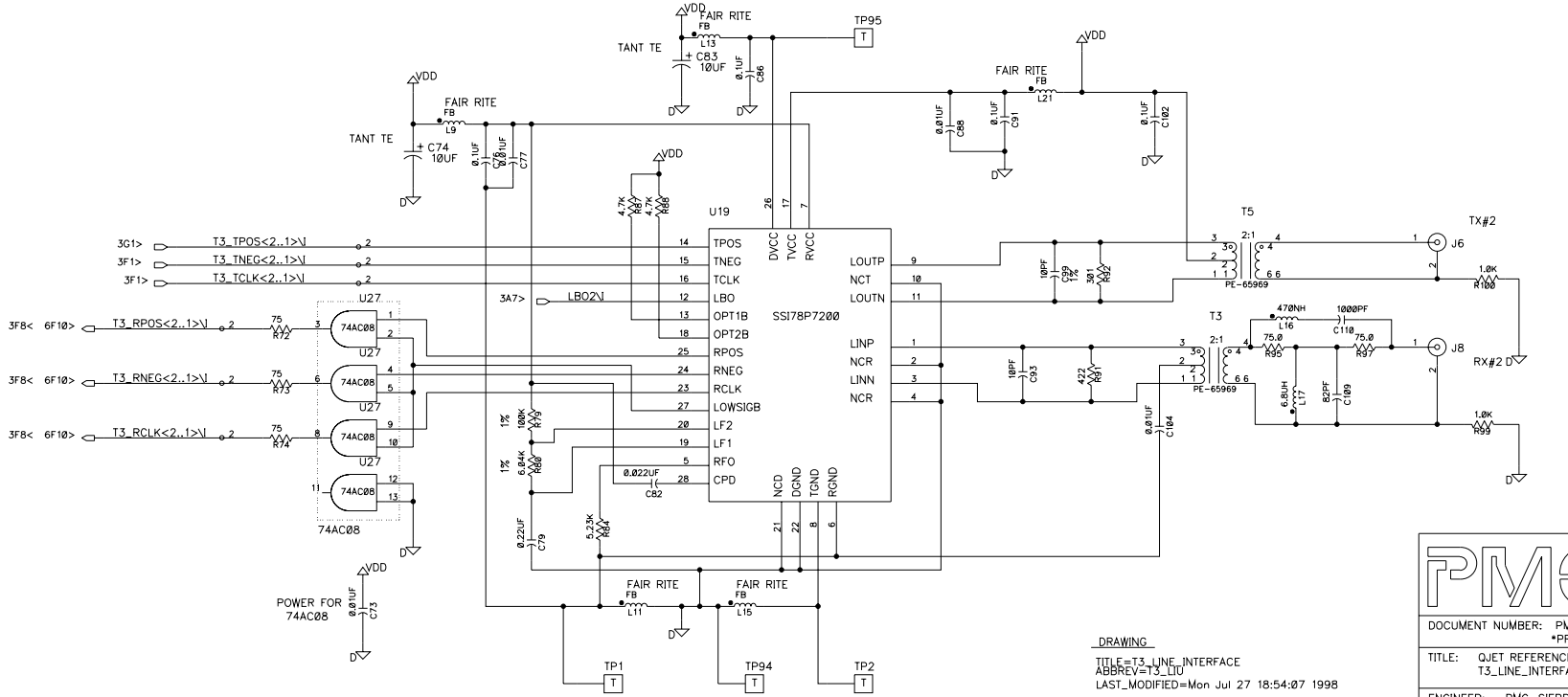

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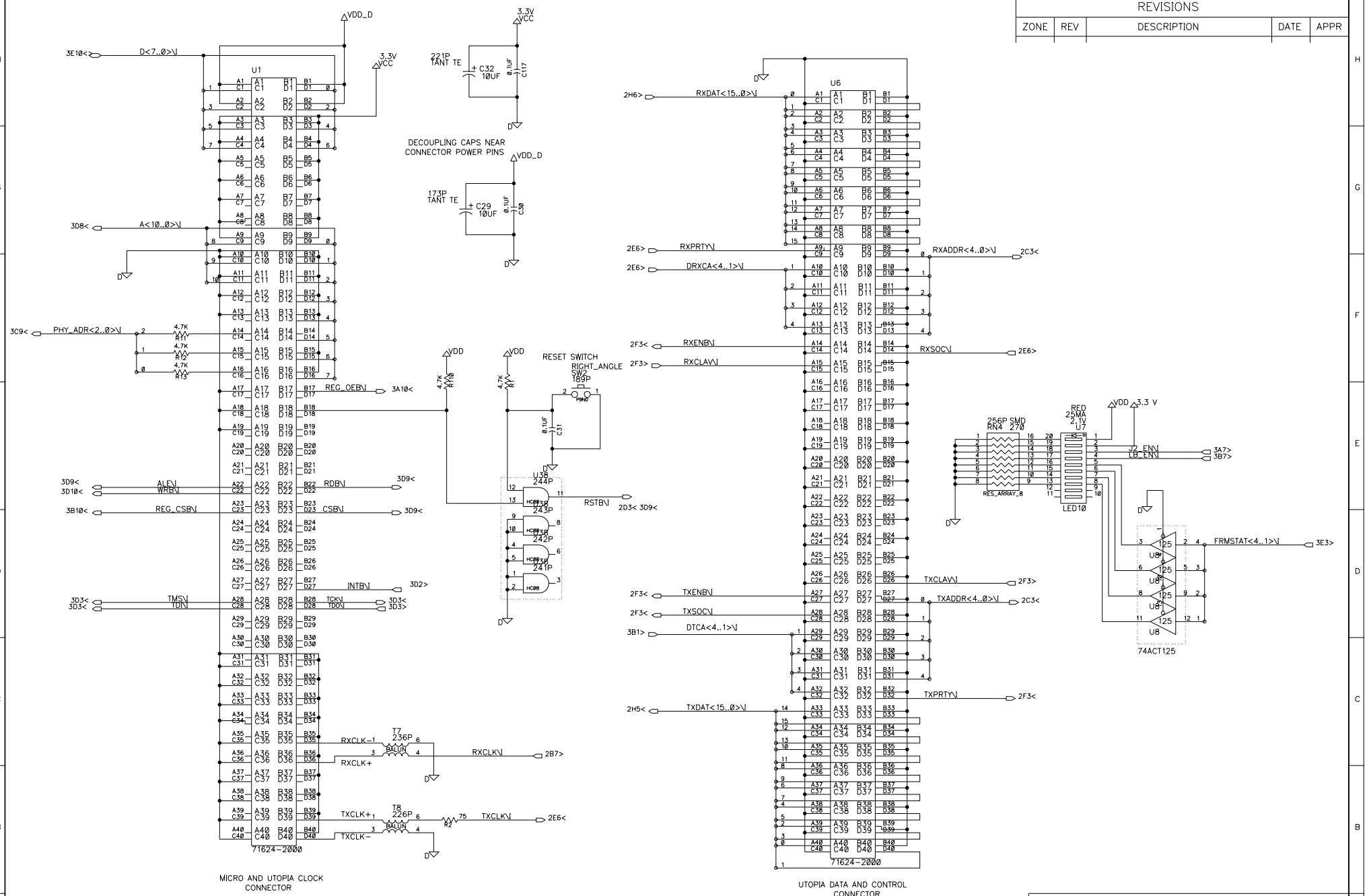

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ENGINEER: PMC-SIERRA	PAGE: 7 OF 8

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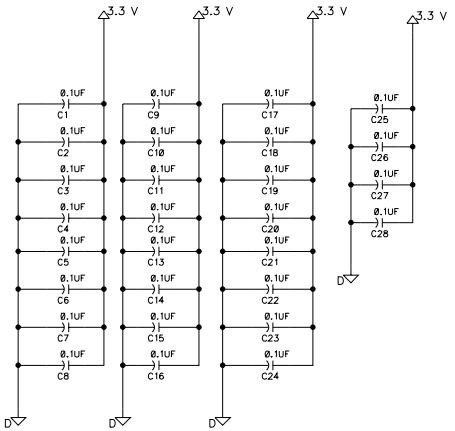
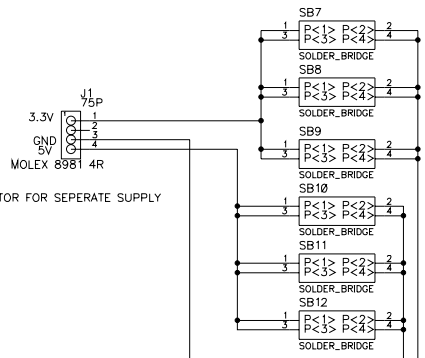
ZONE	REV	DESCRIPTION	DATE	APPR

DECOUPLING CAPS FOR QJET

PLACE ONE CAPACITOR NEAR EACH POWER PIN

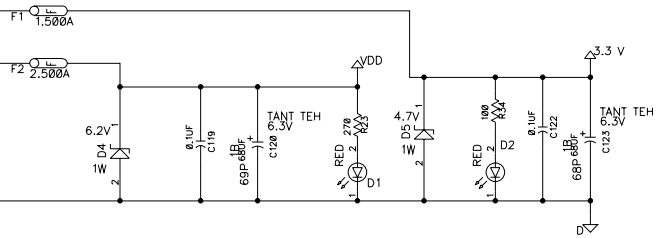


POWER CONNECTOR FOR SEPERATE SUPPLY

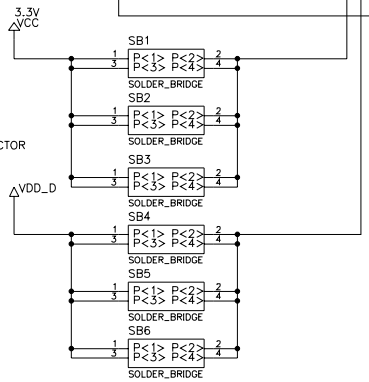


ONLY ONE SET OF SOLDER BRIDGES
CONNECTED AT ANY TIME

POWER COMES FROM EITHER
FOUR PIN CONNECTOR OR
UTOPIA MICRO CONNECTOR



POWER FROM UTOPIA MICRO CONNECTOR



DRAWING

TITLE=UTOPIA_MICRO_INTERFACE
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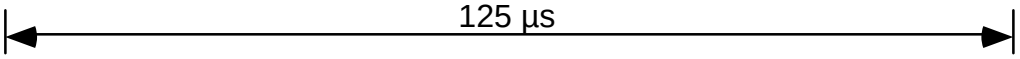
12 APPENDIX A: FRAMING FORMATS

This appendix presents relevant framing formats used in this reference design. The G.704 J2 standard specifies transmission at 6312 kbps with a 789 bit frame structure. The frame is divided into 98 byte time slots with 5 framing bits to end each frame. Four such structures are combined to create a J2 superframe. This structure is illustrated in Figure 4 below.

Figure 4 - J2 Frame Format



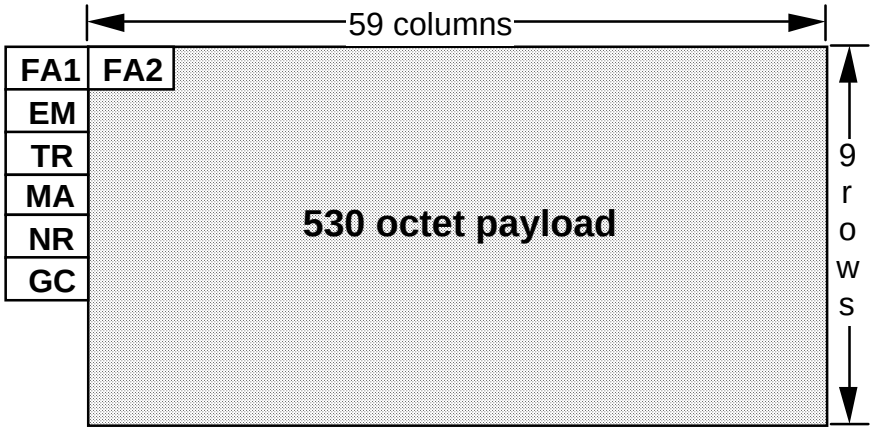
TS 1 - TS96 (96 Octets)	TS97	TS98	1	1	0	0	m
TS 1 - TS96 (96 Octets)	TS97	TS98	1	0	1	0	0
TS 1 - TS96 (96 Octets)	TS97	TS98	x1	x2	x3	a	m
TS 1 - TS96 (96 Octets)	TS97	TS98	e1	e2	e3	e4	e5

The E3 standard specifies a 34.368 Mbit/sec transmission rate. Both the G.751 and G.832 E3 specifications for frame formats are supported by the S/UNI-QJET. These frame formats are shown in Figures 5 and 6 respectively.

Figure 5 - G.751 E3 Frame Format

1	1	1	1	0	1	0	0	0	0	RAI	Na	372 Payload bits
C_{11}	C_{21}	C_{31}	C_{41}	380 Payload bits								
C_{12}	C_{22}	C_{32}	C_{42}	380 Payload bits								
C_{13}	C_{23}	C_{33}	C_{43}	J_1	J_2	J_3	J_4	376 Payload bits				

Figure 6 - G.832 E3 Frame Format



The S/UNI-QJET is also compatible with C-bit parity and M23 DS3 frame formats operating at 44.736 Mbit/sec. Both frame formats use a common structure shown in Figure 7 below, with the differences being in the use of the C overhead bits.

Figure 7 - DS-3 Frame Format

	84 bits	84 bits	84 bits	84 bits	84 bits	84 bits	84 bits	84 bits
M-subframe 1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4

NOTES

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