PM4351

COMET REV. E AND REV. F

DEVICE ERRATA

RELEASED

ISSUE 12: OCTOBER 2000

REVISION HISTORY

Issue No.	Issue Date	ECN #	Details of Change
1	September 1, 1998		Notification of additional information and errors to COMET Data Sheet Issue P4.
2	September 25, 1998		Update to Notification of additional information and errors to COMET Data Sheet Issue P4.
3	December 14, 1998		Update to Notification of additional information and errors to COMET Data Sheet Issue P5.
4	March 9, 1999	1628	Update to Notification of additional information and errors to COMET Data Sheet Issue P6.
5	March 19, 1999	1640	Add 62411 TX program files that will be included in COMET Data Sheet Issue P7.
6	April 27, 1999	1676	Corrects termination resistor value, adds optimized E1 75 ohm TX program files and limits N*DS0 PRBS usage that will be included in COMET Data Sheet Issue P7.
7	May 10, 1999	1710	Notification of additional information and errors to COMET Data Sheet Issue P7.
8	July 9, 1999	1820	Notification of additional information and errors to COMET Data Sheet Issue P8
9	September 17, 1999	1940	Errata updated to reflect PM4351-NI Release to Production
10	January 15, 2000	2143	Errata updated to reflect issues that have arisen since release to production
11	June, 2000	2620	Errata updated to reflect issues that have arisen since release to production
12	October, 2000	3070	Errata updated to reflect issues that have arisen since release to production

CONTENTS

1 ERRATA SCOPE

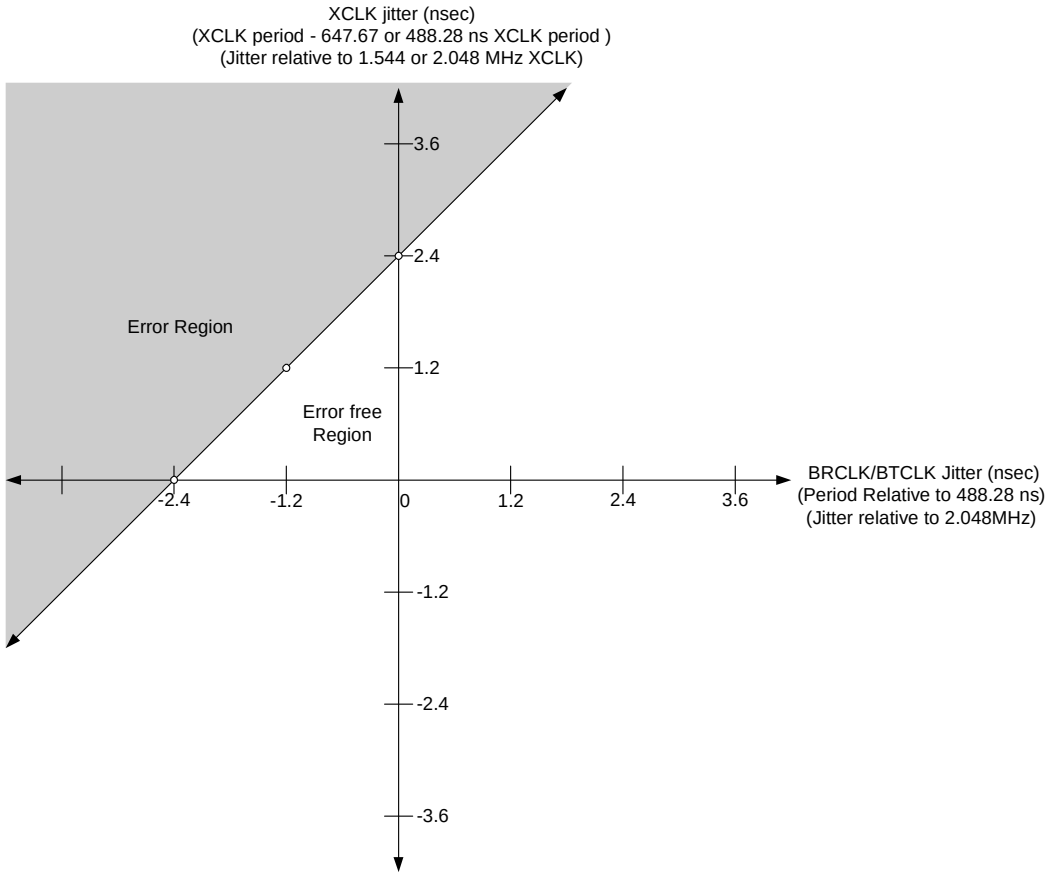
This document is a notification of functional deficiency applied specifically to the Rev. E and Rev. F of the PM4351 COMET. The letters “E” and “F” contained within the respective lot numbers can identify Rev E devices and Rev F devices. The following information was complete as of October 2000.

For documentation notification of additional information and errors for the current issue of the COMET Datasheet (PMC-970624), please refer to the COMET Device Errata (PMC-2001577)

2 COMET FUNCTIONAL DEFICIENCIES

2.1 T1 mode with a 2.048 MHz or greater backplane slave clock

When the COMET is configured for T1 mode with a slaved clock backplane (BRCLK or BTCLK are inputs) with a 2.048 MHz or greater backplane rate, the data and signaling information may be corrupted if the BRCLK, BTCLK, and XCLK jitter (defined as instantaneous worse case period) is not tightly controlled. The following diagram shows the error and error-free operating regions when in the presence BRCLK/BTCLK and XCLK jitter.



The BRCLK/BTCLK jitter is described as the worst case instantaneous peak jitter relative to a jitter-free BRCLK/BTCLK. The XCLK jitter is described as the worst case instantaneous peak jitter relative to a jitter-free XCLK. The jitter for both XCLK and BRCLK/BTCLK are described as positive and negative peak jitter in nanoseconds (ns). Positive peak jitter increases the instantaneous period while negative peak jitter shortens the instantaneous period.

Note that BRCLK and BTCLK are inputs (when the COMET is a backplane slave) and can be 1.544, 2.048, 4.096, 8.192, or 16.384 MHz. If the 4.096, 8.192 or 16.384 MHz clocks are used, they are divided down internally by the COMET to become a 2.048 MHz clock. Thus, internally the period of BRCLK/BTCLK is treated as if it were either a 1.544 or 2.048 MHz clock. The above diagram represents the internally divided down BRCLK/BTCLK clocks.

Proper operation is ensured when the worst case instantaneous XCLK jitter minus the worst case instantaneous BRCLK/BTCLK jitter is less than 2.4ns through all valid voltage and temperature range (XCLK jitter – BRCLK/BTCLK jitter < 2.4). The following are example configurations that allow the COMET to operate error free.

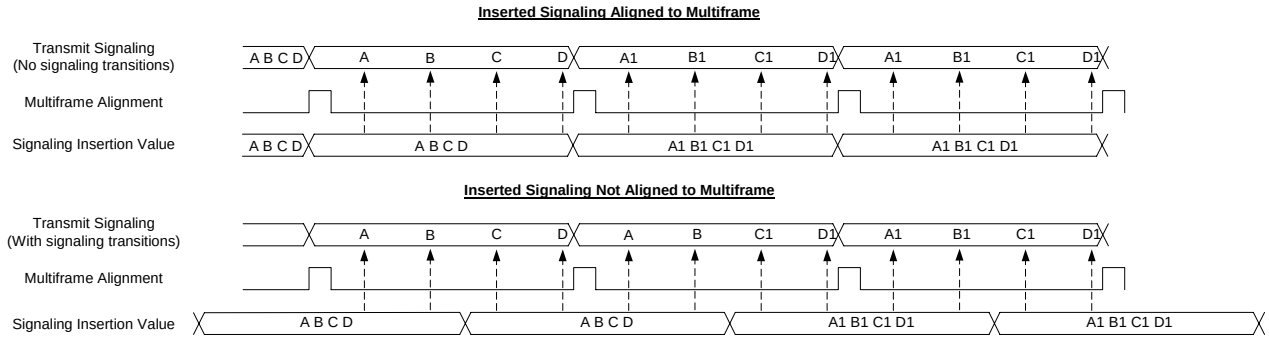
Instantaneous XCLK			Instantaneous BRCLK/BTCLK Range for proper T1 operation		
Frequency[1] (MHz)	Period (ns)	Jitter[2] (ns)	Frequency[3] (MHz)	Allowable Jitter (ns)	Allowable period (ns)
1.544	647.67	+0.6	1.544	> -100	>547.67
1.544	647.67	+0.6	2.048	> -1.8	>486.48
1.544	647.67	-0.6	2.048	> -3	>485.28
2.048	488.28	+0.6	1.544	> -100	>547.67
2.048	488.28	+0.6	2.048	> -1.8	>486.48
2.048	488.28	-0.6	2.048	> -3	>485.28

Notes:
1. The impact of XCLK jitter is relative to 1.544 or 2.048 MHz.
2. Worse case jitter is the sum of the worst case instantaneous jitter plus the worst case parts per million (ppm) drift from the exact 1.544 or 2.048 MHz XCLK.
3. These examples show that clock jitter is not a significant concern with 1.544 MHz backplane.

2.2 Signaling insertion

Signaling insertion could have a transitional state when the signaling state changes.

T1 signaling on the COMET is inserted relative to the multiframe alignment of the transmitted T1 signal. Signaling data is extracted bit by bit from the TPSC indirect register or the BTSIG pin. This means that each of the signaling bits (A, B for SF and A, B, C, and D for ESF) is taken from a different frame relative to the multiframe boundary. If the signaling data on the BTSIG pin (or the TPSC Indirect register) is used to insert signaling, but is not aligned to the multiframe boundary, then transitional signaling states might occur. Signaling data could change from the current signaling state to an intermediate signaling state (for 3ms or one multiframe) before changing to the correct signaling state, as shown below.



When the transmit backplane is configured for basic frame mode, the COMET assumes an arbitrary multiframe alignment. When configured for basic frame alignment, there is no way to align to the internal multiframe. Therefore transitional states for signaling might occur. Hence, it is necessary to configure the backplane for multiframe alignment to ensure signaling insertion occurs without transitional states.

2.3 FPTYP Description

The FPTYP bit in the Register 041H: BTIF Frame Pulse Configuration has limited functionality and the bit description is incorrectly stated.

In the Issue 8 Datasheet, the FPTYP description incorrectly reads, “When operating at T1 in 2MHz backplane mode, the framing pattern can be corrupted

when FPTYP =1. In order to avoid corruption, toggle FPTYP high then low and keep it held low. The transmitter will maintain the multi-frame alignment provided on the BTFP. If BTFP loses multiframe alignment, FPTYP will have to be toggled again."

The following description corrects the description of the FPTYP bit:

"The COMET will not operate correctly when the backplane is configured for T1 ESF mode with 2.048Mbit/s or greater backplane with master multiframe pulse (FMODE = 0 and FPTYP = 1). Slave mode (FMODE =1) should be used.

When operating at T1 ESF in 2.048 Mbit/s or greater backplane mode with slave multiframe pulse (FMODE =1), the framing pattern can be corrupted when FPTYP =1. In order to avoid corruption, toggle FPTYP high and then low within 2ms (16 frames) after the last BTFP active edge. Then keep FPTYP held low. This allows the COMET's internal multiframe alignment to synchronize with the BTFP multiframe pulse input. The transmitter will maintain the last multi-frame alignment captured from the BTFP input. If BTFP loses multiframe alignment, FPTYP will have to be toggled again."

Failure to implement the corrected workaround stated above results in the transmitted multiframe boundary to be different than that indicated by the BTFP input. This could cause signaling transitional state corruption (as discussed in Errata item 2.2) and, Facility Data Link, CRC and F-bit misalignment when framing and signaling is taken from backplane data (BTPCM). The Facility Data Link, CRC and F-bit will not be misaligned when generated internally by the COMET.

2.4 PRBS Functionality

There is a limitation in the usage of the COMET's PRBS functionality when using the PM4351-RI Rev E devices. When using PRBS in any mode, the receive elastic store has to be bypassed. This can be done by setting the RXELSTBYP bit in the receive options register, 002H, to logic 1.

The receive elastic store does not have to be bypassed when using PRBS in the PM4351-RI Rev F devices.

2.5 Forcing RSTB Low upon Power-Up

Table 8 of the PMC-970624 COMET Datasheet states that the RSTB should be asserted for at least 100ns to perform a reset. It also states that CSB must go high at least once after power up to clear internal test modes. This needs further clarification.

Allowing the COMET to power up in a random test mode configuration has the very low but non-zero probability that a fuse blowing test mode configuration could be accidentally enabled, thereby permanently altering the COMET analog pulse mask. To avoid this it is recommended that RSTB be asserted (held low) during power up and held for at least 100 ns after VDDO has stabilized. CSB should be pulsed high at least once after the power up sequence has been completed in order to set test mode into a known state.

The power up sequence should be followed as defined in note 6 of the “Notes on pin descriptions” section (just below Table 11 in the data sheet). During power up the restriction on input pin voltage defined in Section 15 - Absolute Maximum Ratings should be maintained. Note that the voltage on Any Pin is restricted to be from -0.3V to BIAS+0.3V.

2.6 Duplication of APRM Messages

Triggering a manual performance report generation can intermittently cause a duplication of the 13-byte performance report. This is caused by the manual generation of the report not setting the FIFO empty bit high after reading the message. This is not an issue when setting the COMET device to generate the performance report automatically, which is its normal operational mode.

2.7 Use of the HDLC Controller in E1 mode

When using the internal HDLC controllers in E1 mode there are some restrictions to be aware of:

- If the internal HDLC controller (TDPR) is used to insert data into a timeslot and the previous timeslot has an idle code byte inserted from the TPSC, the last two bits of the idle code can be corrupted. This means that if timeslot 4 has data inserted from the HDLC controller, and an idle code has been inserted in timeslot 3 from the TPSC, the least significant two bits of timeslot 3 can be corrupted. It is recommended that HDLC traffic be inserted from the backplane rather than the internal controller if idle codes are being transmitted in the preceding timeslot. Alternatively, the HDLC Controller can be used if idle codes are inserted externally.

- If data is inserted into timeslot 1 from the internal HDLC controller, the least significant bit in timeslot 0 in the NFAS frames (i.e., Sa8) can be corrupted if Sa8 is configured to be inserted from the backplane. The Sa8 bit will not be corrupted when insertion is done via COMET’s E1-TRAN National Bits Codeword register. Using the internal HDLC Controller for timeslot one is not recommended.

- In normal operation, if a timeslot is configured for both HDLC transmission and idle code insertion, the HDLC data is supposed to be transmitted and the idle code ignored. When configured in this mode, it is possible for the COMET to corrupt the last two bits of the HDLC data. To get around this, simply disable idle code insertion for timeslots that transmit HDLC data.

- When the internal HDLC controller (TDPR) is used to insert HDLC data on the Sa8, Sa7, Sa6 or Sa5 bit, the more significant bit next to it (taken from the backplane) can be corrupted. For example, if HDLC data is inserted into Sa7, then Sa6 can be corrupted. National Use Bits inserted internally from the E1-TRAN block are always inserted correctly.

- Inserting HDLC data into the Si bit in TS0 (i.e., the international bit) can cause the least significant two bits of an IDLE code in TS31 to be corrupted.

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PMC-1980578 (R12) ref PMC-970624 (R8) Issue date: October 2000