PM73121

EIGHT LINK CIRCUIT EMULATION SERVICE ON A CHIP

REVISION A DEVICE ERRATA

ISSUE 3: FEBRUARY 1999

CONTENTS

1 FEATURES

This document is the Device Errata Sheet for the Revision A of PM73121.

1.1 Device Identification

This document applies only to Revision A of the PM73121. As illustrated in Figure 1.1, the Revision Code is marked on the face of the device. The PM73121 Revision A is in a 240-pin PQFP package.

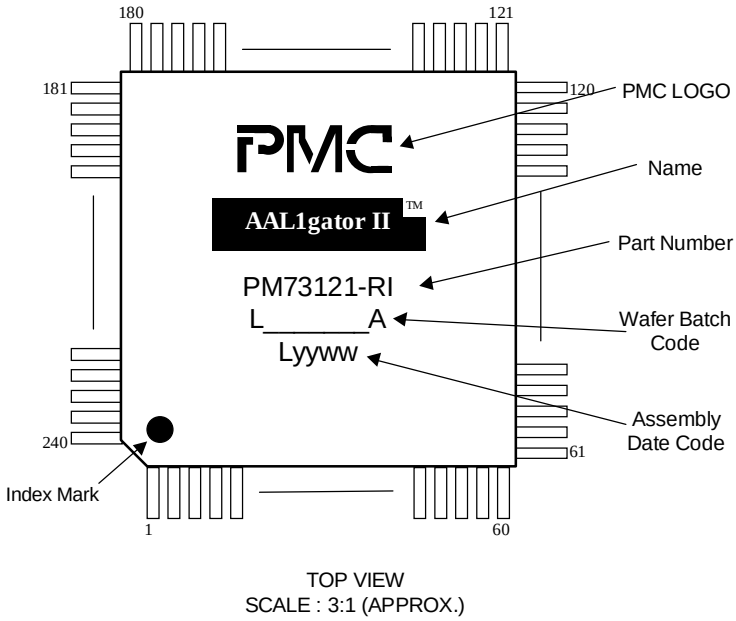

Figure 1.1: PM73121-RI Branding Format.

1.2 References

1. PMC-980620, AAL1 SAR Processor Long Form Datasheet, Issue 3 (January 1999).

2 FUNCTIONAL DEFICIENCY LIST

This section describes the known functional deficiencies associated with Revision A of the PM73121, as of the publication date of this document. For each deficiency, the known work-around is also described.

Please report any functional deficiencies not covered in this document to PMC-Sierra, Inc.

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2.1 Does Not Always Generate a Zero Pointer When Starting a Queue in SDF-MF Mode

Description

In SDF-MF mode, the AAL1gator II does not conform with the following text contained in ITU-T Recommendation I.363.1:

> "… the first structured block to be transmitted after the AAL connection is established uses the P format with sequence count value in the SAR-PDU header equal to 0 and with the first octet of the structured data placed in the second octet of the SAR-PDU payload."

Specifically, the start of the structure may not occur in the second octet of the SAR-PDU payload in SDF-MF mode.

The AAL1gator II begins sending a cell in the frame in which it is scheduled. Since this frame may or may not be the start of a multiframe, the first byte may or may not be the first byte of a new structure.

The pointer will point to wherever the structure begins.

The initial (first) pointer generated in SDF-MF mode is deterministic and can be calculated from the following expressions:

Let X =

Remainder(FRAMES_PER_CELL ÷ MF_SIZE) × NUM_CHAN + SIG_BYTES

where:

MF_SIZE (for E1) = 16
MF_SIZE (for T1) = 24
SIG_BYTES = the number of signaling bytes in the structure

NOTE: If the remainder is 0, then SIG_BYTES should be ignored and the initial pointer is 0.

For full cells:

```
if X ≤ 93 then
     initial pointer = X
else
     first cell built(sn = 0) will not contain a pointer.
     initial pointer will be in 3rd cell built (sn = 2).
     initial pointer = X - (47 × 2)
     ((47 × 2) accounts for the bytes in the first two cells.)
endif
```

For partial cells:

```
if X ≤ BYTES_PER_CELL then
     initial pointer = X
elseif BYTES_PER_CELL < X ≤(2 × BYTES_PER_CELL) then
     initial pointer = 46 + (X - BYTES_PER_CELL)
else
     initial pointer will be in sn = 2 cell (3rd cell built).
     initial pointer = X - (2 × BYTES_PER_CELL)
endif
```

Work Around

This non-conformance is not known to cause any incompatibility problems. No work-around is necessary. Typically, robust AAL1 cell receivers can tolerate pointers of any value if the initial pointer is lost in the network.

You can also force initial multiframe alignment, and an initial pointer of 0 by increasing the FRAMES_PER_CELL value for the queue so it falls on a multiframe boundary in the transmitter data buffer.

Since FRAMES_PER_CELL controls how far back in time data is read, delay increases if FRAMES_PER_CELL increases. The increase will be 125 µs for each frame added.

For example, for an E1 line with 32 channels allocated, fully filled cells, the initial pointer will be:

X = Remainder (3 ÷16) × 32 + 16 = 112.

Since X > 93, the initial pointer = X - (47 × 2) = 18.

Since all queues are added in frame 0 of multiframe 0, the TALP starts building the cell FRAMES_PER_CELL = 3 frames back in the transmit buffer from frame 0 in multiframe. To generate an initial pointer of 0, the TALP must start building the cell on a multiframe boundary (for example, multiframe × frame 0). This can be accomplished by increasing FRAMES_PER_CELL to 16. For T1, with its 24 channels, FRAMES_PER_CELL should be increased to 24 to generate an initial pointer of 0.

Figure 1 shows the transmit data organization for E1 and Figure 2 shows the transmit data organization for T1.

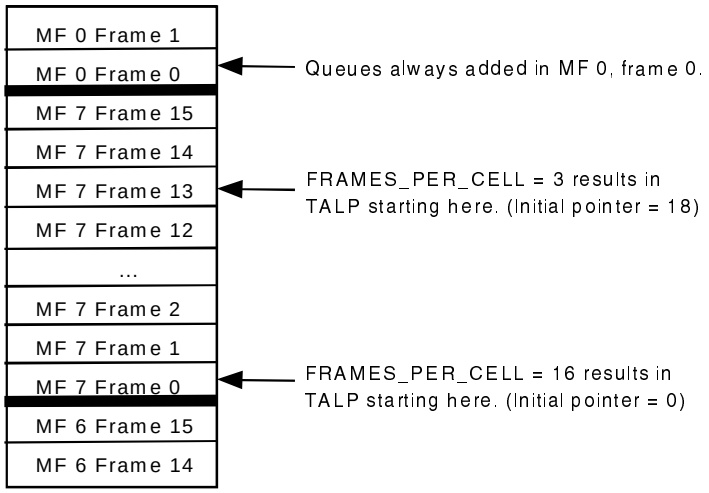

Figure 1: Transmit Data Buffer Organization for E1

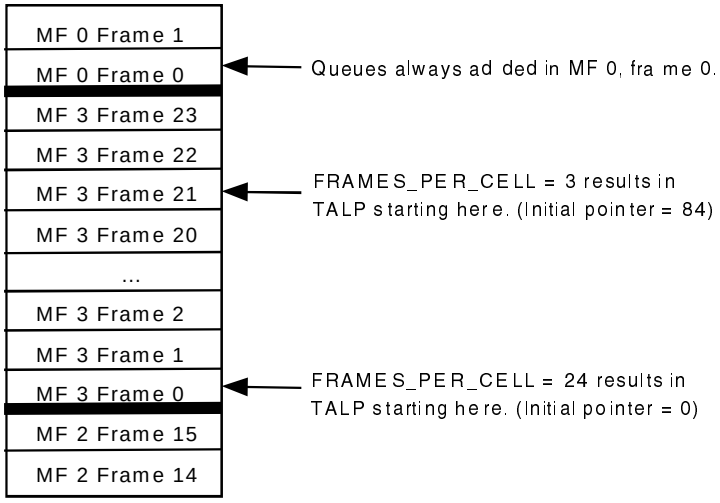

Figure 2: Transmit Data Buffer Organization for T1

Table 1 shows the initial (first) pointer value generated in SDF-MF mode and the specific value required to generate an initial pointer of 0 for full cells.

Table 1: Initial Pointer for Full Cell Situations

NUM_CHAN	FRAMES_ PER_CELL	SIG_BYTES	1st Pointer (E1)	1st Pointer (T1)	Frames per Cell For 1st Pointer = 0 (for E1)	Frames per Cell for 1st Pointer = 0 (for T1)
1	48	1	0	0	n/a	n/a
2	25	1	19	3	32	48
3	17	2	5	53	32	24
4	13	2	54	54	16	24
5	11	3	58	58	16	24
6	9	3	57	57	16	24
7	8	4	60	60	16	24
8	7	4	60	60	16	24
9	7	5	68	68	16	24
10	6	5	65	65	16	24
11	6	6	72	72	16	24
12	5	6	66	66	16	24
13	5	7	72	72	16	24
14	5	7	77	77	16	24
15	5	8	83	83	16	24
16	4	8	72	72	16	24
17	4	9	77	77	16	24
18	4	9	81	81	16	24
19	4	10	86	86	16	24
20	4	10	90	90	16	24
21	4	11	1*	1*	16	24
22	4	11	5*	5*	16	24
23	4	12	10*	10*	16	24
24	3	12	84	84	16	24
25	3	13	88	n/a	16	n/a
26	3	13	91	n/a	16	n/a
27	3	14	1*	n/a	16	n/a
28	3	14	4*	n/a	16	n/a
29	3	15	8*	n/a	16	n/a
30	3	15	11*	n/a	16	n/a
31	3	16	15*	n/a	16	n/a
32	3	16	18*	n/a	16	n/a
NOTE* indicates the pointer is in sn = 2.						

2.2 Data Cells May Be Dropped When OAM Cells Are Generated

Description

If the transmit UTOPIA FIFO fills up due to backpressure on the UTOPIA bus and the last cell written into the FIFO is an OAM cell and another cell request is pending, the pending cell will be dropped. This situation can occur only if an OAM cell fills the FIFO and a cell request is pending as the last byte of the OAM cell is being written into the FIFO. Symptoms of this problem will be SN errors and lost cells detected on the remote end. Since OAM cells are sent at a low rate (usually one per second), the error rate caused by this problem will be quite low. SN processing should minimize the impact of this problem.

Work Around

Two solutions to this problem are: 1) minimize backpressure on the transmit UTOPIA port, or 2) generate OAM cells by some other means.

1. The UTOPIA bus has a 2-cell FIFO. The shortest amount of time that an OAM could be written into the FIFO is 139 SYS_CLK cycles (3.6 µs if SYS_CLK = 38.88 MHz). Therefore, the first cell in the FIFO needs to be written out within 3.6 µs to guarantee the FIFO will not fill up. With no backpressure (/TATM_FULL always high) and a 25 MHz UTOPIA clock rate, it takes 2.1 µs to write out a cell. Therefore, the worst-case backpressure per cell must be less than 1.5 µs.

NOTE: As more lines and queues are added, the time it takes to build an OAM cell increases, since it takes more time to access the processor bus for each word. Therefore, more backpressure can be tolerated before the FIFO fills up.

2. The second solution is to generate OAM cells farther down stream, past the transmit UTOPIA port. Since this problem exists only with OAM cells, the problem cannot occur.

2.3 Bit Integrity is Not Always Maintained Under Certain Error Conditions

Description

Bit integrity will not always be maintained when fewer than six cells are missing, or when a single errored cell occurs. There are two specific cases where bit integrity will not be maintained.

- If the cell containing a pointer value of 00 or the cell before a cell containing a pointer value of 00 has an SN error and the structure size is greater than the available payload of two cells. For full cell queues that meet these characteristics, there is about a 0.3% chance that a lost cell would cause bit integrity to be lost.
- If the following sequence of events occurs:

  (SN = 4, lost cell, lost cell, SN = 7, SN = 0, lost cell)

  and a pointer is in the cell with SN = 0 and the cell with SN = 7 is the first cell after an underrun.

For both of these cases, the AAL1gator II will detect a pointer mismatch error with the next pointer received after the lost cell, and will resynchronize to the next pointer.

Work Around

There is no work-around for this problem. The chance of this condition occurring is very small, and the overall impact is very minimal.

2.4 Bandwidth for a DS3 Line Cannot Always be Maintained with a 38.88 MHz System Clock

Description

Bandwidth for a DS3 line cannot always be maintained with a 38.88 MHz system clock.

Work Around

The AAL1gator II can support a 40 MHz system clock. By using a 40 MHz system clock, the DS3 bandwidth can be maintained as long as the processor accesses the AAL1gator fewer than 100 times per millisecond.

2.5 Behavior of RPHY_SOC with respect to RPHY_CLAV in PHY Mode

Description

When PM73121 UTOPIA interface is configured in PHY mode, the devices asserts RPHY-SOC, *Receive UTOPIA Layer Start of Cell*, when RPHY_DATA contains the first valid byte of the cell.

While receiving ATM cells, if the ATM Layer Device keeps /RPHY_EN, *Receive PHY Layer Enable*, asserted for longer than a cell time, the PM73121 will deassert RPHY_CLAV, *Receive UTOPIA Layer Cell Available*, at the completion of the cell and simultaneously assert RPHY_SOC.

This behavior may confuse some ATM Layer Devices that do not qualify RPHY_SOC signal with RPHY_CLAV signal as required by UTOPIA Level 1 specification: “RxCLAV indicates cycles when there is valid information on RxData/RxSOC.”

Work Around

For those ATM Layer Devices that do not qualify RPHY_SOC with RPHY_CLAV, the solution is to connect the PM73121 RPHY_SOC and RPHY_CLAV signals into an AND gate, and then connect the AND gate output to the RxSOC input of the ATM Layer Device.

3 (UPDATED) CHANGES TO TIMING PARAMETERS

The following timing parameters have been updated in issue 2 of PM73121 AAL1gator Datasheet (PMC-980620). Please refer to the datasheet for additional information:

Fig[1]	Description	Symbol	Parameter	Signal	Min	Max	Unit
55	Transmit Side Interface Bit Timing	Th	Clock hold	RL_SER	2		ns
58	Transmit Side High-Speed Interface Bit Timing	Th	Clock hold	RL_SER[0]	2		ns
59	Receive Side Low-Speed Interface Timing	Tq	Clock-to-output delay	TL_SIG, TL_SER	2	14	ns
63	Transmit UTOPIA ATM Timing	Tq	Clock-to-output delay	TATM_DATA	2	13	ns
64	TUTOPIA SPHY Timing	Tq	Clock-to-output delay	RPHY_DATA	2	13	ns
65	TUTOPIA MPHY Timing	Tq	Clock-to-output delay	RPHY_DATA	2	13	ns
74	RAM Write Cycle Timing	Twp	Write pulse width	/MEM_WE	Tch-1.3	Tch+0.3	ns
76	Microprocessor Memory Write Cycle Timing	Tq	Clock-to-output delay	/PROC_ACK	2	18	ns
76	Microprocessor Memory Write Cycle Timing	Tq	Clock-to-output delay	/MEM_CS	2	18	ns
77	Memory Read Cycle Timing	Tq	Clock-to-output delay	/MEM_CS	2	18	ns
77	Memory Read Cycle Timing	Tqmoe	Clock-to-output delay for activation of /MEM_OE	/MEM_OE	2	25	ns
78	Microprocessor Command Register Write Cycle Timing	Tq	Clock-to-output delay	/PROC_ACK	2	18	ns

[1] Figure numbers are from PM73121 Datasheet (PMC-980620).

Fig[1]	Description	Symbol	Parameter	Signal	Min	Max	Unit
82	Interrupt Timing	Tq	Clock-to-output delay	PROC_INTR	2	17	ns

NOTES

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