PM4351

COMET

ANSWERS TO FREQUENTLY ASKED QUESTIONS REGARDING THE COMET

APPLICATION NOTE

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PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	February 1999	Creation of Document.
2	June 2000	Reference to the receive backplane offset register as being 32H is incorrect. It should be 33H.

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LIST OF TABLES

1 REFERENCES

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2 DEFINITIONS

AIS	Alarm Indication Signal. This is a signal consisting of unframed all-ones serial digital data. It is transmitted when there is no good data to transmit (due to an upstream failure), and is useful for maintaining a timing reference to downstream equipment. This signal can be detected and transmitted by the COMET.
AMI	Alternate Mark Inversion. This is a ternary coding scheme for electrical transmission of digital data. Each binary one that is transmitted is represented by a RZ pulse that is of opposite polarity of the preceding pulse. Each binary zero that is transmitted is represented by a space (no pulse).
ANSI	American National Standards Institute. This is a non-profit, non-government federation of standards-making and standards-using organizations. It publishes standards, but does not develop them. Compliance with an American National Standard is voluntary and does not preclude anyone from manufacturing, marketing, purchasing, or using products, processes, or procedures not conforming to the standards. More on ANSI can be found at their Web site: web.ansi.org/default_js.htm
B8ZS	Block Eight Zeros Substitution. This refers to a zero suppression scheme that replaces eight consecutive zeros with a decodable sequence of LCVs. Zero suppression is important to ensure proper operation of clock recovery circuits
CAS	Channel-Associated Signaling. This is the term for the standardized (ITU-T G.704) signaling method consisting of a signaling multiframe carried in Timeslot 16 of the E1 frame.
CDRC	Clock and Data Recovery unit. This is PMC-Sierra's mnemonic to refer to the functional block in the T1XC which recovers the timing of the received signal, then uses that timing to sample the received data.

CHI	Concentration Highway Interface. This is a channelized timeslot backplane format originally defined on Lucent Technologies Microelectronics devices for T1 and E1 framing. The specification for the CHI can be downloaded from www.lucent.com/micro/prolit.html.
COMET	Combined E1/T1/J1 Framer Transceiver with Long-Haul. This is PMC-Sierra's mnemonic for its single-channel, full featured, 3.3V E1/T1/J1 framing device with integrated long-haul and short-haul LIU capability.
CPU	Central Processing Unit.
CRC	Cyclic Redundancy Check. This is a scheme for error monitoring by making a Boolean cyclic polynomial calculation over a digital data payload. The transmitter transmits the results of this calculation, and the receiver compares this to it's own calculation. If there is a difference, it is assumed that one or more bits have been corrupted during transmission of the digital payload. Of the standardized DS1 formats, only ESF uses a CRC. Of the standardized E1 formats, the CRC-multiframe format uses a CRC.
DAC	Digital-to-Analog Converter. This term is used generically to refer to a circuit that converts digital information into an analog signal. In the COMET, a DAC is used to create the transmitted line pulses.
DJAT	Digital Jitter Attenuator. This is PMC-Sierra's mnemonic for the functional block within the COMET which attenuates phase jitter on a timing reference. It contains a digital PLL to create a jitter-attenuated clock, and a FIFO to absorb the phase jitter.
DRAM	Dynamic RAM.
DS0	Digital Service Level 0. A DS0 is an octet in a bitstream that is repeated at an 8 kHz frame rate to give a total bandwidth of 64 kbit/s. Sometimes the LSB of the octet is robbed for signaling purposes so only 56 kbit/s is available for user data.

DS1	Digital Service Level 1. This term refers to a standardized format for digital signals which is comprised of 24 DS0s plus one bit of overhead which is repeated at an 8 kHz frame rate to give a total bandwidth of 1544 kbit/s.
DS1	Digital Signal, Level 1. This term refers to a standardized (ANSI T1.107) format for transmitting serial digital data at 1.544Mbps.
DS2	Digital Service Level 2. This term refers to a standardized format for digital signals which is comprised of four DS1 signals asynchronously multiplexed plus overhead for a sum of 789 bits repeated at an 8 kHz frame rate to give a total bandwidth of 6312 kbit/s.
DS3	Digital Service Level 3. This term refers to a standardized format for digital signals which is comprised of seven DS2 signals asynchronously multiplexed plus overhead for a sum of 4760 bits sent at a 44.736 MHz bit rate. Note that the frame rate is not 8 kHz.
DSX-1	Digital Signal Cross-Connect, Level 1. This term refers to the interface at a digital cross-connect (a convenient central point of cross-connecting, rearranging, patching and testing digital equipment and facilities) operating at the DS1 level.
E1	European transmission format level 1. This term is used to describe systems signals conforming to the ITU-T 2048 kbit/s format and interface specifications.
E1XC	E1 Transceiver. This is PMC-Sierra's mnemonic for the PM6341 E1 framer/transceiver device.
ELST	Elastic Store. This is PMC-Sierra's mnemonic for the functional block within the COMET that provides the elastic store function. The ELST is used for adapting the received data to the system backplane rate. Since these signals are not necessarily synchronized, they may slip with respect to each other. The function of the ELST is to control the slips such that they occur on the frame boundaries indicated on the backplane. For example, if the received data is faster than the system backplane then the ELST will drop full frames of data while maintaining the timeslot alignment on the backplane.

EMC	Electro-Magnetic Compatibility. This is a generic term used to refer to the ability of electronic equipment to operate in the presence of electro-magnetic forces as well as control of the electro-magnetic forces emanating from electronic equipment so that other equipment is not affected.
ESF	Extended Superframe Format. This is a standardized (ANSI T1.107) DS1 format. It makes use of the DS1 F-Bits to provide a 24-frame signaling multiframe, CRC error checking, and an out-of band maintenance channel.
F-Bit	Framing Bit. This term denotes the first bit of each DS1 frame that is used for carrying the framing overhead information. The specific use of this bit depends on the DS1 framing format.
FEAC	Far-End Alarm and Control. This term is applied to channels in a transmitted data stream that are reserved for carrying alarm and control information to and from the far-end equipment.
FEBE	Far-End Block Error. This term refers to standardized indicators that the far end equipment has received at least one bit error within a block of received data. In the E1 format, the E-bit of the CRC-4 multiframe structure (defined in ITU-T G.704) is used for FEBE indication.
FIFO	First-In First-Out buffer. This term refers to a digital buffer that outputs data in the same order as it was input.
Flag	A pre-defined pattern which marks the start and end of a data packet. For HDLC, the flag character is 01111110 (binary).
Frame Relay	This term is used in multiple contexts. It can refer to a switching technology, an interface standard or a set of data services. More on Frame Relay can be found at the Frame Relay Forum Web site: www.frforum.com
GPIC	General Purpose PCI Controller. This is PMC-Sierra's term for the functional block of the COMET device which translates all transactions initiated by the RMAC and TMAC into activity onto a 32-bit PCI bus operating at up to 33 MHz.

HDB3	High-Density Bipolar of order 3. This is a zero suppression scheme that uses the intentional insertion of AMI LCVs to maintain a minimum transition density in the E1 signal. This function is important since it provides clear channel capability — the payload content is not restricted by the capabilities of the remote receiver's clock recovery unit.
HDLC	High-Level Data Link Control. A common message-based datalink protocol (OSI Layer 2) issued by ISO. Messages are delineated by flag characters and use a CRC frame check sequence for error detection.
IBIS	I/O Bus Interface Simulation. This is a standardized format for simulating I/O of digital logic devices. PMC-Sierra provides free IBIS models for most products, available from the PMC-Sierra Web site.
ISDN	Integrated Services Digital Network. This is a worldwide public telecommunications network that is implemented as a set of digital switches and paths supporting a broad range of services.
IPNS	ISDN PBX Network Specification. This is a forum with the mission "to promote the further worldwide proliferation of QSIG including its extension to other network technologies (e.g., IP, ATM, Frame Relay) with special consideration of quality and other critical characteristics of real-time communication." More on the IPNS Forum can be found at their Web site: www.qsig.ie/index.htm
ITU-T	International Telecommunication Union - Telephony. This is a committee within a United Nations treaty organization. The charter is "to study and issue recommendations on technical, operating, and tariff questions relating to telegraphy and telephony." Its primary objective is end-to-end compatibility of international telecommunications connections. More on the ITU-T can be found at their Web site: www.itu.ch
J1	Japanese transmission format level 1. This term is used to describe systems signals conforming to the TTC format and interface specifications for both 1544 kbit/s and 2048 kbit/s rates.

LCV	Line Code Violation. This term denotes a received bipolar pulse that violates the AMI, B8ZS, or HDB3 ternary coding scheme. LCV events are detected and accumulated by the COMET.
LIU	Line Interface Circuit. This is a generic term used to refer to the circuitry in telecommunications equipment responsible for shaping the electrical signal for transmission on the transmission cable and responsible for recovering a clock from the received electrical signal on the cable. The LIU will usually implement a line-coding scheme (e.g. B8ZS or HDB3) as well as some performance monitoring, alarm, and diagnostic circuitry.
Long-Haul	This term applies to T1 interconnections over 100 Ω twisted pair cable that are more than the 655 feet specified in DSX-1 electrical interface specifications (e.g. ITU-T G.703). Cable distances up to 6000ft are typical of long-haul connections. ANSI T1.403 specifies that the signal attenuation that can be expected over a long-haul cable span is 22dB, although most long-haul receivers are designed to operate with attenuation up to 36dB.
LOS	Loss-of-Signal. This term refers to the state a clock recovery unit is in when there is no input signal. Since both DS1 and E1 require a minimum pulse density, the COMET monitors for both digital and analog LOS. The COMET declares digital LOS if the number of consecutive spaces (ZEROs) received exceeds a programmable threshold. The COMET declares analog LOS by implementing the ITU-T G.775 analog LOS requirements based on the analog signal level.
MVIP	Multi-Vendor Interface Protocol. This is an industry standard for a TDM bus interface between a physical layer framing subsystem and a payload processing (or switch) subsystem. More on MVIP can be found at the GO-MVIP Web site: www.mvip.org
NRZ	Non-Return-to-Zero. This refers to the common electrical coding scheme for serial digital data. Logical ones are represented as a pulse that is high for the full bit period. Logical zeros are represented as no pulse for the full bit period. This scheme is useful for serial digital data that has an associated clock signal.

OOF	Out-Of-Frame alignment. This is the state a DS1 or E1 framer is in if it cannot find the frame alignment pattern within the received serial 1.544Mbps data.
PCM	Pulse-Coded Modulation. A term encompassing digital serial data which is encoded into electrical pulses. AMI, B8ZS, and HDB3 are PCM coding schemes.
PLL	Phase-Locked Loop. The generic term for a feedback system that generates a clock with a fixed (locked) phase/frequency relationship to some reference clock.
QSIG	QSIG is a protocol specified by the IPNS to link ISDN PBXs in a private telecommunications network. It has also found many other important applications such as: multi-vendor ISDN PBX based private networks, networking of remote ISDN PBXs interconnecting voice/fax/DP servers, providing network wide reach for applications supporting mobility in corporate networks Virtual Private Networks, broadband private networks, and trans-european trunked radio. Further information on QSIG can be found at the IPNS Web site: www.qsig.ie/qsig/index.htm
RJAT	Receive Jitter Attenuator. This is PMC-Sierra's mnemonic for the functional block within the COMET which attenuates phase jitter on the receive timing reference. It contains a digital PLL to create a jitter-attenuated clock, and a FIFO to absorb the phase jitter.
RPSC	Receive Per-Channel Serial Controller. This is PMC-Sierra's mnemonic for the functional block of the COMET which allows per-channel functions to be performed on the received PCM and signaling data, before being passed to the receive backplane.
RZ	Return-to-Zero. This refers to an electrical coding scheme for serial digital data. A logical ONE is represented as a pulse that is high for half the bit period then returns to low (zero) for the remainder of the bit period. A logical ZERO is represented as no pulse. This scheme is useful for serial digital data from which a clock must be recovered.
SF	Superframe Format. This is a standardized (ANSI T1.107) DS1 format. It makes use of the DS1 F-Bit to maintain a 12-frame signaling multiframe.

SIGX	Signaling Extractor. This is PMC-Sierra's mnemonic for the functional block of the COMET that extracts and stores the received robbed-bit (channel-associated) signaling information. It also provides some per-channel functions on the received PCM data.
SLC®96	Subscriber Loop Carrier 96. This is a standardized[12] DS1 format. It is similar to SF, but makes use of the F-Bits such that it also carries a datalink. This datalink is used for concentrating up to four DS1 streams for an aggregate of 96 (4 x 24) 64kbps channels.
ST-BUS®	Standard Telecom Bus. This is a registered trademark of Mitel Corporation used to describe a TDM bus used for DS0 cross-connection. The ST-BUS is a subset of the MVIP bus.
T1	Transmission format level 1. This term is used loosely to describe systems carrying DS1-formatted signals electrically over cable.
T1DM	T1 Data Multiplexer. This is a standardized[9] DS1 format. It uses Timeslot 24 of the DS1 frame to pass additional framing information as well as a remote alarm and datalink.
T1XC	T1 Transceiver. This is PMC-Sierra's mnemonic for the PM4341A T1 framer/transceiver device.
TDM	Time-Division Multiplexed.
TJAT	Transmit Jitter Attenuator. This is PMC-Sierra's mnemonic for the functional block within the COMET which attenuates phase jitter on the transmit timing reference. It contains a digital PLL to create a jitter-attenuated clock, and a FIFO to absorb the phase jitter.
TPSC	Transmit Per-Channel Serial Controller. This is PMC-Sierra's mnemonic for the functional block of the COMET which allows per-channel functions to be performed on the PCM and signaling data from the transmit backplane, before transmission.
TRAN	Transmitter. This is PMC-Sierra's mnemonic for the functional block of the COMET that inserts the DS1 or E1 framing overhead into the transmitted data stream. The TRAN can be configured to operate in unframed mode.

V5	V5. This is a standardized (ITU-T and ETSI) protocol suite for the connection of access networks to local exchange. The access network itself typically has public switched telephone network and ISDN interfaces (user ports) to the customer. The V5 interfaces are based on interfaces at 2048 kbit/s (E1).
XLPG	Transmit Line Pulse Generator. This is PMC-Sierra's mnemonic for the functional block of the COMET that generates the transmit pulse shapes that drive the line interface. The XLPG provides the industry's highest resolution of pulse shape programmability.

3 BACKGROUND AND OVERVIEW

PMC-Sierra's PM4351 Combined E1/T1/J1 framer with long-haul transceiver is a full-featured device for processing bit serial links running international first order transmission formats over cable at lengths exceeding 6000 ft.

Due to the versatility of the COMET, the data book (PMC-970624) for that device is quite lengthy. In order to help customers quickly find the answers to their questions, the following list of answers to frequently asked questions has been compiled.

If further clarification is required, please contact PMC-Sierra's technical support team at apps@pmc-sierra.com.

4 ANSWERS TO FREQUENTLY ASKED QUESTIONS

4.1 General Questions

Q1) Are there any reference designs or application notes available for the COMET?

A1) Yes. There are reference designs and application notes available for the COMET.

The COMET Reference Design (PMC-981210) shows four COMET devices in a channelized T1 or E1 application. On the system side, the COMET devices are shown connecting to a 8.192 MHz MVIP bus; on the line side, the COMET devices are shown with line protection and EMC circuitry and can be connected directly to T1 or E1 lines carrying short-haul or long-haul signals.

The COMET Software Driver, complete with both a user's guide and source code in C-language, gives examples of how to program a PCI host to work with the COMET.

The COMET Compliance Reports (PMC-981182, PMC-981183, PMC-981184, PMC-981185, and PMC-981186) are from an independent test house showing compliance of the COMET Reference Design with COMET Software Driver to ETSI ISDN interface and surge protection standards.

A COMET Technical Overview (PMC-970605) is available which explains the functions and technology of the COMET.

PMC-Sierra Sales Representatives have copies of these documents available for distribution. It is suggested that customers periodically query their local PMC-Sierra Sales Representative for the latest documentation for the COMET.

PMC-Sierra also has a World Wide Web site at www.pmc-sierra.com from which documentation can be ordered or downloaded. Furthermore, customers can register themselves on the Web site to be notified in the event of changes to the documentation.

Q2) Is there an evaluation platform for the COMET?

A2) PMC-Sierra does plan to provide an evaluation kit consisting of a PCI-based hardware module and a Windows 95 user software interface. However, at the time of issuance of this document, this kit was still under development.

Please contact your local PMC-Sierra sales representative to inquire on the status of this kit.

In the meantime, it is possible to request a demonstration of the COMET by a PMC-Sierra Field Applications Engineer. Again, please contact your local PMC-Sierra sales representative to make arrangements for such a demonstration.

Q3) What are the packaging options for the COMET?

A3) The COMET comes in two packaging options:

- 80-pin PQFP (14mm x 14mm). This package option has a –RI suffix.
- 81-ball CABGA (9mm x 9mm). This package option has an –NI suffix.

Q4) Does the COMET support industrial temperature range?

A4) Yes, the COMET supports industrial temperature range (-40C to 85C).

Q5) What is the power consumption of the COMET?

A5) The power consumption of the COMET is dependent on the aggregate bandwidth as well as the number of functions enabled in the device.

Typical power consumption has been measured at 300mW. However, the characterization of the power consumption is still ongoing. For the latest information regarding power consumption of the COMET please contact Larry Kennedy, Marketing Manager. Mr. Kennedy can be reached at larry_kennedy@pmc-sierra.com or 604-415-6163.

4.2 Software Questions

Q6) Is a microcontroller required to control and monitor COMET?

A6) Yes, the COMET must be controlled and monitored via an 8-bit parallel microprocessor bus. This bus is compatible with both Motorola and Intel microcontrollers.

The COMET Software Driver gives reference software routines in C-language source code for controlling and monitoring the COMET. This driver can be compiled to run on most microprocessor platforms.

The COMET requires much less microprocessor interaction than PMC-Sierra's previous generation of T1XC and E1XC devices:

- The COMET automates the ETSI CRC-to-non-CRC interworking procedure, eliminating the need for microprocessor interaction in this procedure.
- The COMET automates the transmission of RAI and Yellow alarms.
- The COMET has the industry's deepest FIFOs (128 bytes) in each of its three integrated HDLC controllers. These deep FIFOs reduce the frequency at which the microprocessor must transfer data to/from them.
- The COMET has an interrupt-on-signaling-change feature that eliminates the need for continuous polling of the internal signaling registers.

Q7) Are there any software drivers available for the COMET?

A7) Yes. PMC-Sierra provides a basic software drivers for the COMET for a zero-dollar license (i.e. they are free for registered customers). This software driver can be downloaded after registering on PMC-Sierra's Web site at www.pmc-sierra.com.

Q8) Can the COMET be reset via software?

A8) Yes. In fact the COMET should always be reset by software after a power-up sequence (following a hardware reset) and at any other time required by the embedded processor.

After software or hardware reset, all the COMET internal registers will be at the default values described in the COMET Databook (PMC-970624).

Q9) How should the COMET be initialized?

A9) After a reset (software reset or hardware reset), the registers will default to the values listed in the register descriptions in the COMET Data Book (PMC-970624). However, some additional configuration is almost always required. In general, the initialization of the COMET depends on the desired functionality — the COMET is designed to be highly flexible and therefore has many registers that must be initialized.

The COMET Software Driver gives example routines for initializing the COMET for many standard T1, E1 and J1 applications.

If your application is not covered in the COMET Software Driver, please contact PMC-Sierra's technical support team at apps@pmc-sierra.com for initialization recommendations.

4.3 Modeling and Simulation Questions

Q10) Are IBIS models available for the COMET?

A10) Yes. PMC-Sierra plans to provide an IBIS model for the COMET for a zero-dollar license (i.e. free for registered customers). This model can be downloaded after registering on PMC-Sierra's Web site at www.pmc-sierra.com.

However, at the time of the issuance of this document the generation of the IBIS model is pending a complete characterization of the COMET. Therefore please check PMC-Sierra's Web site regularly for the release of this model.

Q11) Are full-functional models available for the COMET?

A11) Yes. PMC-Sierra plans to provide a full-functional model for the COMET for a zero-dollar license (i.e. free for registered customers). Customers interested in obtaining this model should contact Larry Kennedy, Marketing Manager. Mr. Kennedy can be reached at larry_kennedy@pmc-sierra.com or 604-415-6163.

4.4 Line Interface Questions

Q12) Can the COMET terminate long-haul signals?

A12) Yes, the COMET is designed to terminate both long-haul and short-haul signals on the line interface.

The LIU portion of the COMET is greatly enhanced over the equivalent function in PMC-Sierra's T1XC, E1XC, and QDSX products. It is capable of sourcing and sinking T1 or E1 interface signals that have been typically attenuated up to 36 dB or 43 dB respectively. These highly attenuated signals are commonly termed "long-haul" because they are the result of transmission over long lengths (over 6000 ft) of cable.

In the receive direction, the COMET contains adaptive equalization circuitry with a wide dynamic range. This equalization is capable of equalizing the attenuation caused by cable types such as ABAM, PIC, and pulp-insulated cable.

In the transmit direction, the COMET has the industry's most sophisticated pulse shaper. It is fully programmable (with a much higher resolution than the T1XC, E1XC, or QDSX) and allows the application of pre-emphasis on short-haul pulses or the application of line build-out on long-haul pulses. Line build-out is a standardized function (ANSI T1.403 and FCC Part 68) required to minimize near-end cross-talk.

Q13) Does the COMET meet line protection requirements?

A13) Yes, the COMET was designed with the assumption that line protection components would be present on the line interface. That circuitry is described in the COMET Reference Design (PMC-981210) and that reference design was tested for compliance against FCC Part 68 requirements for line protection. Copies of the compliance certificates are given in the appendices of the reference design.

Q14) Does the COMET meet EMC requirements?

A14) Yes, the COMET was designed with the assumption that it would be used in environments where EMC is required. Guidelines for ensuring EMC in COMET-based designs are given in the COMET Reference Design (PMC-981210).

Q15) Does the COMET meet T1, E1 and J1 jitter requirements?

A15) Yes. Although, there are many different standards that specify jitter requirements on T1 and E1 interfaces, the COMET meets all the major applicable standards such as:

- ANSI T1.102
- ANSI T1.107
- ANSI T1.403
- AT&T TR 54016
- AT&T TR 62411
- Bellcore GR-303-CORE
- Bellcore TA-NWT-000170
- ETS 300 011
- ETS 300 166
- ETS 300 233
- ETSI CTR 4, CTR 12, and CTR 13
- ITU-T G.823
- ITU-T I.431

These standards specify four kinds of jitter requirements on these interfaces: jitter tolerance, jitter transfer, intrinsic jitter, and output jitter.

Jitter tolerance describes the ability of the receive port to recover a clock from the received signal in the presence of timing jitter. The requirement is normally specified that no bit errors should occur in the presence of jitter that falls within a specific range of amplitudes and frequencies.

Jitter transfer describes the ability of a transmit port to minimize the timing jitter transferred from the transmit reference clock to the transmit line signal. Jitter transfer requirements specify a minimum attenuation for each jitter frequency.

Intrinsic jitter (also called generated jitter or residual jitter) describes the ability of a transmit port to minimize the timing jitter it adds to the transmit line signal, independent of the jitter transferred from the transmit reference clock.

Output jitter is a combination of jitter transfer and intrinsic jitter. Output jitter is easier to measure because it does not require that the transferred and intrinsic components be separated. Therefore a wide-band jitter measurement is made at the transmit port while a range of jitter is applied to the transmit reference clock. At no time should the output jitter exceed a specified jitter amplitude.

The COMET meets all applicable standards for jitter tolerance, jitter transfer, intrinsic jitter and output jitter for T1, E1, and J1 interfaces.

Q16) Are the jitter attenuators on the COMET “crystal-less”?

A16) Yes. The jitter attenuators, RJAT and TJAT, in the COMET are both based on digital phase-locked loops. Therefore, their loop filters are implemented as digital functions and no external pullable crystals are required. This means that the COMET provides crystal-less jitter attenuation.

The COMET, like all T1/E1 LIUs, does require one jitter-free system clock that may be sourced from a crystal oscillator.

Q17) How does the COMET meet return loss requirements on the line interface?

A17) To meet return loss requirements, the receive and transmit circuits must prevent an impedance that matches the cable characteristic impedance. The better the match, the better the return loss.

Common return loss requirements are shown in Table 1.

Table 1 - Standardized T1/E1 Return Loss Requirements

		Interface Type			
		T1 100Ω	**E1 75Ω**	**E1 120Ω**	**J1 100Ω**
Receive Return Loss	Standard	None	ITU-T G.703	ETS 300 011	JT-G703
	Requirement	N/A	≥ 15dB at 2048 kbit/s	≥ 12dB from 51 kbit/s to 102 kbit/s, ≥ 18dB from 102 kbit/s to 2048 kbit/s, ≥ 14dB 2048 kbit/s to 3072 kbit/s	≥ 15dB at 2048 kbit/s
Transmit Return Loss	Standard	None	None	ETS 300 166	None
	Requirement	N/A	N/A	≥ 6dB from 512 kbit/s to 102.4 kbit/s, ≥ 8dB from 102.4 kbit/s to 3072 kbit/s	N/A

Q18) Does the COMET meet ETSI transmit return loss requirements?

A18) Yes, the COMET meets the requirements for transmit return loss described in ETS 300 166 (and shown in Table 1).

Q19) Where is the 110Ω impedance mentioned in the COMET line interface circuit description?

A19) Tto provide software-selectibility between T1, E1, and J1, the COMET analog designers determined that a line interface impedance of 110Ω sufficiently matches both 100Ω T1/J1 cable as well as 120Ω E1 cable. Therefore, the recommended line interface circuit for those applications has an effective impedance of 110Ω.

There is no physical component of value 110Ω, rather the impedance matching relies on impedance “reflection” through the transformers. The effective impedance at the line side of the transformers is equal to the impedance at the chip side multiplied by the square of the turns ratio.

For example, in the receiver there is an 18.2Ω resistor placed differentially on the chip side of the transformer. This resistance drives the line through a 1:2.42 ratio transformer. The effective impedance is therefore approximately 110Ω.

Q20) Does the COMET support the 75Ω E1 interface?

A20) Yes, the COMET certainly supports the 75Ω E1 interface standardized in ITU-T G.703. The circuitry required for this interface is described in the COMET databook.

Q21) Why does the COMET reference design not show the 75Ω E1 interface?

A21) For ISDN UNIs and access (as well as many other structured and unstructured E1 services) the120Ω interface is the only standardized interface. Therefore, the COMET reference design addresses the majority of the application space for E1 interfaces while highlighting the great advantage of the COMET's software-selectibility.

Using the COMET, it is possible to design one board for sale in Europe, North America and Japan, with software selecting between the 100Ω T1/J1 and the 120Ω E1 — no need for relays or population options!

If it is desired to also support the 75Ω E1 interface, then the corresponding circuitry (detailed in the COMET Databook, PMC-970624) would be added to the circuitry of the reference design. Relays or population options would be used to select that interface.

Q22) What transformer manufacturers does PMC-Sierra recommend for use with the COMET?

A22) Most manufacturers of telecommunications pulse transformers should be able to provide a transformer suitable for use with the COMET.

Manufacturers that PMC-Sierra has evaluated for use with the COMET are (in alphabetical order):

Halo Electronics
P.O. Box 5826
Redwood City, CA 94063
Phone: (650) 568-5800
Fax: (650) 568-6161
E-mail: HALOElect@aol.com
Web: www.haloelectronics.com

Midcom

121 Airport Drive
P.O. Box 1330
Watertown, SD 57201-6330
Toll Free: 1-800-643-2661(US and Canada)
Phone: (605) 886-4385
Fax: (605) 886-4486
Web: www.midcom-inc.com

Pulse
12220 World Trade Drive
San Diego, CA 92128
Phone: (619) 674-8100
Fax: (619) 674-8262
Web: www.pulseeng.com

Schott Corporation
1000 Parkers Lake Road
Wayzata, MN 55391
Phone: (612) 475-1173
Fax: (612) 475-1786
Web: www.schottcorp.com

Q23) How does the COMET generate transmit pulse shapes?

A23) The COMET has the industry's most sophisticated integrated transmit pulse shaper, contained in the XLPG functional block. This pulse shaper uses a high-resolution DAC to convert a series of user-programmable values into a precision pulse shape on the transmit line interface.

This programmability accommodates transmit line build-out requirements for long-haul interfaces, as well as pulse pre-emphasis for short-haul interfaces.

The recommended values for all standard pulse shapes are given in the COMET Databook (PMC-970624).

Q24) Does the COMET have a special transmit pulse shape to help meet AT&T TR62411 intrinsic jitter requirements?

A24) Yes. The TR62411 pulse template is different than other T1 pulse templates (e.g. ANSI T1.403) because it is designed to ensure that there is no inter-symbol interference perceived as jitter effects on the transmitted pulse.

The COMET provides the ability to programmably alter the transmit pulse shape. Using this XLPG function, the COMET Data Book (PMC-970624) specifies a set of XLPG codes that should be used to generate a pulse shape that meets TR62411 pulse shape and intrinsic jitter requirements.

Q25) How would protection switching and redundancy be accomplished with the COMET?

A25) Depending on the extent of the redundancy and the desired protection switching characteristics, the COMET has features that aid design.

At the chip level, the COMET's transmit line drivers are tri-stateable. Therefore it is possible to use this tri-stating to have one COMET in standby while the another drives the line. This facilitates switching between redundant COMET devices without the use of external relays.

The COMET provides extremely flexible timing options that can allow redundant COMET devices to be aligned such that when switching, the data corruption is minimal (one or no bits corrupted).

The COMET provides all standardized performance monitoring alarms and parameters, many with interrupts, to allow software to quickly identify and react to failures and performance degradation.

4.5 Frame Format Questions

Q26) What are the differences between J1 and T1?

A26) J1 refers to Japanese first order digital transmission systems. Unfortunately however, the term "J1" can refer to quite a number of interface variants. Here is an explanation of those variants.

In the past Japan has adopted both European and American formats. Therefore, there are some J1 interfaces that operate at the E1 rate of 2.048 Mbit/s rather than the T1 rate of 1.544 Mbit/s. The COMET can support E1 formats, but was not specifically designed to meet Japanese standards for 2.048 Mbit/s.

For Japanese PBX interfaces, the TTC has created its own standards for a "Y-interface." In particular, JJ-20.11 states that the interface rate is 2.048 Mbit/s. However, there are many significant differences with respect to European E1. Firstly, the line coding used is CMI rather than HDB3. The basic frame alignment is indicated by CMI violations rather than a framing pattern in Timeslot 0. An 8-frame multiframe is used rather than a 16-frame multiframe. There are many other differences as well. The COMET is not compatible with this interface.

For Japanese 2.048 Mbit/s ISDN PRI interfaces, the TTC has adopted ITU-T standards with JT-I431-b. This is exactly equivalent to European ISDN and is fully supported by the COMET.

Within the 1.544 Mbit/s J1 application, Japan has a number of variants as described below.

For Japanese "Inter-Network" interfaces, the TTC has adopted the ITU-T standards with JT-G703, JT-G704, JT-G706 and JT-G733. However, these Japanese versions do differ significantly. Firstly, the Japanese want the output pulse shape to be measured at the output port, rather than at the distribution frame. Also, the cable characteristic impedance is 110Ω rather than 100Ω. The Japanese interface only supports the use of ESF for inter-network interfaces, but they change the way the CRC-6 is calculated. The COMET has been designed to be able to accommodate all of these differences, including framing in the presence of the alternate CRC-6.

For older Japanese inter-network interfaces a 1.544 Mbit/s format based on SF was used. This did differ from American T1 SF in that the yellow alarm was transmitted in the 12th F-Bit rather than in Bit 2 of all timeslots. This variant of the yellow alarm, often called the "Japanese yellow alarm" created difficulty for many American T1 framers. The COMET however has an option to frame in the presence of the Japanese yellow alarm and is therefore compatible with this interface. The COMET can also transmit the Japanese yellow alarm under software control.

For Japanese 1.544 Mbit/s ISDN PRI interfaces (the "I-interface"), the TTC has adopted the ITU-T standards with JT-I431. There are some minor differences with respect to American ISDN. The ESF datalink is not used. The CRC-6 is required to be checked as protection against mimic framing. The COMET is compatible with these requirements.

The trend of Japanese standards is toward better harmonization with American and European standards. This implies that the COMET will be compatible with most emerging J1 applications.

Q27) Does the COMET meet ETSI framing and interworking requirements?

A27) Yes, the COMET automatically performs the framing and interworking requirements described in the following ETSI standards: ETS 300 011, ETS 300 233, TBR 004, TBR012, and TBR013. The COMET was tested against these standards at an independent test facility and the compliance reports are available as a document (PMC-981182, PMC-981183, and PMC-981184).

The COMET does not need the extensive interrupt processing that was required on PMC-Sierra's previous generation of E1 framers, such as the PM6341 E1XC.

Q28) Does the COMET have a transmit elastic store?

A28) Yes. The COMET has a two-frame circular elastic store in each of the transmit and receive directions. These elastic stores can be optionally bypassed.

Q29) When should the COMET transmit elastic store be used?

A29) In general, an elastic store in a T1/E1 physical interface is used to provide controlled frame slip buffering. This allows data to be rate-adapted to system backplanes that may be asynchronous to the line timing. The purpose of these system backplanes is to align multiple lines on frame boundaries to facilitate cross-connection of the DS0 timeslots.

Historically, frame slip buffering was only performed in the receive direction and the transmit timing was synchronized to the system backplane.

However, now some carriers require that the transmit timing of every port to be loop-timed to its receive timing. To accomplish this while also maintaining independent timing on the system backplane requires frame slip buffering in both the transmit and receive directions.

Another application that requires transmit frame slip buffering is when multi-channel echo cancellation is needed in both directions. Echo cancellers can be an expensive component and it is often more cost-effective to use one system backplane in both directions so that a single multi-channel echo canceller can be used. The transmit elastic store allows the line timing to flow through in both directions while the echo canceller operates on many simultaneous channels.

By integrating the transmit elastic store, the COMET is suitable for applications with unusual transmit timing requirements.

Q30) Why does the COMET have three integrated HDLC controllers?

A30) The number of HDLC controllers required depends on the application. Some applications require up to three HDLC controllers. Here is a brief discussion of COMET applications and how many HDLC controllers are required for each.

- For T1 SF interfaces, no HDLC controller is needed.
- For T1 ESF interfaces, an HDLC controller is needed to process the facility datalink packets carried in the M-Bit overhead.
- For T1 ISDN PRI, two HDLC controllers are needed. One controller processes the ESF facility datalink; the other controller processes the ISDN D-Channel carried in Timeslot 24.
- For J1 ISDN 1.544 Mbit/s PRI interfaces, only one HDLC controller is needed (to process the D-Channel because the ESF facility datalink is not used).
- For J1 ISDN 2.048 Mbit/s PRI, one HDLC controller is needed to process the ISDN D-Channel carried in Timeslot 16.

- For E1 basic framing (non-CRC) interfaces, no HDLC controller is needed.
- For E1 ISDN PRI, one HDLC controller is needed to process the ISDN D-Channel carried in Timeslot 16.
- For E1 V5.1 and V5.2 interfaces, up to three HDLC controllers are needed. These controllers process the V5 C-Channels carried in Timeslots 15, 16 and 31.

As you can see, the COMET's three integrated HDLC controller supports all major T1/E1 applications, including the emerging V5 applications.

Q31) Does the COMET support QSIG?

A31) Yes. QSIG is an extension of public ISDN signaling into private networks. As such it has the same Layer 1 and Layer 2 of public ISDN signaling. In other words it uses the HDLC subset called LAPD carried in the D-Channel.

The COMET internal HDLC controllers are capable of terminating the LAPD protocol carried in the D-Channel, and is therefore compatible with QSIG applications.

QSIG does differ from public ISDN signaling protocol at Layer 3, but that Layer is transparent to the COMET.

More on QSIG can be found at the ISPN Forum Web site: www.qsig.ie/qsig/index.htm.

Q32) Can I process frame relay packets using the COMET integrated HDLC controllers?

A32) No. The integrated HDLC controllers can only be trained on single timeslots and are intended for overhead processing such as facility data links and ISDN D-Channel. The high bandwidth of frame relay and the fact that many frame relay channels span multiple timeslots mean that external HDLC controllers should be used instead.

In particular, PMC-Sierra's PM7364 and PM7366 FREEDM family of products provide optimized HDLC processing for frame relay applications. The FREEDM products connect seamlessly to the COMET using the NxDS0 backplane mode.

Q33) How do the COMET PMON counters relate to ANSI T1.231 performance parameters?

A33) The COMET contains several performance monitor counter registers (PMON) that accumulate common performance parameters on intervals (up to one second) that are under the microprocessor's control.

The operation of these counters is explained in the COMET databook (PMC-970624). There is also an explanation in the Operations section of the databook. Writing any value to the Global PMON Update register (00DH) will update all the PMON registers. The PMON registers can then be read until the polling interval is complete and the micro updates the PMON again.

The PMON registers contain the raw defect counts collected in a one second interval, while specifications like ANSI T1.231 require more comprehensive performance parameters collected on 15 minute intervals. Therefore, software must process the PMON values and accumulate them in memory. Furthermore, the COMET must be configured such that its PMON registers count appropriate events.

Here are some examples of T1.231 parameters and their relationship to the COMET PMON counters.

- T1.231 defines the CV-L (coding violation) parameter as "count of BPV plus the count of EXZ" for both SF and ESF. In the COMET PMON there is an LCV counter. The COMET contains a BPV bit in Register 003H that controls the definition of LCV. The default setting is BPV=0 which means that both BPV and EXZ events will be counted by the PMON LCV counter. Therefore, so long as BPV=0 then the LCV count in the COMET will correspond to the CV-L parameter required by T1.231.

- T1.231 defines the ES-L (errored second) parameter as "(BPV + EXZ) ≥ 1 or LOS ≥ 1" in the interval. The (BPV + EXZ) is of course the same as the CV-L described above. The LOS event in T1.231 is "175 +/- 75 contiguous pulse positions with no pulses of either positive or negative polarity." In the COMET the LOS defect detection criteria is controlled by the LOS[1,0] bits in Register 010H. When set to LOS[1]=1 and LOS[0]=1, the COMET will declare LOS defect when 175 continuous bit periods with no pulses are detected. The LOS defect is indicated with the LOSV bit in Register 012H. Therefore, your software should poll the LOSV bit in addition to the PMON registers. To report the T1.231 ES-L parameter, your software must check both the COMET LCV count and the LOSV status; if either are non-zero then ES-L=1.

- T1.231 defines the SES-L (severely errored second) parameter as "(BPV + EXZ ≥ 1544 or LOS ≥ 1" in the interval. This is similar to the ES-L except that

your software would only check to see if the COMET LCV count is greater or equal to 1544 or that the LOSV bit is set before declaring SES-L.

As you can see, the COMET provides all the basic defect detection and counting required for T1.231 performance monitoring, but software may have to combine some of this information to derive the standardized performance parameter definitions.

4.6 Backplane Interface Questions

Q34) What are the details of the COMET MVIP backplane interface?

A34) The MVIP bus is a TDM bus that is byte-interleaved and scalable in multiples of 2.048 MHz. The bus consists of three signals: a frame synchronization pulse, a data signal and a clock signal. Typically multiple ports (T1, E1 or J1) are frame aligned to the MVIP bus using frame slip buffers. This allows cross-connection of the DS0 timeslots.

The MVIP bus is specified by the GO-MVIP industry group. More information on the MVIP bus and the GO-MVIP group can be found at their Web site: www.mvip.org.

The COMET backplane interface is fully compatible with the MVIP bus at the rates of 2.048 MHz, 4.096 MHz, and 8.192 MHz.

Q35) Can multiple COMET devices be connected to a single MVIP bus?

A35) Yes. Up to four COMET devices can be connected to an 8.192 MHz MVIP bus without any external glue logic. Similarly, up to two COMET devices can be connected to a 4.096 MHz MVIP bus and a single COMET can be connected to a 2.048 MHz MVIP bus.

This is accomplished by programming each COMET on the shared bus with a unique timeslot offset in the receive and transmit backplane offset registers (registers 33H and 43H respectively). The MVIP frame pulse is common to all the COMET devices on the bus so each COMET will take control of the bus in the order of its timeslot offset. When the COMET is not in control of the bus it will automatically tri-state to avoid bus contention.

Q36) What are the details of the COMET CHI backplane interface?

A36) Framers from Lucent Technologies Microelectronics Group (formerly AT&T Microelectronics) have a flexible backplane interface that has some differences from the MVIP bus but generally serves the same purpose of frame aligning multiple ports to allow easy cross-connection of DS0 timeslots.

The specification for the CHI bus can be downloaded from Lucent's ISDN documentation Web page at www.lucent.com/micro/isdn/prolit.html.

The COMET backplane interface is fully compatible with the CHI bus.

Q37) How is the fractional NxDS0 interface on the COMET used?

A37) Some applications of T1, E1, and J1 only use a fraction of the payload available, for services termed "fractional." These fractional payloads are typically allocated in integral multiples of DS0's, for Nx64kbit/s service or Nx56kbit/s service.

The COMET supports fractional services by providing a NxDS0 backplane interface mode. In this mode, the COMET will gap the backplane clocks during unused payload and overhead cycles, leaving the backplane clocks toggling only during desired payload timeslots. This enables direct connection to external serial controllers. For example, using the NxDS0 mode the COMET can be connected seamlessly to PMC-Sierra's PM7366 FREEDM-8 frame relay protocol engine.

The NxDS0 mode in the COMET is enabled using Registers 030H and 040H.

4.7 Layout and Board Design Questions

Q38) Is special treatment of the power supply necessary for the COMET?

A38) The COMET does contain sensitive analog circuitry (e.g. phase-locked loops, equalizers, DACs and ADCs) and therefore some care should be taken to ensure that the COMET power supply is noise free and capable of providing required switching current.

In general, the COMET Reference Design (PMC-970624) shows a scheme that sufficiently protects the power pins from noise by using noise bypassing capacitors and filtering inductances (i.e. ferrite beads).

On boards where there are known excessively noisy components, extra precautions such as isolated power planes may be necessary for the COMET. If you are unfamiliar with such techniques or unsure whether they are necessary, feel free to contact PMC-Sierra Applications Technical Support at apps@pmc-sierra.com.

Q39) How do I ensure good signal integrity in my COMET design?

A39) Signal integrity is more dependent on edge rates than on clock frequency. Since the clock edges of modern integrated circuits (such as those produced by PMC-Sierra) are quite fast, even in T1 and E1 rate applications the designer should

take great care to ensure good signal integrity on the interconnections between components.

The most common signal integrity issue in such designs is signal reflection due to impedance mismatch. When the propagation time of a signal on an interconnection exceeds the edge rate, a feedback delay is created in the output driver causing an underdamped step response. This is seen as “ringing” on the signal edges, with corresponding overshoot and undershoot.

PMC-Sierra product inputs typically have an absolute maximum voltage rating of a diode drop (0.3V in case of COMET) above the power supply voltage and an absolute minimum voltage rating of a diode drop below ground. If these ratings are exceeded then the COMET is not guaranteed to operate correctly, in fact damage to the COMET may occur. Therefore it is essential that signal reflections be minimized so that the overshoot and undershoot do not violate these ratings.

Signal reflections are minimized by ensuring that load impedance are matched to the characteristic impedance of the interconnection. There are many techniques for doing this, and the topic is beyond the scope of this document.

In general, the series resistance termination scheme is recommended on all clock traces of over an inch in length. This scheme consists of placing a series resistor as close to the output pin as possible. The value of this resistor added to the output impedance of the driver should equal the characteristic impedance of the circuit board trace. No other termination resistors are required.

The COMET Reference Design (PMC-970624) uses series termination on some of its connections.

Although fast clock edges create issues of signal reflection, slow clock edges may be susceptible to noise. If power supply noise or signal noise coincides with a slow clock edge, the resulting glitch may cause the edge to cross the switching point more than once (i.e. the edge is not monotonic). If this occurs, then extra clock cycles will be detected by the COMET (or other device) causing a severe failure in signal integrity.

Although there are no set requirements for minimum rise and fall times on the COMET, it is recommended that if these times exceed 8ns then the signal should be buffered with a faster output driver. (Note that the faster output driver will likely require series termination.)

Q40) Is the COMET pin-compatible with the T1XC or E1XC?

A40) No. The COMET has many different interface enhancements that prevent it from being pin-compatible with PMC-Sierra's older T1/E1 products such as the T1XC and E1XC.

Some interface enhancements on the COMET are:

- JTAG port
- Revised transmit analog outputs that meet transmit return loss and that are tri-stateable
- 8.192 MHz MVIP backplane mode
- Transmit elastic store buffering
- Line rate high-speed clock, XCLK

However, designers who have used PMC-Sierra's T1XC and E1XC products will still find many portions of the COMET familiar.

Q41) What PQFP socket is recommended for prototyping with the COMET?

A41) The COMET comes in an 80-pin PQFP package option. For testing and prototyping with the COMET, PMC-Sierra used PQFP sockets from:

Yamaichi Electronics U.S.A., Inc.
2235 Zanker Road
San Jose, CA 95131
U.S.A.
Phone: (408) 456-0797
Fax: (408) 456-0799
Web site: http://www.yeu.com

Q42) What oscillator manufacturers does PMC-Sierra recommend for use with the COMET?

A42) Any reputable crystal oscillator manufacturer should be able to provide the required 1.544 MHz or 2.048 MHz oscillator to source the COMET XCLK input signal. Since this is a non-standard frequency, they will generally have to be custom cut. The 1100 series of custom-cut crystal oscillators is suitable and available from most manufacturers. The oscillator should output TTL (or TTL-compatible) levels.

Some manufacturers which PMC-Sierra has used in-house are: Champion Technologies, Connor-Winfeld, Ecliptek Corporation, and Fox Corporation. These should be available from most electronic component distributors.

Custom cut oscillators can have very long lead times (16 weeks typical) so they should be ordered well in advance of when they will be needed.

Q43) Do the COMET input clocks need to come from on-board oscillators?

A43) No. As long as the input clocks to the COMET meet the timing requirements specified in the COMET Data Book (PMC-970624), then it does not matter if the clock signal comes from an oscillator, a PLL, another logic device, or some other source.

In particular, clock inputs must meet:

- set-up and hold requirements with respect to associated with that clock;
- duty cycle requirements;
- frequency tolerance (in parts per million) if specified.

Q44) Can the COMET be damaged if the XCLK does not meet the minimum frequency requirement?

A44) No. During conditions where COMET XCLK does not meet the frequency requirements specified in the COMET Data Book (PMC-970624), the COMET cannot be guaranteed of operating properly. However, no damage will occur to the COMET during conditions where XCLK does not meet the frequency requirement.

5 NOTES

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