PM4351

COMET

COMET REFERENCE DESIGN REV. 2.0

ADVANCED

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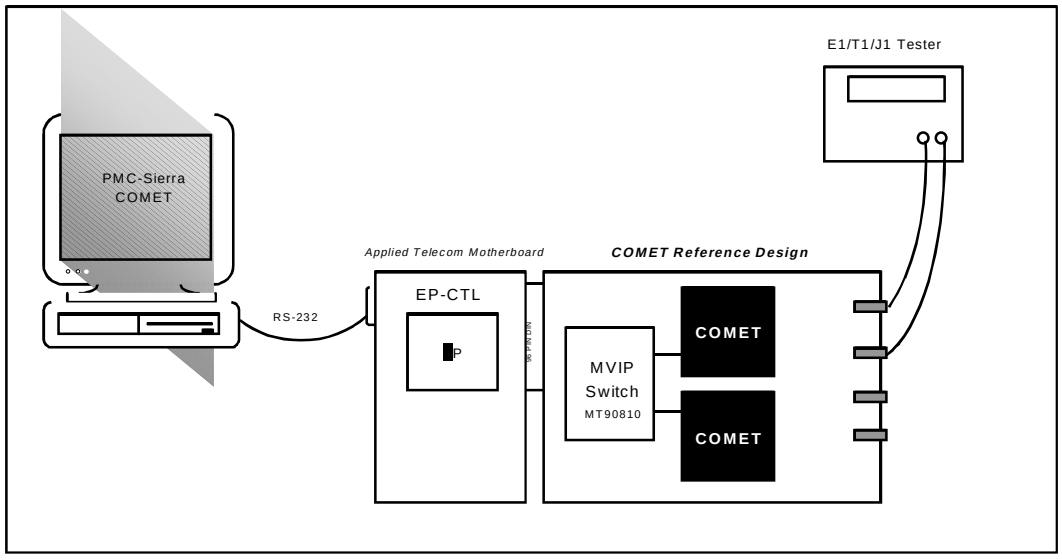
1 FEATURES

- A complete reference design of a dual channel, T1/E1/J1 switch card with an MVIP (Multi-Vendor Integration Protocol) interface.
- Two ports, each using a COMET device, provide framing and, line interface circuitry for short haul and long haul T1, E1, and J1 transmission rates.
- Provides a platform for the demonstration of the COMET's functions and performance.
- Provides a microprocessor Interface to Applied Telecom Evaluation motherboard (EP-CTL). The software drivers include the basic drivers available from PMC-Sierra and the Telecom Application Package (TAP) available from Applied Telecom. A GUI interface is provided for ease of operation.
- Provides a platform for V5.1/5.2 applications with third party application software.
- Provides a platform for ETS 300-011 E1 homologation and T1 testing to ANSI T1.403.
- Provides fractional N*DS0 backplane rates.
- Provides software-selectable E1, T1, J1 rate selection.
- Provides software-selectable backplane timing selection.
- Provides a programmable PRBS test patter generator, receiver and analyzer.
- Demonstrates protection circuitry that meets both ETS 300 046 and FCC part 68.

2 OVERVIEW

The COMET reference design allows for the evaluation and demonstration of the PMC-Sierra PM4351 COMET device. This reference design illustrates how to implement a dual channel, T1/E1/J1 switch card, with an MVIP interface, using two COMET devices. This board is designed to interface with an Applied Telecom evaluator module (EP-CTL) to form a complete reference design. A graphical user interface, along with the COMET software drivers, are provided for operation of the reference design. Software is also provided for operation of the Mitel 8986 digital switch. All required decoding logic is provided on the COMET reference board to give the Applied Telecom's evaluator module direct access to all registers of both COMET devices. The Applied Telecom evaluator interfaces to a PC directly through an RS-232 connector.

Figure 1: COMET Reference System



The COMET reference design includes two COMET devices, an MVIP bus switch, analog line circuitry and a microprocessor interface to the Applied Telecom Evaluator. The MVIP standard specifies a common bus interface for network, telephony, voice, and fax device interconnection. The backplane signals from the two COMET devices are connected to a Mitel 8986 Digital Switch for support of distributed switching as defined in MVIP-90 standard. The COMET reference design illustrates the COMET's MVIP compatibility. MVIP-90 specifies that for a MVIP switching compatible board, the switch must be capable of making full-duplex connections and of connecting any incoming network channel

to some sub-set of the MVIP bus time-slots, together with the ability to drive any outgoing network channel from some set of MVIP time-slots.

The COMET reference design, together with the ATI Evaluation Motherboard, can be used to demonstrate V5.1/V5.2 applications. The ATI Evaluation Motherboard and Application Program Interface (API) provide access to COMET's three HDLC controllers for data processing. Investigations on software tools for V5.1/V5.2 applications for the demonstration of protocol handling and system management are now underway.

The COMET reference design board is configured, monitored, and powered through an edge connector that is designed to mate with an Applied Telecom evaluator module. Software drivers and API are available from Applied Telecom to fully control and utilize the COMET reference design.

2.1 Applications

The COMET reference design is suitable in the following applications

- T1/E1 Wireless Cellular Base Transceiver Stations (BTS)
- T1/E1 Internet Access Equipment
- T1/E1 Channel Service Units (CSU)
- V5.1/V5.2 Interface Applications

Figure 2 illustrates the COMET reference design in a wireless base transceiver station (BTS) application. The COMET reference design represents a line card which processes the incoming and outgoing E1 or T1 data signal in a MVIP system. The backplane data signal are input into the MVIP switch and can be switched on a DS0 time slot basis. Since the MVIP switch does not provide a multiplexer/demultiplexer function, an external multiplexer/demultiplexer is needed to transfer 64Kbps data from and to the cell site. The MVIP bus data rates can be set to 2.048, 4.096 or 8.192 Mbps depending on the application.

Figure 2: Wireless Application

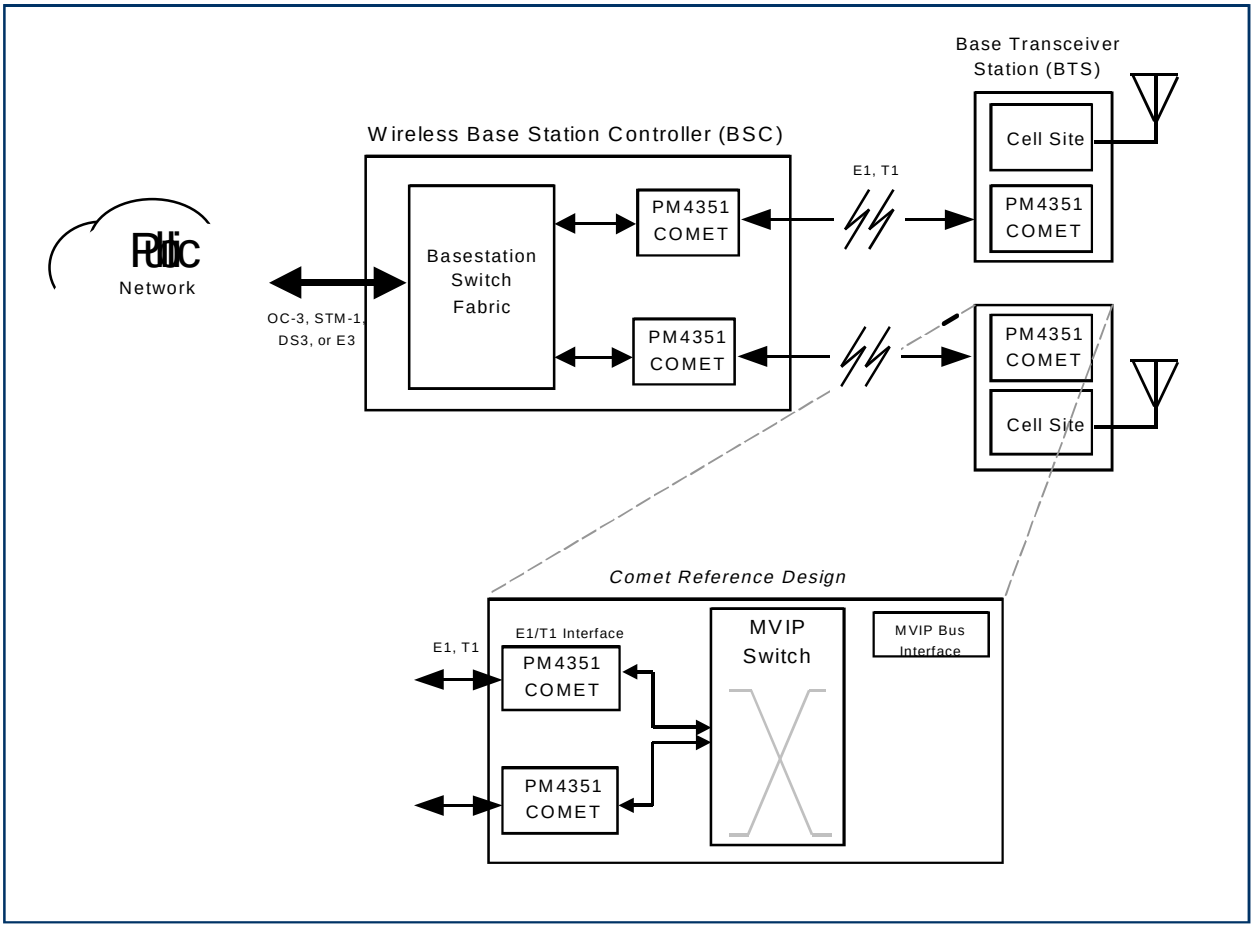
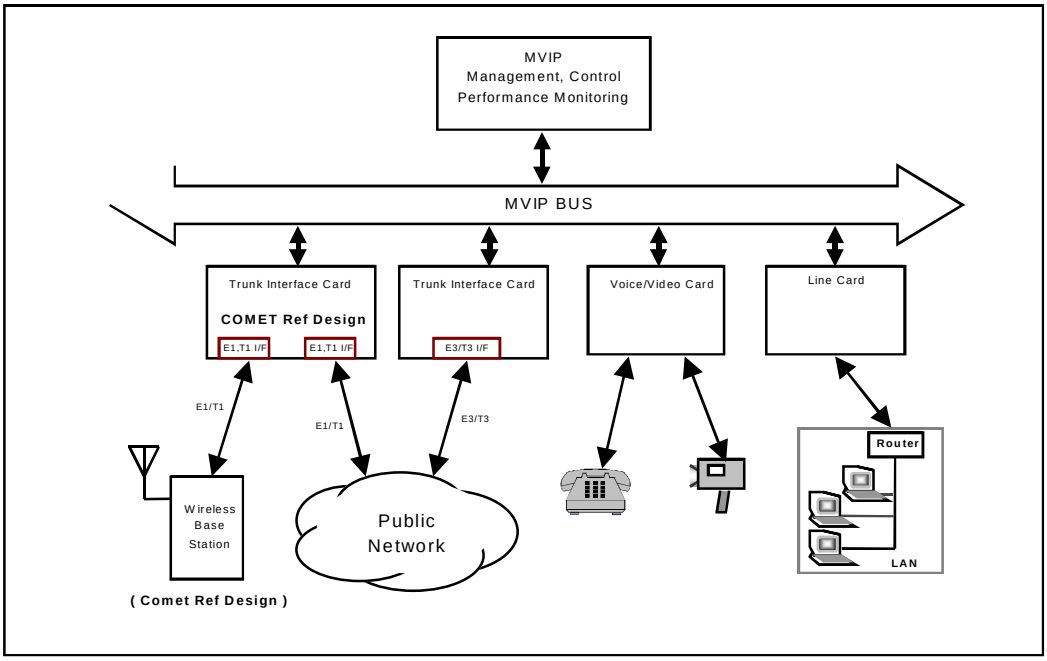


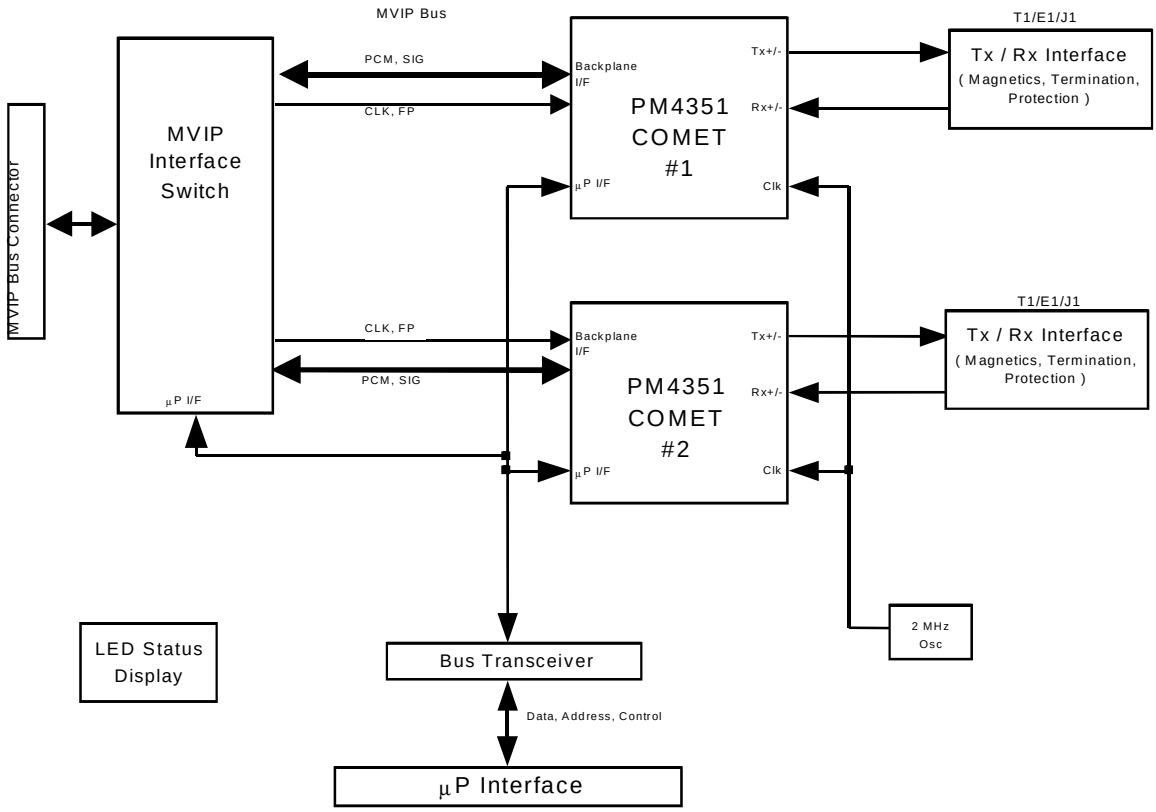
Figure 3 shows a MVIP bus switching system architecture. The COMET reference board can be used to interface to a BTS or to the public network at T1, E1, or J1 data rates.

Figure 3: MVIP Bus Architecure



3 FUNCTIONAL DESCRIPTION

Figure 4: Block Diagram



3.1 COMET

The PM4351 Combined E1/T1/J1 Transceiver (COMET) is a feature-rich monolithic integrated circuit suitable for use in long haul and short haul T1, E1, and J1 systems with a minimum of external circuitry. The COMET is software configurable, allowing feature selection without changes to external wiring.

Analog circuitry is provided to allow direct reception of long haul E1 and T1 compatible signals with up to 43 dB cable loss (at 1.024 MHz in E1 mode) or up to 36 dB cable loss (at 772 kHz in T1 mode) using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required. Digital line inputs are provided for applications not requiring a physical T1 or E1 interface.

The COMET recovers clock and data from the line and frames to incoming data. In T1 mode, it can frame to several DS-1 signal formats: SF, ESF, T1DM (DDS) and SLC®96. In E1 mode, the COMET frames to basic G.704 E1 signals and CRC-4 multiframe alignment signals, and automatically performs the G.706 interworking procedure. AMI, HDB3 and B8ZS line codes are supported.

The COMET supports detection of various alarm conditions such as loss of signal, pulse density violation, Red alarm, Yellow alarm, and AIS alarm in T1 mode and loss of signal, loss of frame, loss of signaling multiframe and loss of CRC multiframe in E1 mode. The COMET also supports reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and time slot 16 alarm indication signal in E1 mode. The presence of Yellow and AIS patterns in T1 mode and remote alarm and AIS patterns in E1 mode is detected and indicated. In T1 mode, the COMET integrates Yellow, Red, and AIS alarms as per industry specifications. In E1 mode, the COMET integrates Red and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events is provided in T1 mode. In E1 mode, CRC-4 errors, far end block errors, framing bit errors, and line code violation are monitored and accumulated.

Dual (transmit and receive) elastic stores for slip buffering and rate adaptation to backplane timing are provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

In T1 mode, the COMET generates framing for SF, ESF and T1DM (DDS) formats. In E1 mode, the COMET generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled.

Internal analog circuitry allows direct transmission of long haul and short haul T1 and E1 compatible signals using a minimum of external components. Typically, only line protection, a transformer and an optional line termination resistor are required. Digitally programmable pulse shaping allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect, E1 short haul pulses into 120 ohm twisted pair or 75 ohm coaxial cable, E1 long haul pulses into 120 ohm twisted pair as well as long haul DS-1 pulses into 100 ohm twisted pair with integrated support for Line Build Out (LBO) filtering as required by the FCC rules. In addition, the programmable pulse shape extending over 5-bit periods allows customization of short haul and long haul line interface circuits to

application requirements. Digital line inputs and outputs are provided for applications not requiring a physical T1 or E1 interface.

In the transmit path, the COMET supports signaling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per-channel basis. Zero code suppression may be configured to Bell (bit 7), GTE, or DDS standards, and can also be disabled. Transmit side data and signaling trunk conditioning is also provided. Signaling bit transparency from the backplane may be enabled.

The COMET provides three transmit HDLC controllers. These controllers may be used for the transmission of messages on the ESF data link (T1) or national use bits (E1) and in any time slot. In T1 mode, the COMET can be configured to generate in-band loop back codes and ESF bit oriented codes. In E1 mode, transmission of the 4-bit Sa codewords defined in ETSI 300-233 is supported.

The COMET provides optional jitter attenuation in both the transmit and receive directions.

The COMET provides both a parallel microprocessor interface for controlling the operation of the device and serial PCM interfaces that allow backplane rates from 1.544 Mbit/s to 8.192 Mbit/s to be directly supported. Up to four COMET devices can be multiplexed on a byte-interleaved basis on a common bus with no additional arbitration logic. The COMET supports the Mitel ST® bus, AT&T CHI® and MVIP standards.

For a complete description of the COMET, please refer to PMC-Sierra's COMET databook, PMC-970624.

3.2 MT90810 Flexible MVIP Interface Circuit (FMIC)

The Mitel MT90810 FMIC provides a MVIP interface between the MVIP system bus and different variety of processors, telephony and communication interfaces. The MT90810's built-in digital time-slot switch provides MVIP Enhanced Switching between the MVIP system bus and any combination of up to 128 full duplex local channels of 64kb/s each. The MT90810's local serial interface supports PMC rates of 2.048, 4.096, and 8.192 Mb/s.

The MT90810 takes in two 8KHz recovered clocks from the two COMET devices and selects one of the two to generate a 8.192 MHz clock. This 8.192 MHz is synchronized to the selected COMET's receive line. The MT90810 then supplies

the 8 MHz clock to the receive and transmit backplane clocks (BTCLK, BRCLK) of both COMET devices. This ensures the three devices are all synchronized to one clock. The MT90810 also generates a 8KHz frame pulse signal for the two COMET devices.

The MT90810 provides an interface to 4 pairs of input and output local streams. For this reference design, the four local streams include BTPCM, BTSIG, BRPCM, and BRSIG as two stream pairs for each COMET device. The MT90810 is configured and setup through a 8-bit microprocessor interface from the ATI controller motherboard.

3.3 Bus Transceiver

Bus Transceivers are provided at the ATI connector interface to prevent excessive loading of the ATI's Evaluation Motherboard.

3.4 Oscillators

The COMET can run in both T1 or E1 modes. To run in T1 mode, oscillator Y1 should be populated with a 1.544 Mhz oscillator. To run in E1 mode, oscillator Y1 should be populated with a 2.048 Mhz oscillator.

3.5 Transmit and Receive Line Interface

The transmit and receive line interface consists of line connectors, line protection circuitry and magnetics. The reference board provides two types of interface connectors, a mini-bantam and RJ-48C. The RJ48C has been provided according to the ANSI T1.403 standard for a Universal Service Ordering Code (USOC) connector. The line interface provides one termination scheme for both T1 and E1 rates. A termination of 110Ω is used to allow the interface to be compatible with both T1 and E1. This provides a software switchable reference board for both T1 and E1 by simply configuring the COMET device.

The protection circuitry prevents overvoltage and overcurrent power surge due to lighting strikes or other power impairments, and meets both ETS 300 046 and FCC Part 68 requirements.

3.6 Power Supply

The COMET reference design contains components that operate at either 3.3V or 5V, referenced to the ground. The Applied Telecom's Evaluator provides

power to the COMET reference board through the edge DIN connector. The 5V power is converted into 3.3V using a DC-DC voltage regulator.

It is recommended that 5.0V power is provided before 3.3V power to avoid latchup in 5.0V tolerant systems. Please refer to the COMET datasheet for further details steps of powering up the COMET device.

3.7 MVIP Bus Connector

The MVIP bus connector provides an interface to the MVIP system bus. The MVIP bus consists of sixteen 2.048 Mbit/s serial data streams (DSi0-7 and DSo0-7), clocking, and framing signals. Clocks /C4 and C2 are 4.096 and 2.048 MHz clocks respectively. Frame pulse /F0 is the MVIP 8KHz framing signal. SEC8K is a secondary 8 kHz signal line used to carry 8 kHz timing information derived from trunks on a secondary or subsequent digital trunk interface. The connector is a 20x2 40 pin shroud header.

Table 1 : MVIP Bus Connector Pin Assignments

Pin Number	Pin Name	Pin Number	Pin Name
1	Reserved	2	Reserved
3	Reserved	4	Reserved
5	Reserved	6	Reserved
7	DSo0	8	DSi0
9	DSo1	10	DSi1
11	DSo2	12	DSi2
13	DSo3	14	DSi3
15	DSo4	16	DSi4
17	DSo5	18	DSi5
19	DSo6	20	DSi6
21	DSo7	22	DSi7
23	Reserved	24	Reserved
25	Reserved	26	Reserved
27	Reserved	28	Reserved

Pin Number	Pin Name	Pin Number	Pin Name
29	Reserved	30	Ground
31	/C4	32	Ground
33	/F0	34	Ground
35	C2	36	Ground
37	SEC8K	38	Ground
39	Reserved	40	Reserved

3.8 Microprocessor Interface Connector

The microprocessor interface to Applied Telecom's evaluator is a 96 pin DIN edge connector. Table 1 describes the signals and pin designations of the microprocessor connector.

Table 2 : Microprocessor Interface Connector

Pin Name	Type	Pin No.	Function
CS0	Input	A25	Chip Select for COMET #1
CS1	Input	A26	Chip Select for COMET # 2
CS2	Input	A27	Chip Select for the MVIP Switch
RSTB	Input	C2	Reset Pin for COMET and MVIP Switch RSTB is an active low asynchronous hardware reset
WRB	Input	C3	Write Strobe. WRB is an active low signal that asserts during a register write to any of the COMET or MVIP devices
RDB	Input	C4	Read Strobe. RDB is an active low signal that asserts during a register read from any of the COMET or MVIP devices

Pin Name	Type	Pin No.	Function
ALE	Input	C5	Address Latch Enable. ALE is an active high address latch enable and latches the address bus when low.
IRQ1B	Input	C6	Interrupt Signal. IRQ1B is active low maskable hardware interrupt. IRQ1B goes low when any of the three devices interrupt source is active
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	Input / Output	C9 C10 C11 C12 C13 C14 C15 C16	Data Bus. D[7:0] is an eight-bit bi-directional data bus used for microprocessor read and write access
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8]	Input	C17 C18 C19 C20 C21 C22 C23 C24 C25	Address Bus. A[8:0] is a nine bit address bus that selects specific registers during microprocessor access
VCC	Power	B27 B28 B29 B30 B31 B32	+5V Power Supply from the Evaluation Motherboard
Ground	Power	B1 to B26	Ground

4 IMPLEMENTATION DESCRIPTION

The COMET reference design schematics were captured using Cadence software Concept Schematics Capture tool.

4.1 ROOT DRAWING, Sheet 1

This sheet provides an overview of the major functional blocks of the COMET reference design. It shows interconnections between the COMET_BLOCK1, COMET_BLOCK2, BACKPLANE_BLOCK, LINE_INTERFACE, SYS_TIMING, and MICRO_INTERFACE blocks. Groups of signals have been combined into a bus type name format even though these signals are not typically made into buses. This is done to make the schematic less cluttered and more readable and to utilize the capabilities of the schematic capture tool. An example of such signals are the B_CLK<3..0>, B_FP<3..0> and SYS_CLK<3..0>.

4.2 COMET BLOCK, Sheet 2 & 3

This sheet shows the COMET device and its power circuitry. The power circuitry includes a schottky diode for protection while powering up the COMET device and separate filtering circuitry for the analog and digital power pins. The analog power circuitry consists of decoupling capacitors and ferrite beads. For digital power circuitry, ferrite beads are not recommended because of fast CMOS switching of digital I/O's.

4.3 BACKPLANE BLOCK, Sheet 4

The backplane block schematics shows the MVIP Interface Switch (MT90810) with an external header. A buffer is provided to buffer the clock and frame pulse to the backplane of the two COMET devices. The clock filtering circuitry ensures the correct operation of the PLL inside the MVIP Interface Switch. Jumpers are provided to optional select termination for the C2 and /C4 clock lines. When connecting two COMET reference boards together, the slave COMET board needs to terminate the clock lines. A 20x2 header allows two COMET reference boards to be connected via a ribbon cable.

4.4 LINE INTERFACE, Sheet 5

This schematics shows the termination, magnetic and protection circuitry for the line interface. A 1:2.42 transformer is used to couple the COMET transmit and receive line to the connectors. The LC01-6 transient voltage suppressor (TVS)

and the Raychem PTC provides over voltage protection. A common-mode choke is used on the transmit side for reducing electromagnetic noise. A single footprint is provided for both the bantam and RJ48C connectors.

4.5 SYS TIMING, Sheet 6

The 2.048 MHz or 1.544 MHz clock for the two COMET devices is buffered through a 8-bit buffer. The clock lines are series terminated to reduce reflection and bouncing.

4.6 MICRO INTERFACE, Sheet 7

This schematics shows the connector to the ATI EP-CTL and buffers for the microprocessor signals. The LM3940 drop-out voltage regulator supplies 3.3V to the two COMET devices. Two LED's are provided to display the status of power supply to the COMET board.

5 SCHEMATICS

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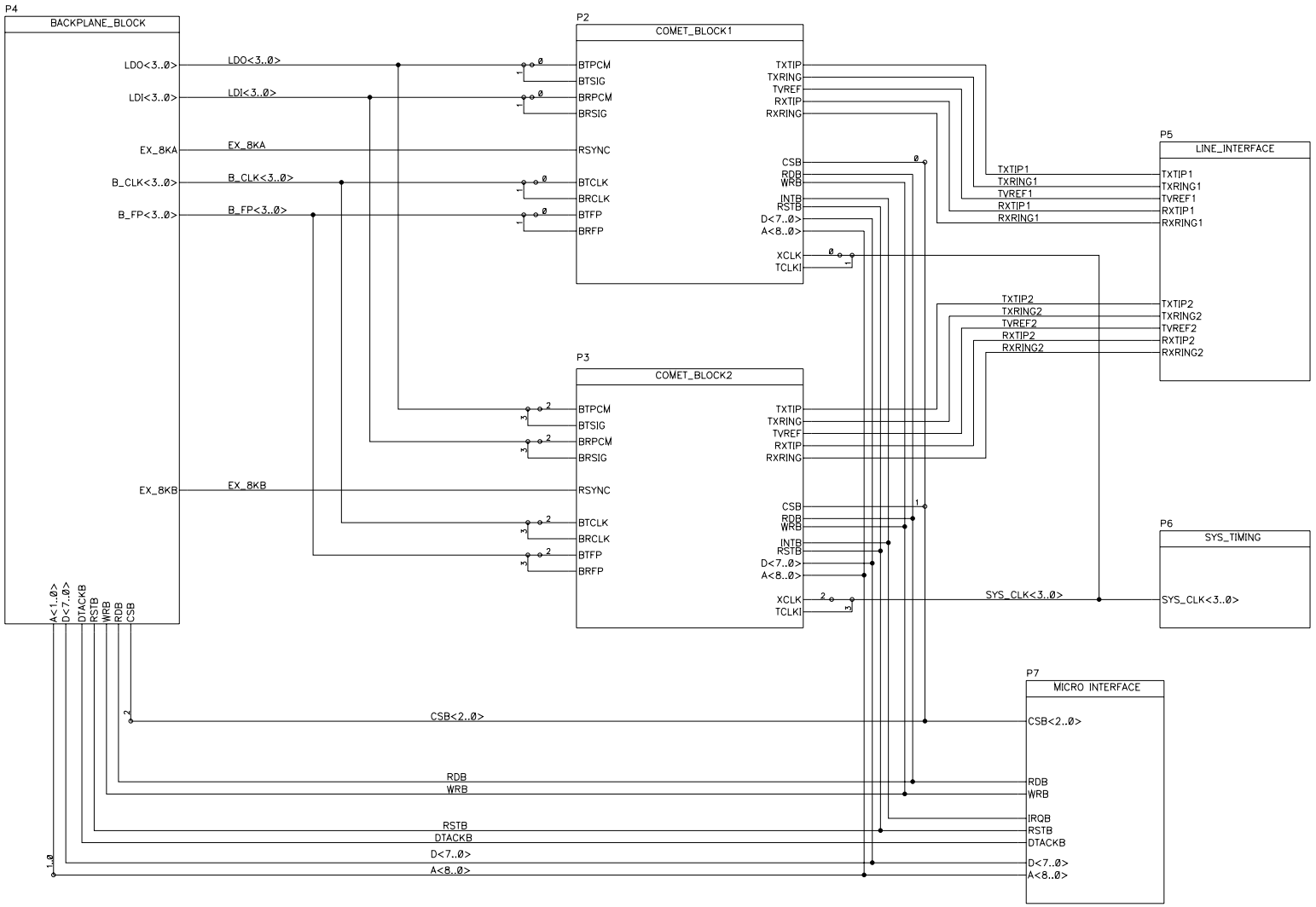

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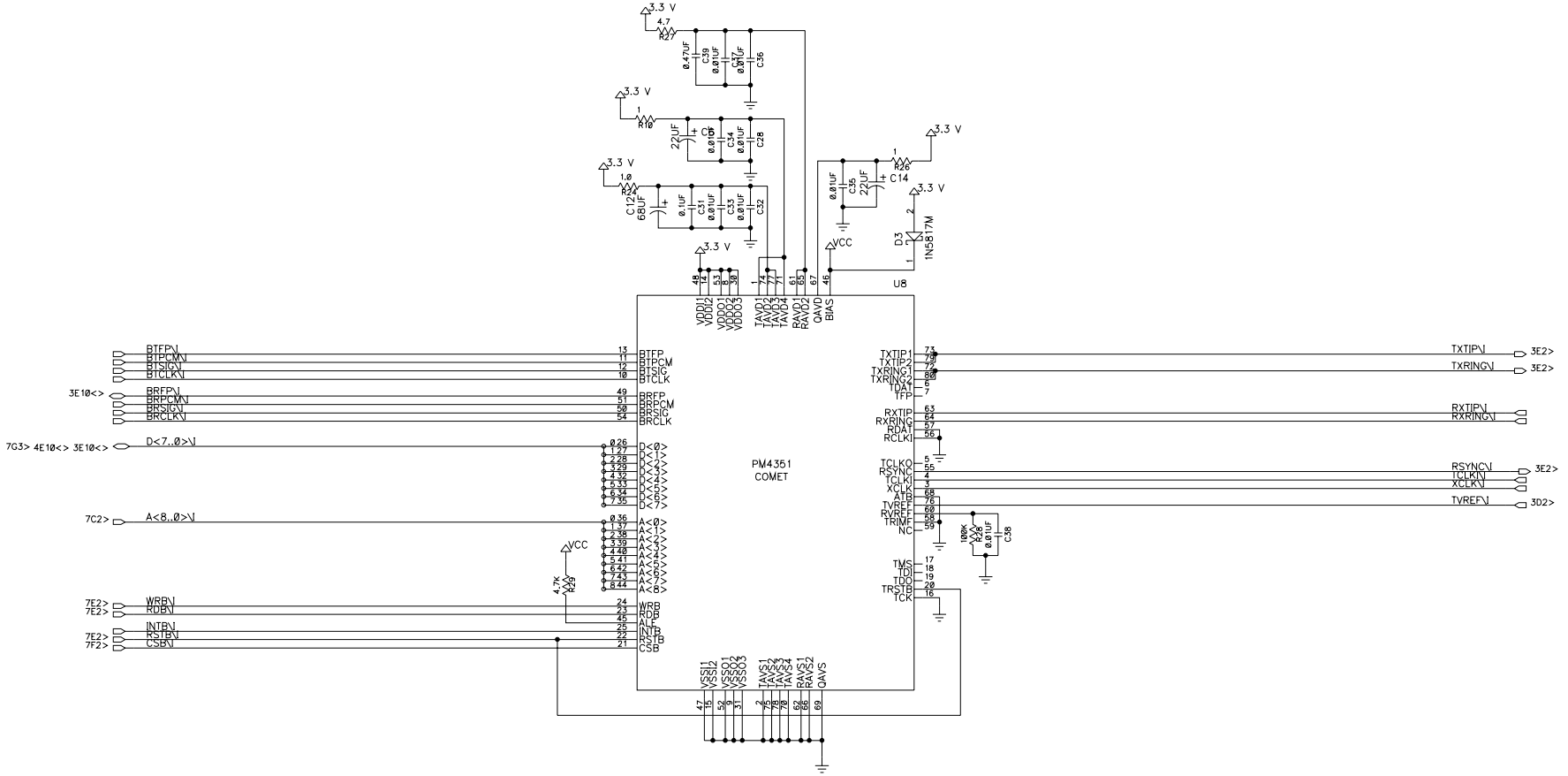

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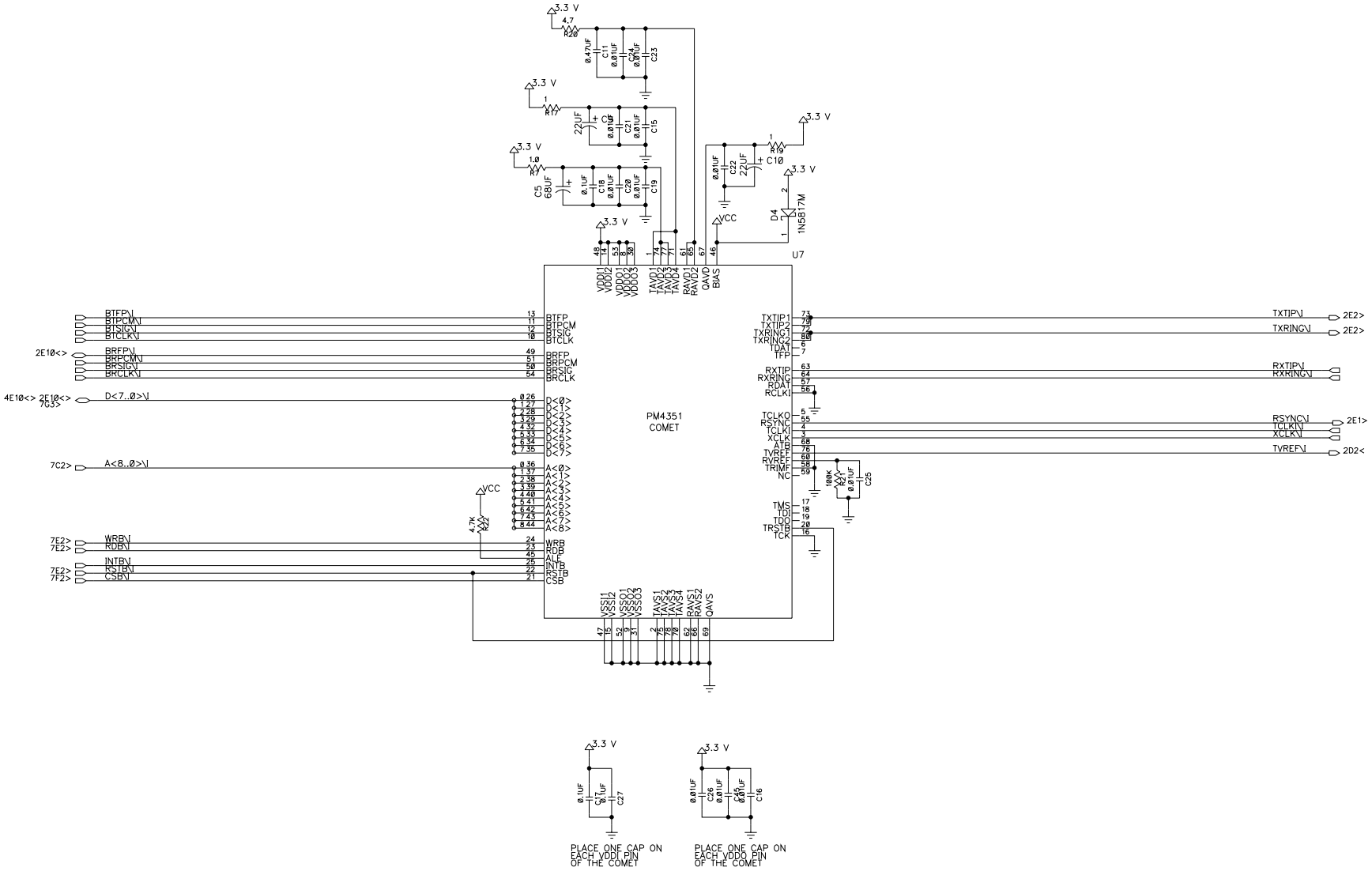

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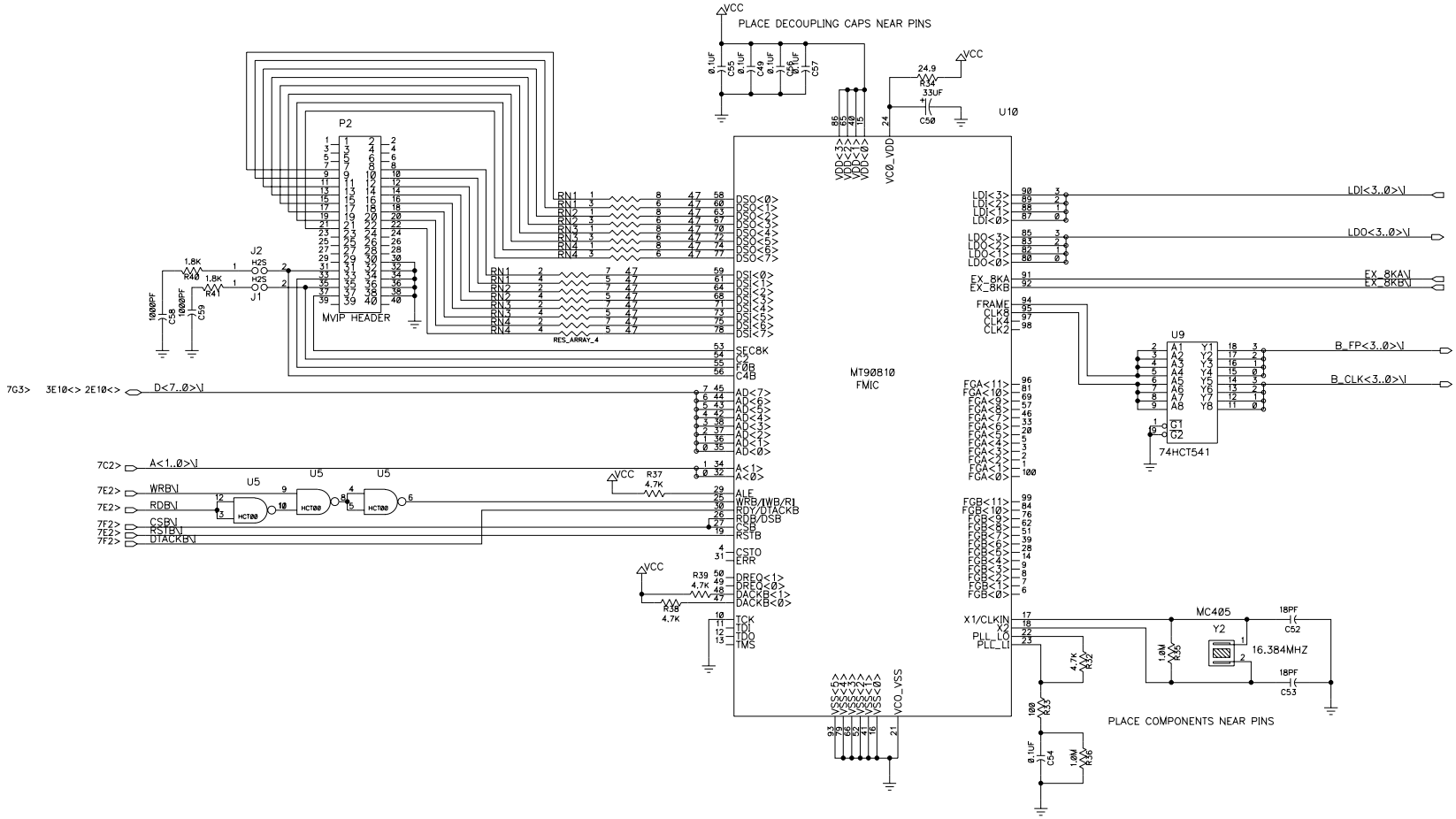

CONNECT UNUSED PINS TO GROUND

PLACE DECOUPLING CAPS NEAR IC

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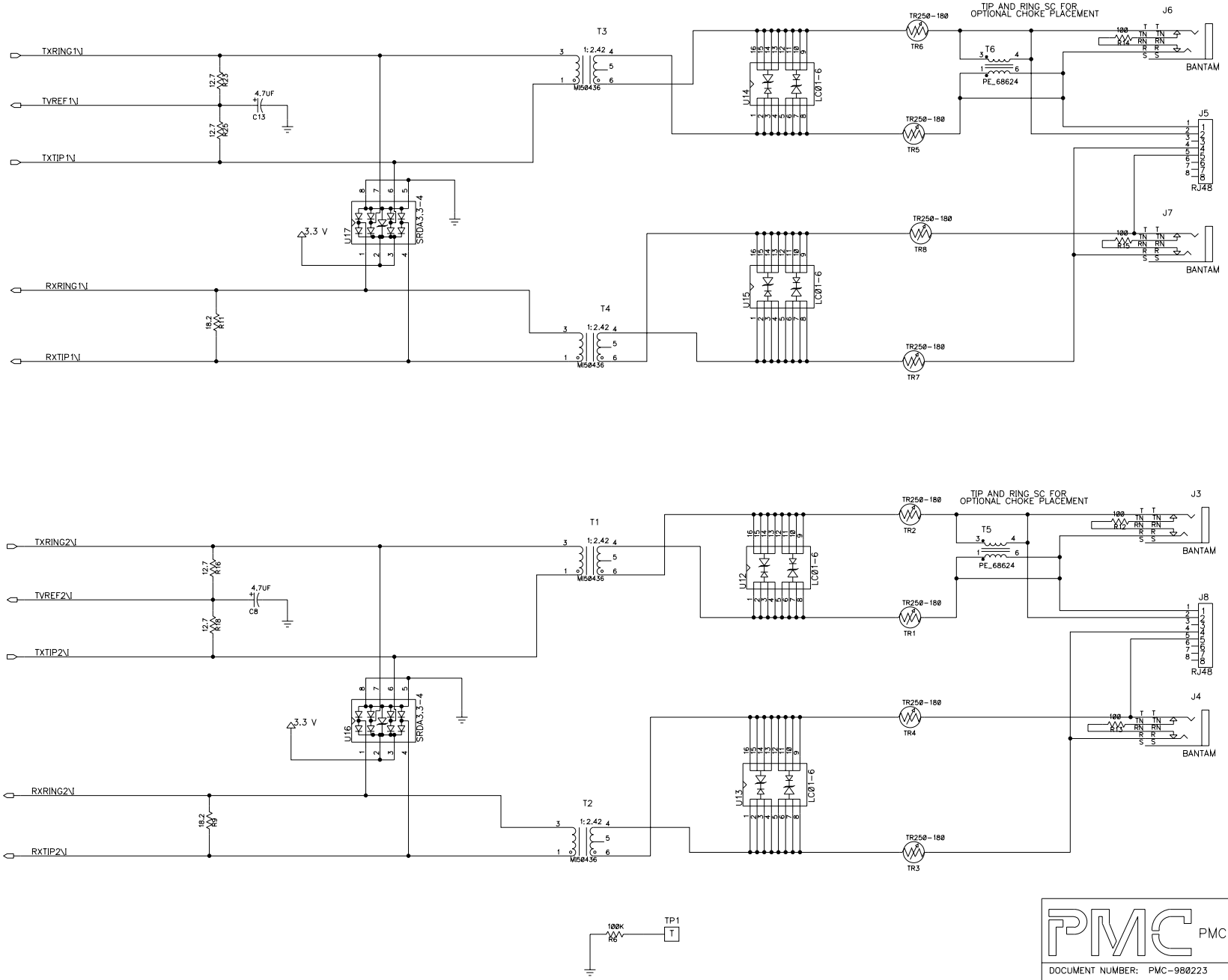

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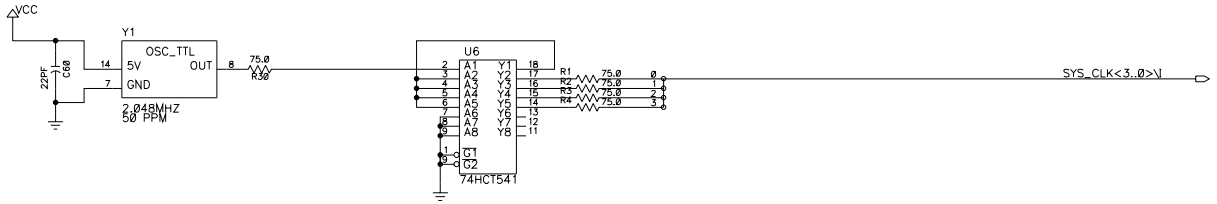
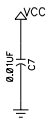


PLACE CAPACITORS CLOSE TO PINS



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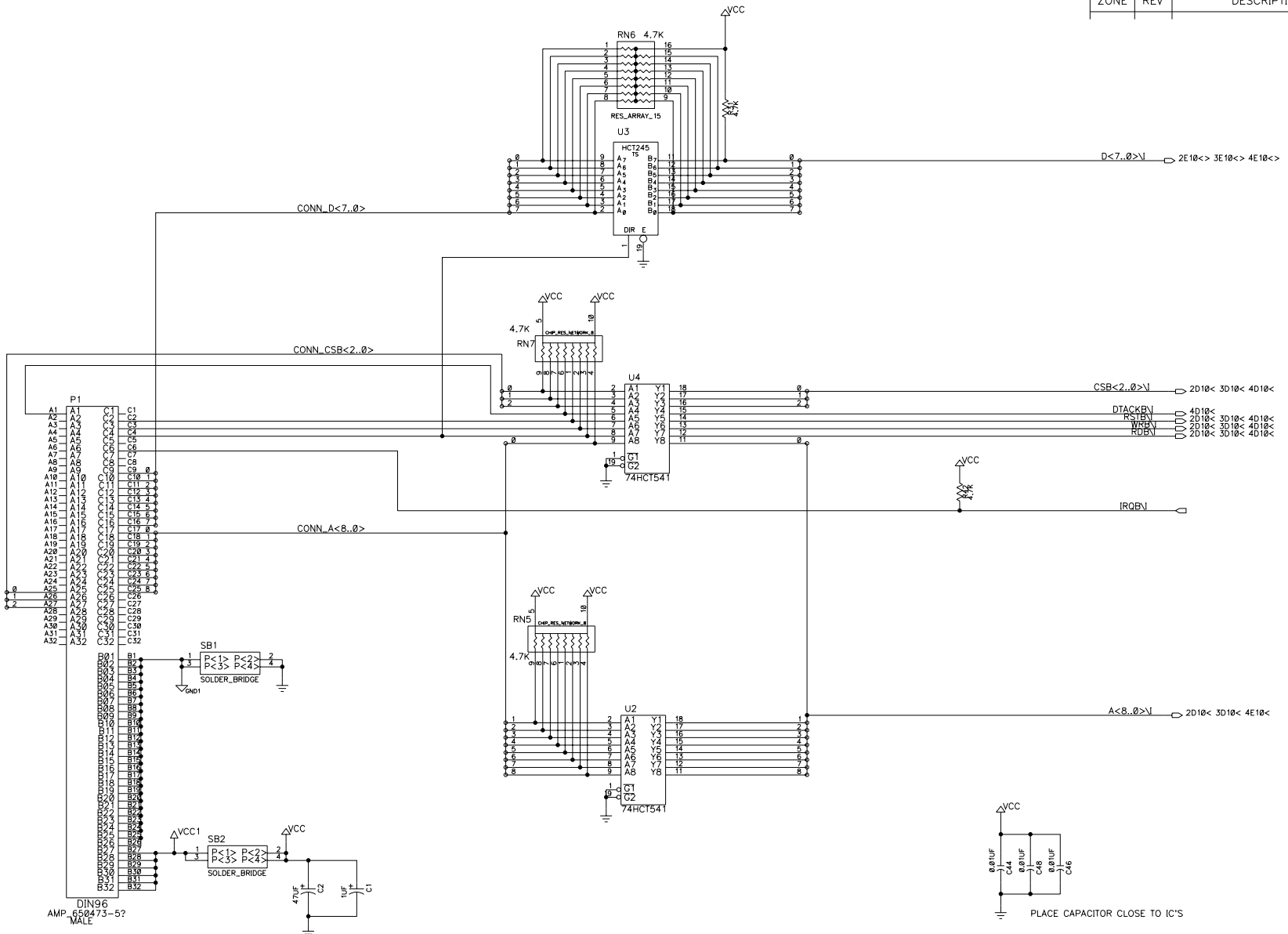

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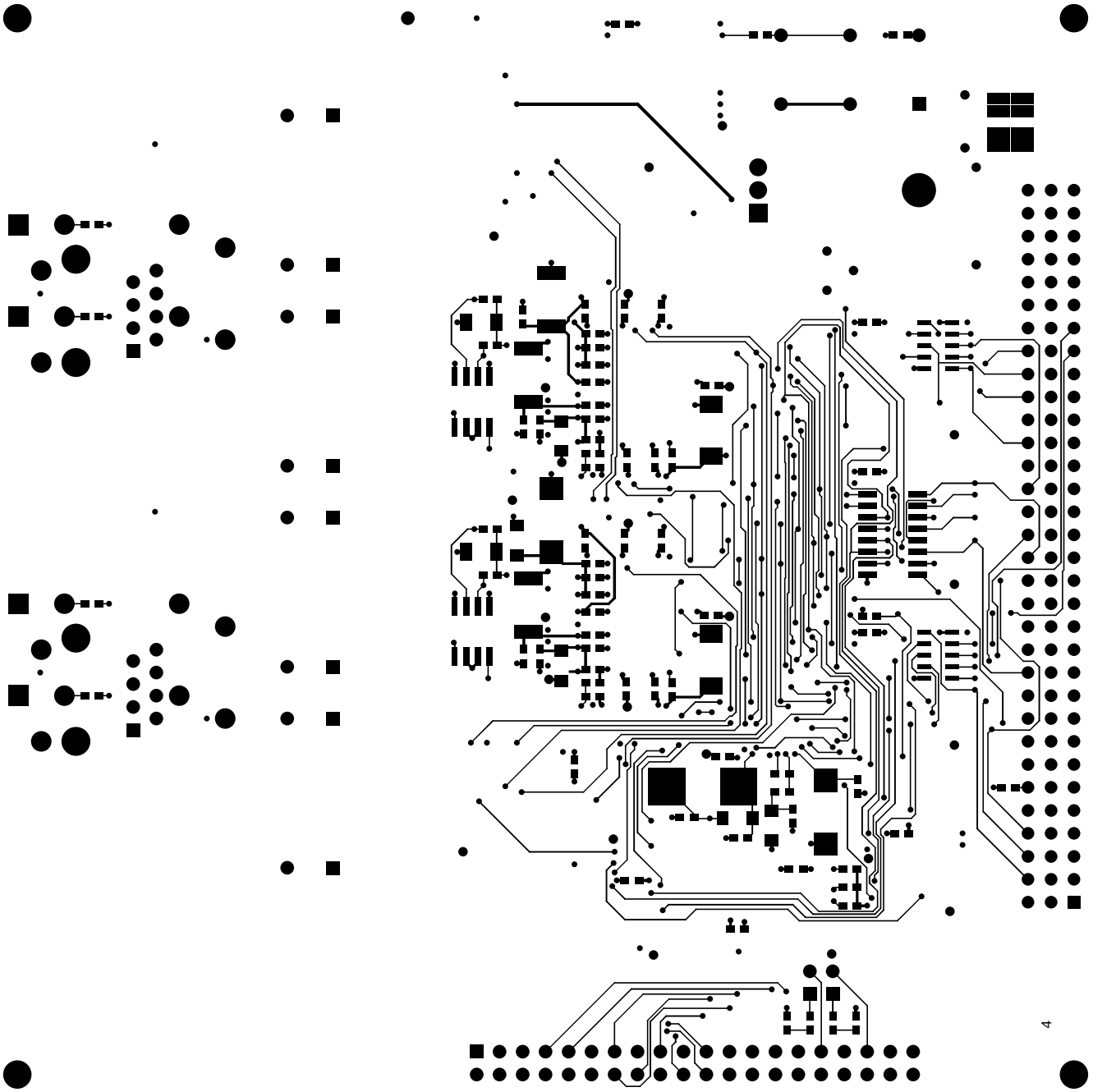
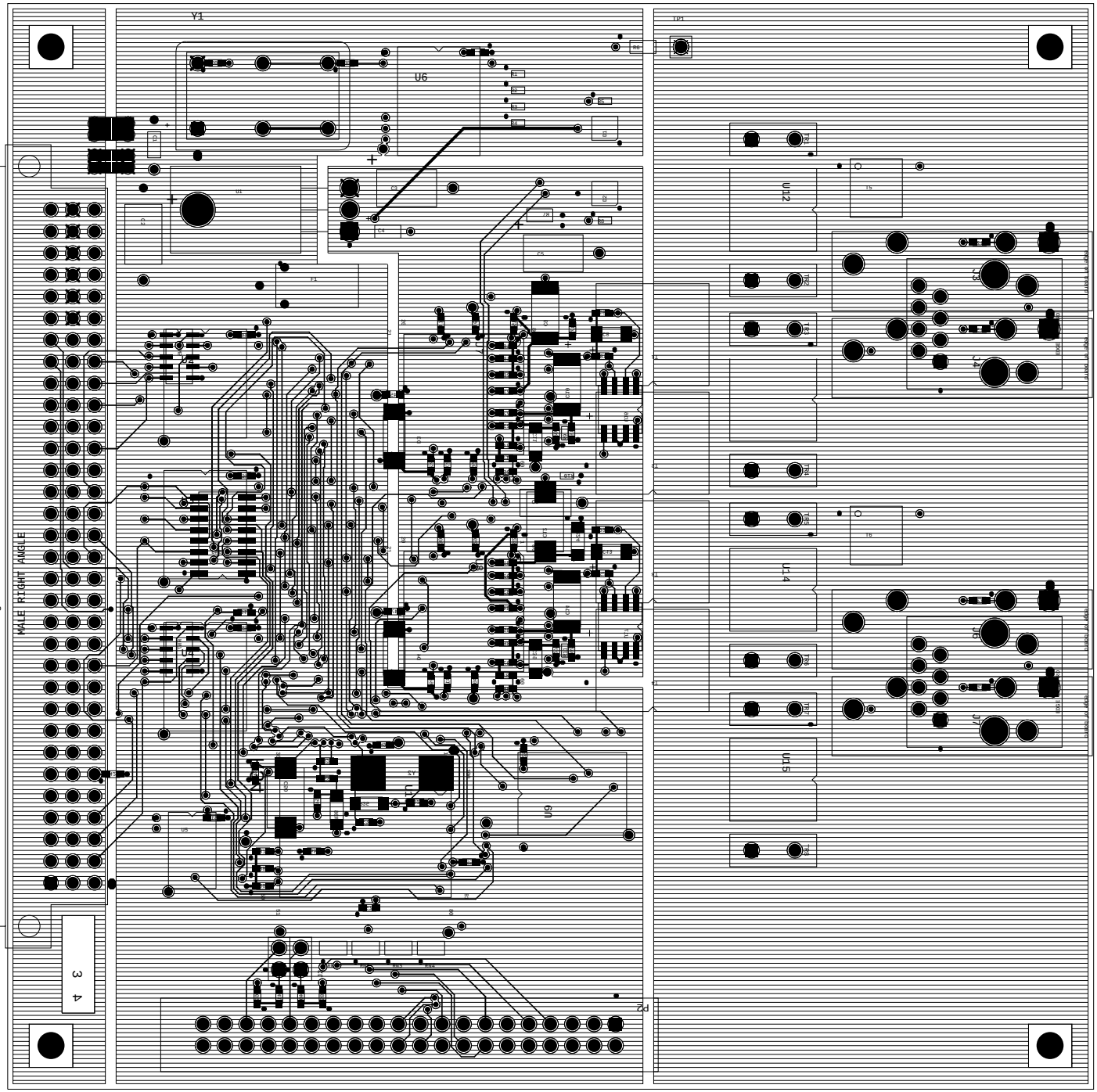


COMP TOP

COMP BOTTOM

VCC PLANE

BOTTOM LAYER



PMC-SIERRA COMET REFERENCE DESIGN REV.2.0 1998

PMC-SIERRA COMET REFERENCE DESIGN REV.2.0 1998

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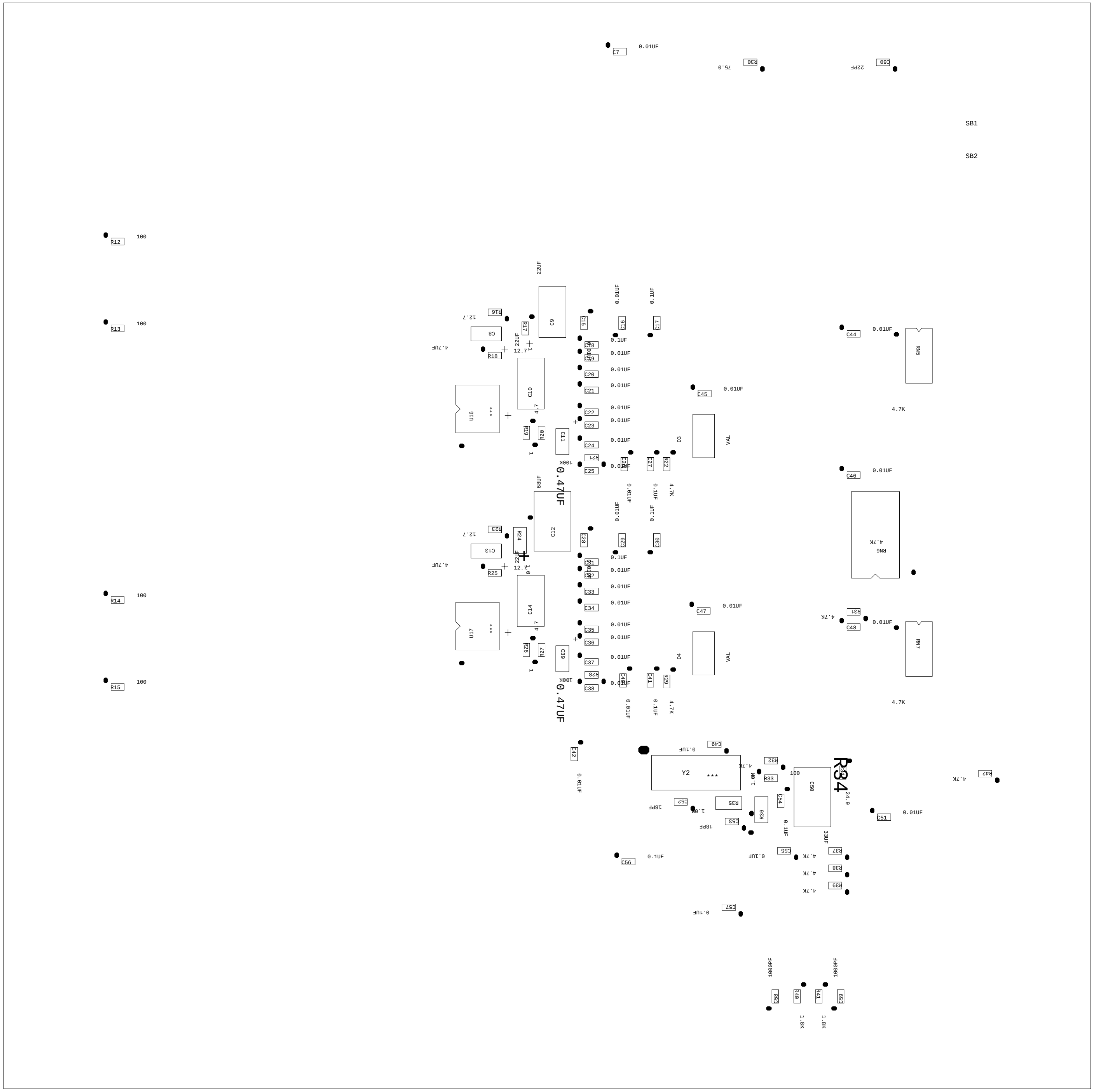

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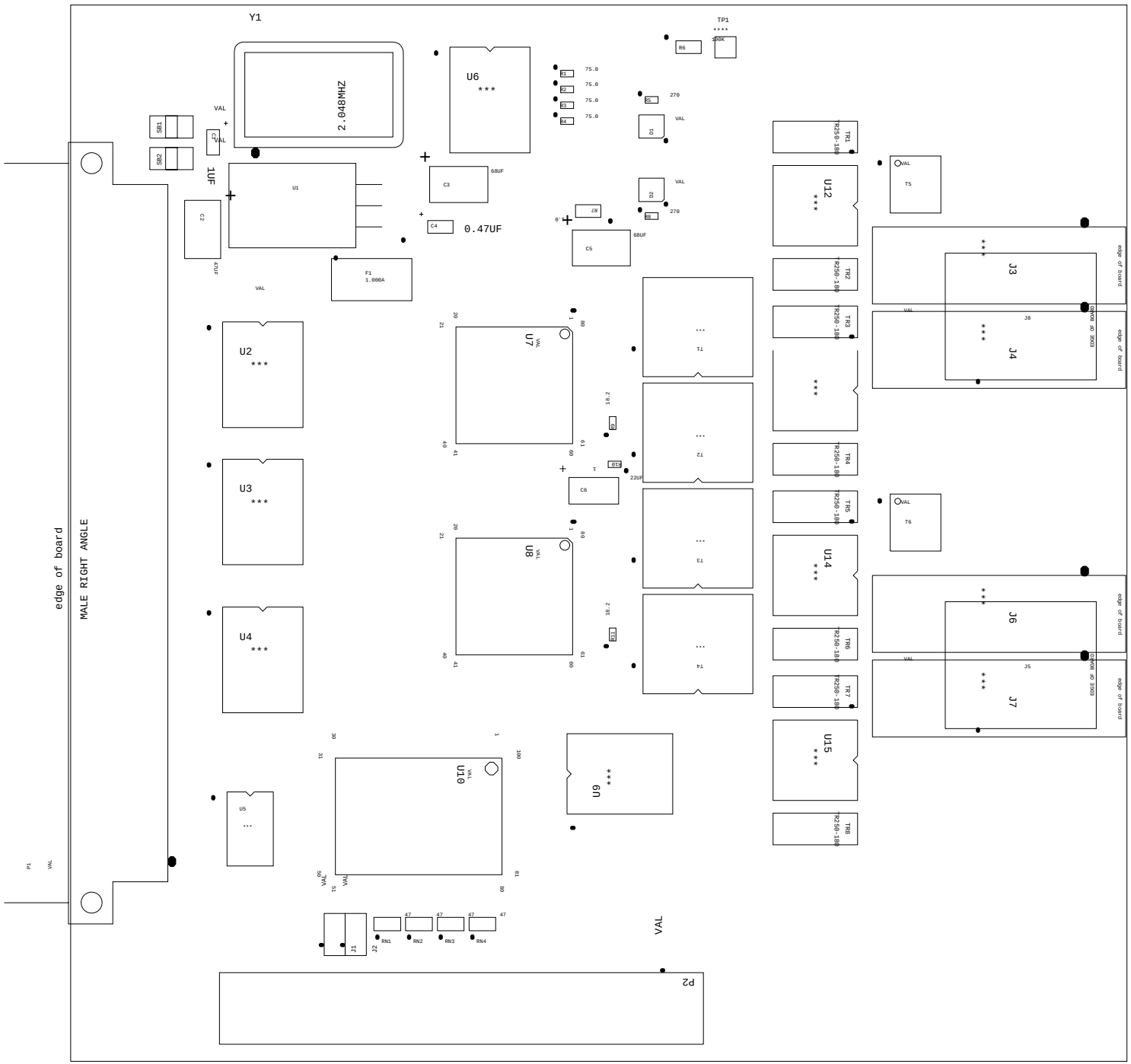
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2.048MHZ
TP1
U6
U1
U2
U3
U4
U5
U7
U8
U9
U10
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U15
J3
J4
J6
J7
J8
J5
P2
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T2
T3
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C5
C6
1UF
0.47UF
68UF
22UF
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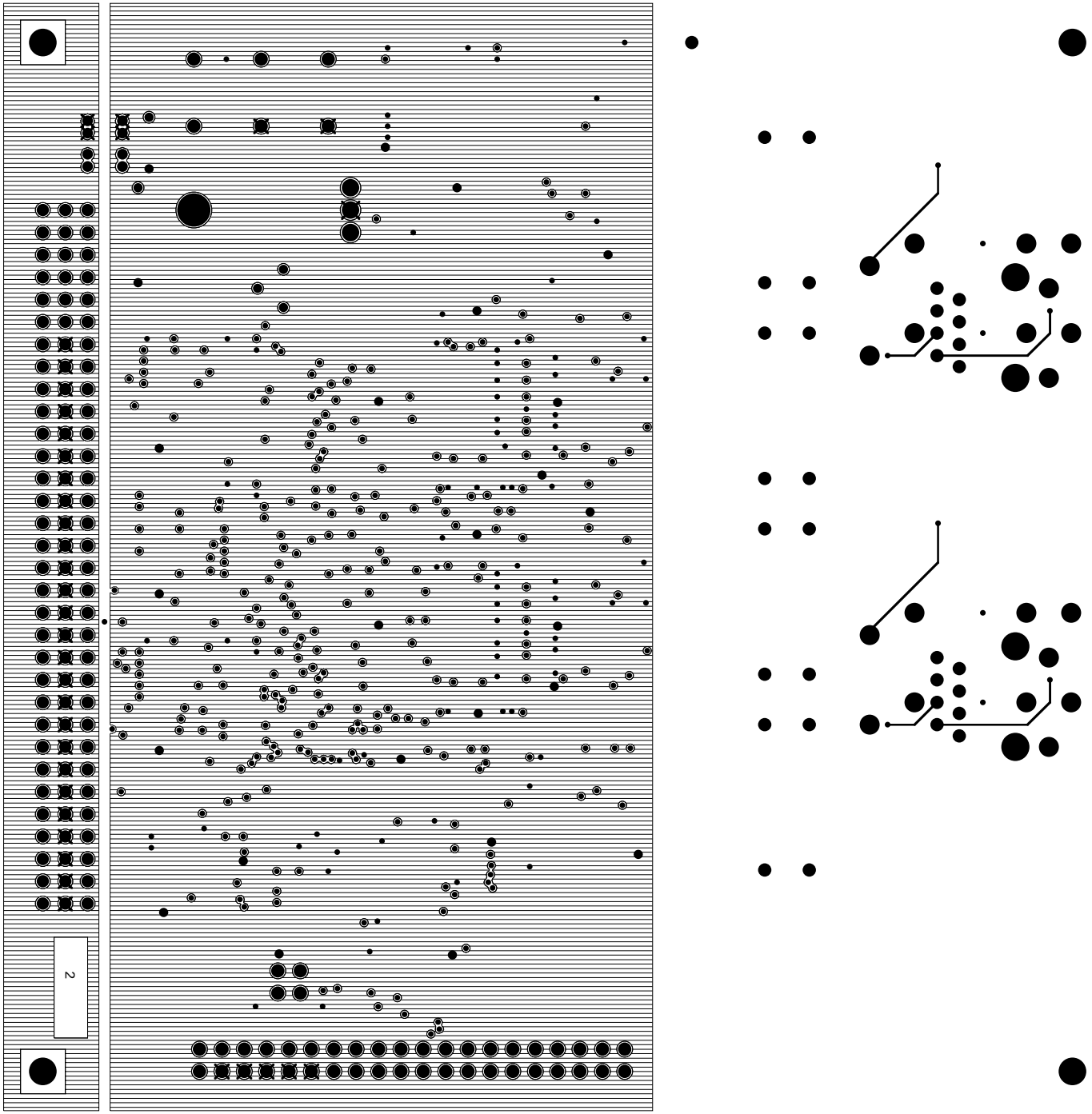
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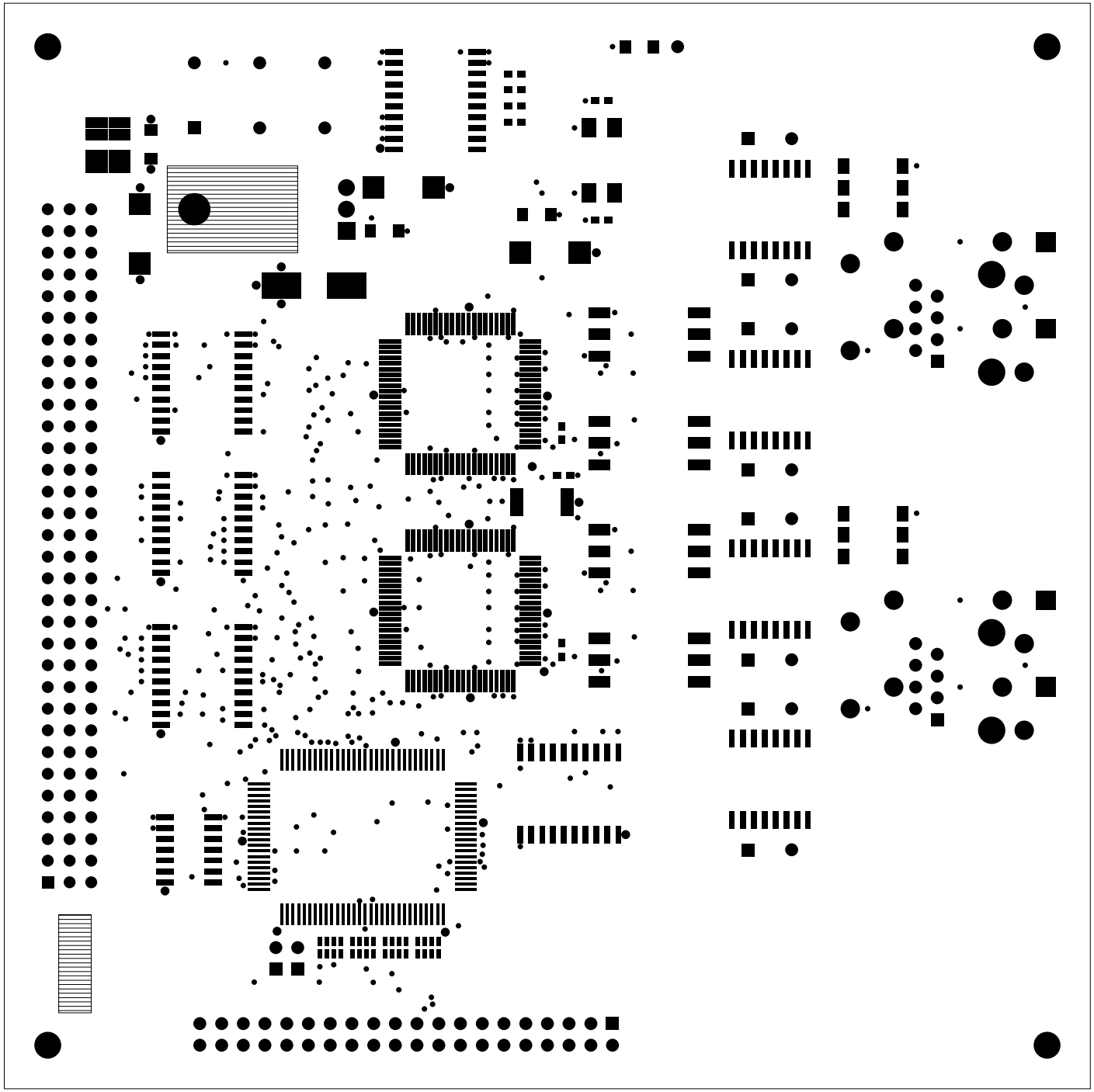


	Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
#	COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	--------
	FR-4	DIELECTRIC	--------	--------	7.0 mil	
	COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	--------
	FR-4	DIELECTRIC	--------	--------	44.0 mil	
	COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	1.44 mil	--------
	FR-4	DIELECTRIC	--------	--------	7.0 mil	
#	COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	--------

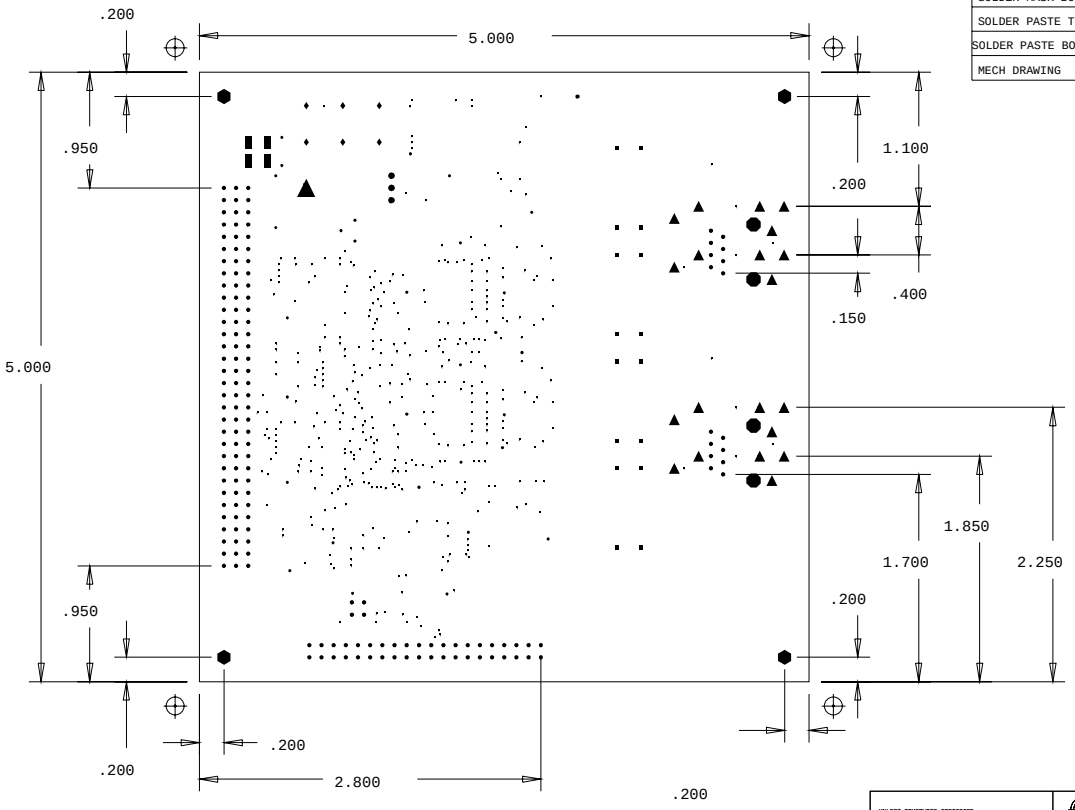
ARTWORK FILM
TOP LAYER
GROUND PLANE
VCC PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
SOLDER PASTE TOP
SOLDER PASTE BOTTOM
MECH DRAWING

REVISIONS

REV	DESCRIPTION	DATE (YY MM DD)	APPROVED

Notes:

1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers. All track width shown under Gerber files are final trace width.
2. Total thickness of board shall be 62 mil +/- 7 mil. The stackup shown is the final stackup of this board.
3. The outline dimension are spedified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
   All holes size shown are final hole size.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.



DRILL CHART			
FIGURE	SIZE	PLATED	QTY
·	13.0	PLATED	398
⋆	25.0	PLATED	30
■	32.0	PLATED	8
▪	32.0	PLATED	16
•	36.0	PLATED	157
♦	42.0	PLATED	6
▲	50.0	PLATED	20
●	55.0	PLATED	3
⬢	125.0	NOT PLATED	4
⬣	128.0	NOT PLATED	4
▲	150.0	NOT PLATED	1

PMC-SIERRA COMET REFERENCE DESIGN REV.2.0 1998

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES

TOLERANCES ON:

2 PL DECIMALS +/- .03

3 PL DECIMALS +/- .003

ANGLES

FRACTIONS

		DATE YY	MM	DD
DRAWN	S. SIU	98	04	01
CHECKED				
ENGINEER				
APPROVED				

PMC-Sierra, Inc.

105-8555 Baxter Place, Buranby B.C.
Canada, V5A 4V7

Tel: 604 415-6000 Fax: 604 415-6200

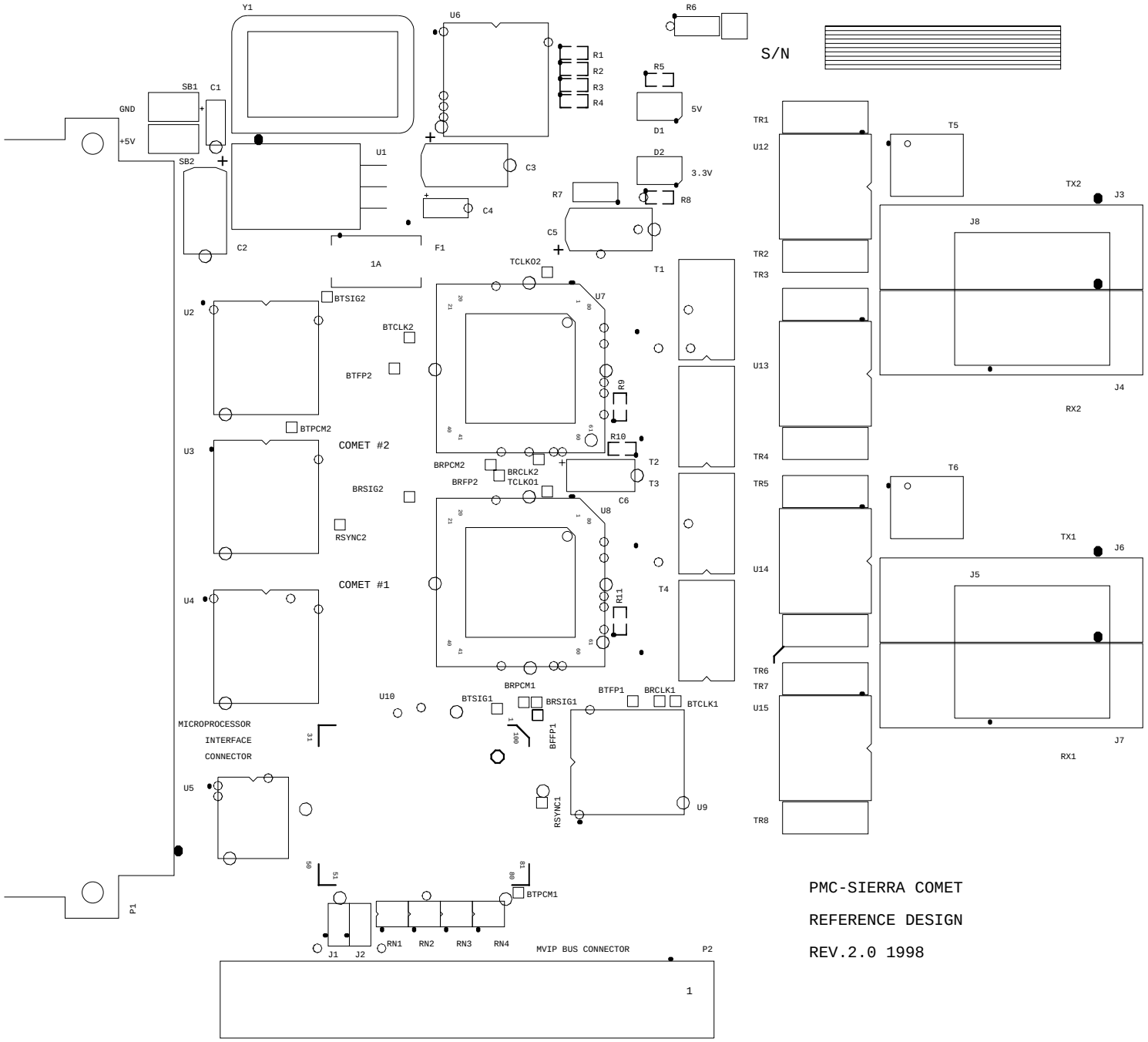
SIZE	FSCM NO	DWG NO
B		

SCALE | SHEET 1 OF 1


C7
R30
C60
SB1
SB2
R12
R13
R14
R15
C9
R16
C8
R18
U16
U17
R17
C15
C16
C17
C10
C11
C18
C19
C20
C21
C22
C23
C24
C27
R22
C45
D3
R19
R20
R21
C26
C12
C25
R24
R23
C13
R25
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C14
C47
D4
R26
R27
C39
R28
C38
C40
C41
R29
C44
RN5
C46
RN6
C48
R31
RN7
R32
R33
C49
Y2
C52
R35
C53
C42
C56
C57
R34
R42
C50
C51
C54
R36
C55
R37
R38
R39
R40
R41
C58
C59


C7
R30
C60
SB1
SB2
R12
R13
R14
R15
C9
R16
R17
C15
C16
C17
C8
C18
C19
R18
C10
C20
C11
C21
U16
C22
C23
C24
C27
R22
C45
D3
C44
RN5
C46
RN6
R19
R20
R21
C26
C25
C12
C28
C29
C30
R24
R23
C31
C13
C32
R25
C33
C14
C34
U17
C35
C36
C37
C47
D4
C48
RN7
R31
R26
R27
C39
R28
C38
C40
C41
R29
R32
R33
C49
R34
R42
C42
Y2
C52
R35
C53
C54
C50
C51
R36
C55
R37
R38
R39
C56
C57
R40
R41
C58
C59

SILK_SCREEN TOP

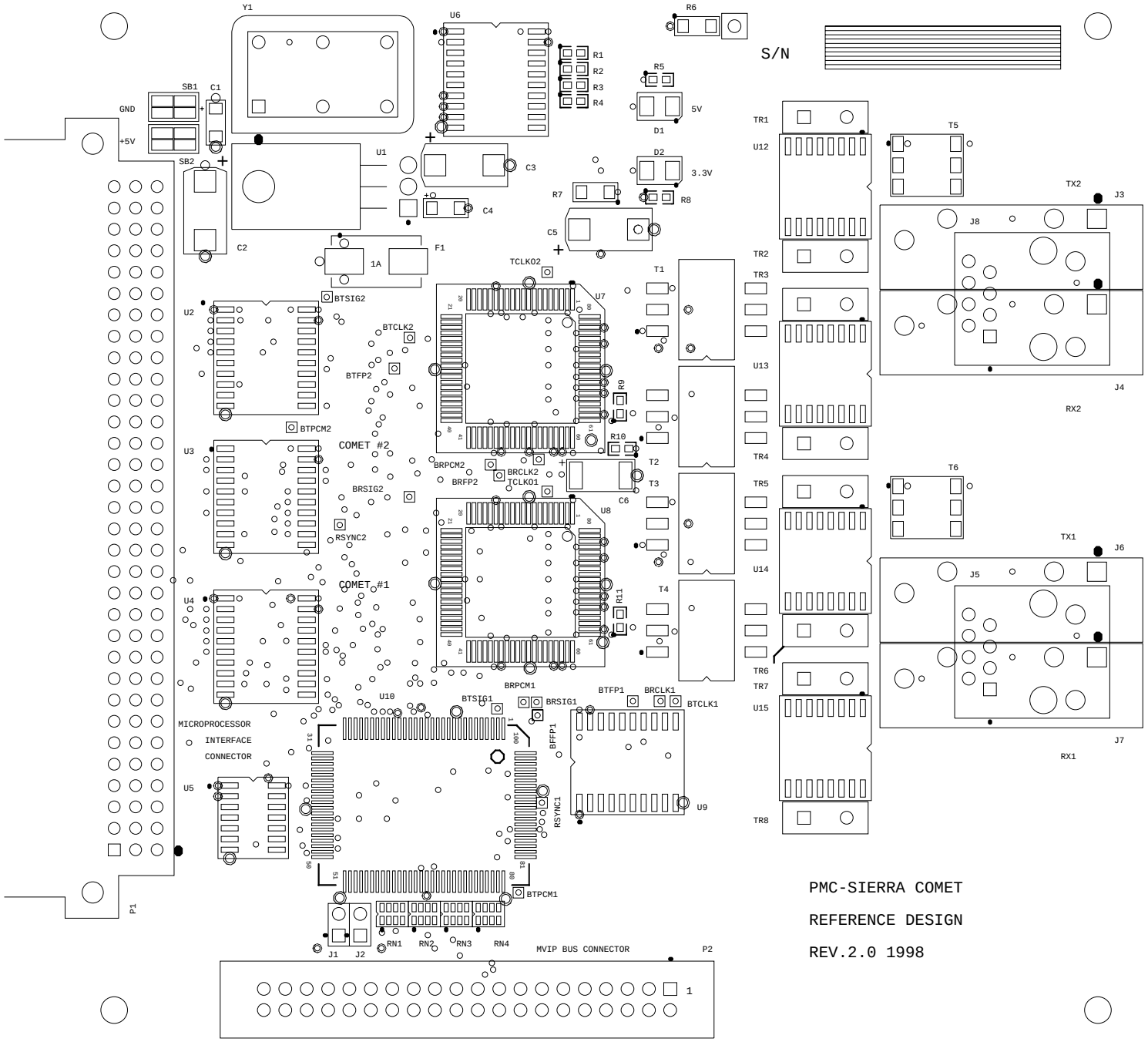


PMC-SIERRA COMET

REFERENCE DESIGN

REV.2.0 1998

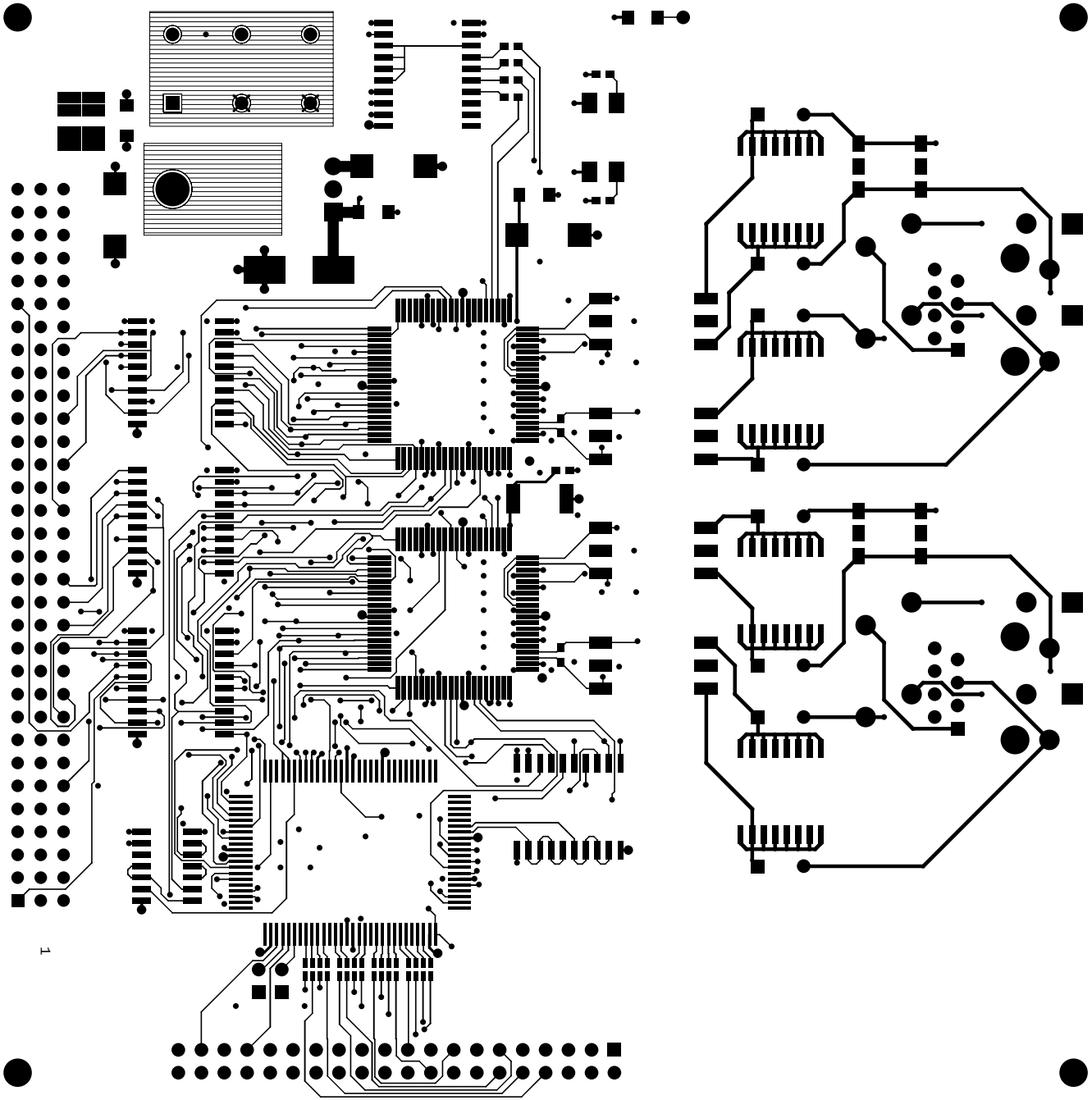
SILK_SCREEN TOP

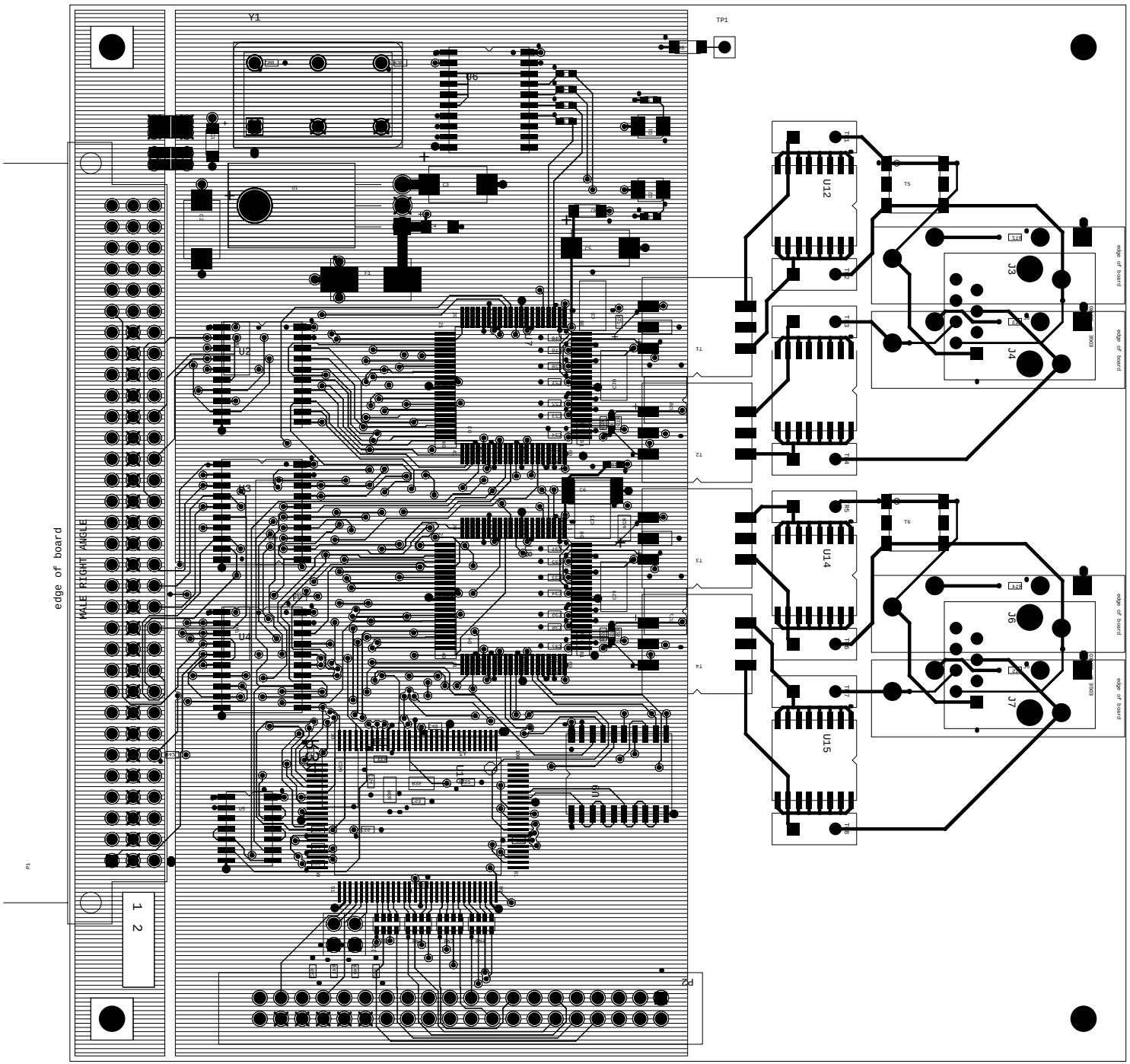


PMC-SIERRA COMET

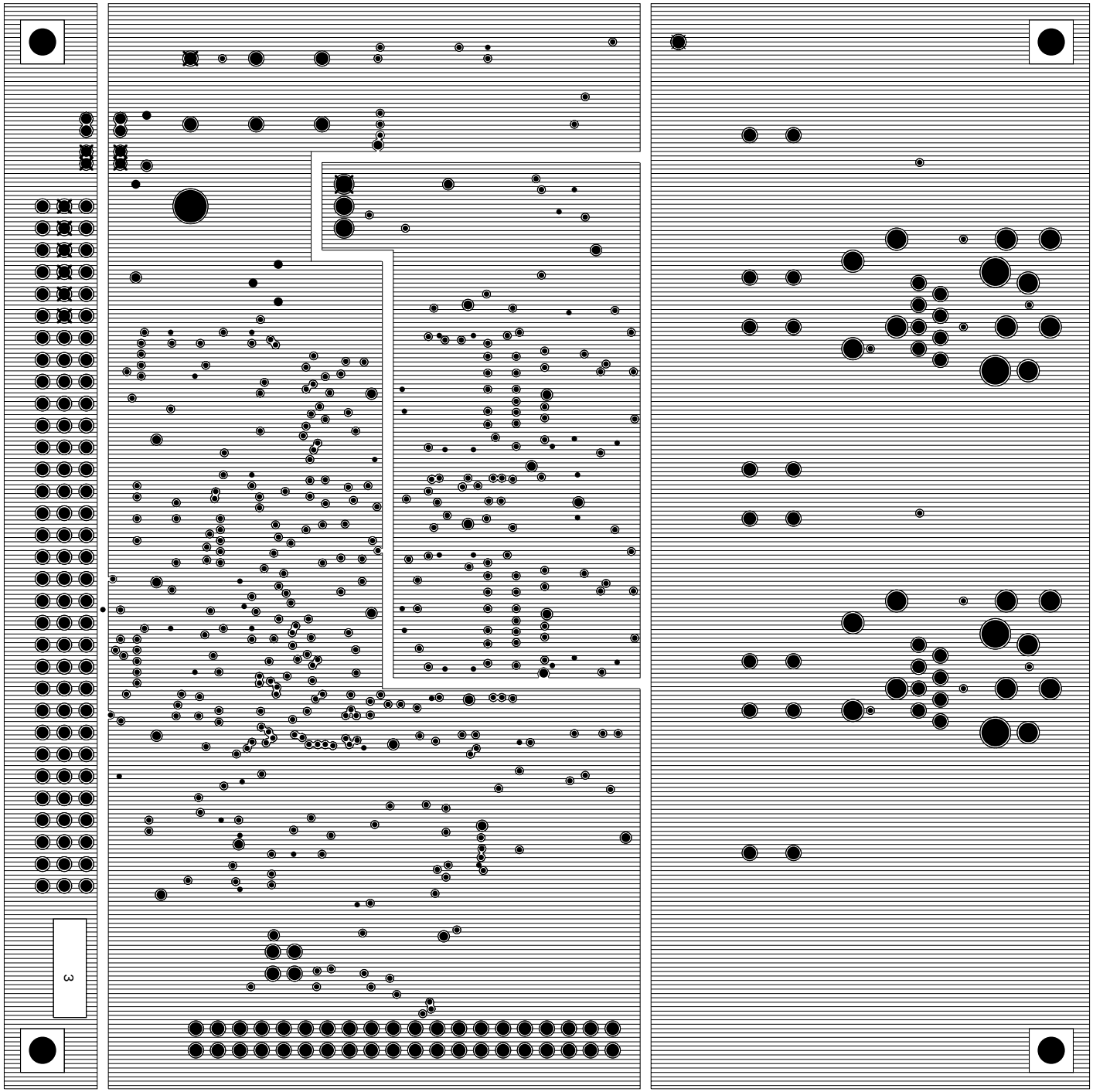
REFERENCE DESIGN

REV.2.0 1998




Y1
TP1
U6
U2
U3
U4
U1
U5
U12
U14
U15
J3
J4
J6
J7
T5
T6
edge of board
MALE RIGHT ANGLE
1 2
P2

VCC PLANE



6 BILL OF MATERIAL

Table 3 : Major Components List

Ref. No	Component	Manufacturer	Package Type	Quantity
U12-U15	LC01-6	Semtech 805-498-2111	SOIC16	4
U16, U17	SRDA3.3-4	Semtech	SOIC8	2
TR1-TR8	Thermistor-TR250-180	Raychem 800-227-7040	RES200	8
U10	MT90810	Mitel 800-648-3579	PQFP100	1
U1	LM3940	National Semiconductor 408-721-5000	TO220	1
P2	20x2 Connector	3M 800-364-3577	Headers	1
T1-T4	MI-50436	Midcom 605-886-4385	RF-trans6_mir	4
	TG23-1505NS	Halo Electronics 650-568-6161	SMD 6 pin	

	Part Name - Value	Part Number	Jedec Type	Ref Des	Qty
1	1N5817_-1N5817M	1N5817M	MLL41	D3, D4	2
2	74HCT00_SOIC-123_XXX XXX		SOIC14	U5	1
3	74HCT245_SOIC-123_XX XXXX		SOIC20W	U3	1
4	74XXX541_SOIC-HCT, 74HCT541	MM74HCT541WM	SOIC20W	U2, U4, U6, U9	4

5	BANTAM-BASE	ELECTRO SONIC -- PC-834-J-(BLACK)	BANTAM	J3, J4, J6, J7	4
6	CAPACITOR-0.01UF, 50V, X7R_603	DIGIKEY PCC103BVCT-ND	603	C7, C15, C16, C19-C26, C28, C29, C32-C38, C40, C42, C44-C48, C51	28
7	CAPACITOR-0.1UF, 16V, Y5V_603	NEWARK -- 52F017	603	C17, C27, C30, C41	4
8	CAPACITOR-0.1UF, 25V, Y5V_603	NEWARK -- 52F017	603	C18, C31, C49, C54-C57	7
9	CAPACITOR-0.47UF, 25V, TANT TEH	DIGI-KEY -- PCT5474CT-ND	SMDTANCAP_A	C4, C11, C39	3
10	CAPACITOR-1000PF, 50V, X7R_0603	DIGI-KEY -- PCC102BNCT-NE	603	C58, C59	2
11	CAPACITOR-18PF, 50V, NPO_603	DIGI-KEY -- PCC180ACVCT-ND	603	C52, C53	2
12	CAPACITOR-1UF, 16V, TANT TEH	DIGI-KEY -- PCT3105CT-ND	SMDTANCAP_A	C1	1
13	CAPACITOR-22PF, 16V, Y5V_603		603	C60	1
14	CAPACITOR-22UF, 6.3V, TANT TEH	DIGI-KEY -- PCT1226CT-ND	SMDTANCAP_C	C6, C9, C10, C14	4
15	CAPACITOR-33UF, 16V, TANT TEH	DIGI-KEY -- PCT3336CT-ND	NEC_D	C50	1
16	CAPACITOR-4.7UF, 10V, TANT TEH	DIGI-KEY -- PCT2475CT-ND	SMDTANCAP_B	C8, C13	2
17	CAPACITOR-47UF, 10V, TANT TEH	DIGI-KEY -- PCT2476CT-ND	NEC_D	C2	1
18	CAPACITOR-68UF, 6.3V, TANT TEH	DIGI-KEY -- PCT1686CT-ND	NEC_D	C3, C5, C12	3
19	CHIP_RES_NETWORK_8_S MD-4.7K	DIGI-KEY -- U7472CT-ND	RN-EXBA	RN5, RN7	2
20	COMET_QFP-BASE	PM4351	QFP80-1	U7, U8	2
21	CON_HEADER_20X2_3M_2 540-BASE	3M -- 2540-6002 UG	HEADER_20X2_3M_2540	P2	1
22	CRYSTAL_MC405-BASE	DIGI-KEY -- SE2405CT-ND	CRYS_MC-405	Y2	1
23	DIN96_MALE-BASE	DIGI-KEY -- A1254-ND	AMP_650473-5	P1	1

24	FUSE__SMD_SOCKET-1.0 00A, NANO	DIGIKEY -- F1222CT-ND	NANO_SMF_SOC KET	F1	1
25	HEADER2S_100 MIL-BASE	DIGI-KEY S1011-36-ND	JUMPER2	J1, J2	2
26	LC01_6_SMD-BASE	SEMTECH -- LC01-6	SOIC16WB	U12-U15	4
27	LED-SUPER_GREEN, SURFACE MOUNT	NEWARK -- 95F9373	LED_11	D1, D2	2
28	LM3940_TO220-BASE	LM3940IT-3.3	TO220ABH	U1	1
29	MI50436		RF-TRANS6_MIR	T1-T4	4
30	MT90810_PQFP-BASE	MT90810AK	QFP100-5	U10	1
31	OSC_TTL_DIP-2.048MHZ , 50 PPM, CHA	K1150BA	CRYS14	Y1	1
32	PE_68624		PE_68624	T5, T6	2
33	RESISTOR-1, 5%, 603		603	R10, R17, R19, R26	4
34	RESISTOR-1.0, 1%, 1206	DIGI-KEY -- P<VALUE>RCT-ND	SMDRES1206	R7, R24	2
35	RESISTOR-1.0M, 5%, 1206	DIGI-KEY -- P<VALUE>ECT-ND	SMDRES1206	R35, R36	2
36	RESISTOR-1.8K, 5%, 603	DIGI-KEY -- P1.8KGCT-ND	603	R40, R41	2
37	RESISTOR-100, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	603	R12-R15, R33	5
38	RESISTOR-100K, 1%, 603		603	R21, R28	2
39	RESISTOR-100K, 5%, 1206	DIGI-KEY -- P<VALUE>ECT-ND	SMDRES1206	R6	1
40	RESISTOR-12.7, 1%, 603	DIGI-KEY -- P12.7HCT-ND	603	R16, R18, R23, R25	4
41	RESISTOR-18.2, 1%, 603	DIGI-KEY -- P18.2HCT-ND	603	R9, R11	2
42	RESISTOR-24.9, 1%, 603	DIGI-KEY -- P24.9HCT-ND	603	R34	1
43	RESISTOR-270, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	603	R5, R8	2
44	RESISTOR-4.7, 5%, 603		603	R20, R27	2

45	RESISTOR-4.7K, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	603	R22, R29, R31, R32, R37-R39, R42	8
46	RESISTOR-75.0, 1%, 603		603	R1-R4, R30	5
47	RES_ARRAY_15_SMD-4.7 K	DIGI-KEY -- 766-161-R<VALUE>-ND	SOIC16	RN6	1
48	RES_ARRAY_4_SMD-47	DIGI-KEY -- Y4<VALUE CODE>-ND	RN4	RN1-RN4	4
49	RJ48-MOLEX_95001	MOLEX -- 95001-9841	RJ48	J5, J8	2
50	SRDA3_3_4_SMD-BASE	SEMTECH -- SRDA3_3_4	SOIC8	U16, U17	2
51	THERMISTOR-TR250-180 , RES200		RES200	TR1-TR8	8
52	TST_PT-BASE	DIGI-KEY S1011-36-ND	TST_PT_1	TP1	1

7 REFERENCES

- PMC-Sierra, Inc., PM4351 COMET Data Sheet, Issue 4, April 1998
- GO-MVIP, Inc., MVIP-90 Standard, Release 1.1, October 1994
- Applied Telecom web page: www.apptel.com
- ANSI - T1.403-1995 – American National Standard for Telecommunications – Carrier to Customer Installation – DS-1 Metallic Interface Specifications.
- European Telecommunication Standard – ETS 300 046 – Integrated Services Digital Network (ISDN); Primary rate access – safety and protection
- ETSI Technical Basis for Regulation - TBR 13 – Business Telecommunications (BTC); 2048 kbit/s digital structured leased lines (D2048S); Attachment requirements for terminal equipment
- ETSI Technical Basis for Regulation - TBR 12 – Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2048 kbit/s digital unstructured leased lines (D2048U); Attachment requirements for terminal equipment interface
- ETSI Technical Basis for Regulation - TBR 4 – Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN usin ISDN primary rate access
- Federal Communications Commission code of federal regulations - FCC Part 68

NOTES

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