PM5350

S/UNI-155 ULTRA

SATURN USER NETWORK INTERFACE

DATASHEET ERRATA

ISSUE 4: FEBRUARY 2002

REVISION HISTORY

Issue No.	Issue Date	Details of Change
4	February 2002	Added Canadian patent number (Prep 6584) Added U.S., Canadian, UK and French patent numbers (Prep 7005)
3	May 2000	Capacitor needed between RCAP1 and RCAP2 for UTP-5 mode to function.
2	Jun 1999	Specification of power supply ramp in low temperature conditions.
1	Jan 1999	This document contains changes to the datasheet revision 5 and details changes for industrial temperature optical operation

CONTENTS

1 ISSUE 4 ERRATA

This issue 4 errata notifies that changes have been made to the issue 5 of the PMC-960924 data sheet. A summary of the changes made to the issue 5 datasheet is provided. The issue 5 datasheet and issue 4 errata supersede all prior editions and versions.

2 INDUSTRIAL TEMPERATURE OPERATION

The device has been re-qualified for operation in industrial temperature conditions under certain circumstances. Specifically, if the device is operated in PECL mode only (i.e. with PECLSEL selected TTL high) the device can be used in industrial temperature conditions (i.e. -40 to 85 degrees Celsius). However, if the device is used in UTP-5 applications (i.e. with PECLSEL selected TTL low) the device is only rated for commercial temperature operation (i.e. 0 to 70 degrees Celsius).

If the device is used in PECL mode under industrial temperature conditions certain timing parameters will be changed. However, the device can be used in PECL mode under commercial temperatures without modifying the timing.

2.1 Page 183

Page 183 section 10 “Absolute maximums” has been changed to the following:

Ambient Temperature under Bias (UTP-5)	0°C to +70°C
Ambient Temperature under Bias (PECL)	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Junction Temperature	+150°C

2.2 Pages 197-199

Pages 197-199 Tables 6 and 7 of the issue 5 datasheet has changed to the following:

Table 6 - Drop Side Receive Synchronous Interface (TSEN = 0) (Figure 28)

Symbol	Description	Min	Max	Units
	RFCLK Frequency		50	MHz
	RFCLK Duty Cycle	40	60	%
$^{t}S_{RRDENB}$	RRDENB to RFCLK High Setup	4		ns
$^{t}H_{RRDENB}$	RFCLK High to RRDENB Hold	1		ns
$^{t}P_{RDAT}$	RFCLK High to RDAT[7:0] Valid	2*	14	ns
$^{t}P_{RXP}$	RFCLK High to RXPRTY Valid	2*	14	ns
$^{t}P_{RCA}$	RFCLK High to RCA Valid	2	14	ns
$^{t}P_{RSOC}$	RFCLK High to RSOC Valid	2	14	ns

*** NOTE:**

For PECL mode (i.e. not for UTP-5, PECLSEL pin driven TTL high) under industrial temperature, -40°C to 85°C operation (instead of 0°C to 70°C operation), the following timing parameters change:

$^{t}P_{RDAT}$ is 1.5ns for MIN. instead of 2ns

$^{t}P_{RXP}$ is 1.5 ns. for MIN. instead of 2ns

Note PECL operation under 0°C to 70°C conditions can use the original values in Table 6.

Table 7 – Drop Side Receive Synchronous Interface (TSEN = 1) (Figure 29)

Symbol	Description	Min	Max	Units
	RFCLK Frequency		50	MHz
	RFCLK Duty Cycle	40	60	%
$t_{SRRDENB}$	RRDENB to RFCLK High Setup	4		ns
$t_{HRRDENB}$	RFCLK High to RRDENB Hold	1		ns
t_{PRDAT}	RFCLK High to RDAT[7:0] Valid	2	14	ns
t_{ZRDAT}	RFCLK High to RDAT[7:0] Tristate	2	14	ns
t_{PRXP}	RFCLK High to RXPRTY Valid	2	14	ns
t_{ZRXP}	RFCLK High to RXPRTY Tristate	2*	14	ns
t_{PRCA}	RFCLK High to RCA Valid	2	14	ns
t_{PRSOC}	RFCLK High to RSOC Valid	2	14	ns
t_{ZRSOC}	RFCLK High to RSOC Tristate	2	14	ns

*** NOTE:**

For PECL mode (i.e. not for UTP-5, PECLSEL pin driven TTL high) under industrial temperature, -40°C to 85°C operation (instead of 0°C to 70°C operation), the following timing parameters change:

t_{ZRXP} is 1ns. for MIN. instead of 2ns

Note PECL operation under 0°C to 70°C conditions can use the original values in Table 7.

3 ANALOG POWER-UP RAMP RATE REQUIREMENT AT LOW TEMPERATURE

Description

The analog supply voltage (RAVD2) requires a minimum voltage ramp rate during up power up. If the power ramp is too slow the S/UNI ULTRA will be unable to lock to received data. The required ramp rate is a strong function of temperature, as shown in Table 1.

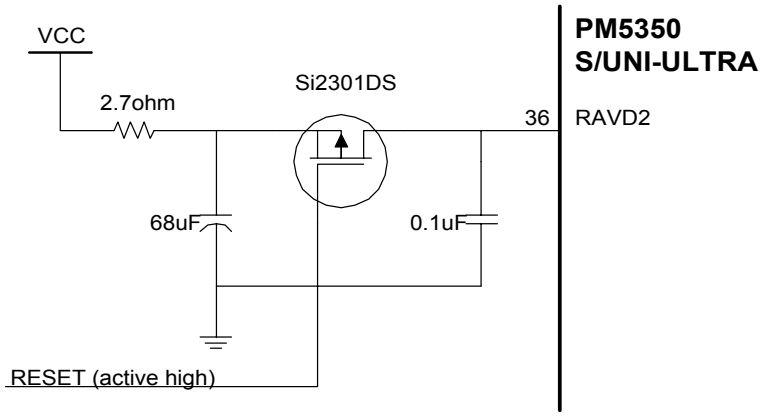
Table 1 Maximum RAVD2 Power-up Ramp Time vs. Temperature

$T_{ambient}$ (°C)	Maximum Ramp Time Requirement (10% to 90% voltage ramp)
25	50ms
0	1ms
-40	1μs

Devices that are not powered up correctly will recover normal operation when the ambient temperature rises. Once operating normally, a device will continue to operate normally over the full rated temperature range.

Recommendation

Some board-level power supplies cannot provide the required voltage ramp rates for proper operation at 0°C or –40°C, so an external circuit is needed to gate the power to RAVD2. A recommended circuit is given below.



Resistor, capacitors are part of existing supply filtering recommendations in reference design.

The RESET signal is a standard CMOS signal: 0 to 5V swing with t_{rise} and t_{fall} <20ns. During device power-up, RESET must be held active (high) for at least 10ms to allow the capacitors to discharge. Then, when RESET is brought low, the device will begin operating normally.

Please contact the PMC-Sierra Applications department for more information.

Performance with Recommendation

All devices will power-up correctly over the entire industrial temperature range (-40 to 80°C).

Performance without Recommendation

Upon power-up at low temperature, some devices may not lock to reference clock (RROOLV=1 in register 08h) and to data (RDOOLV=1 in register 80h). In this condition, the reference clock output (RCLK, pin 55) may be DC or very low frequency.

4 CAPACITOR NEEDED BETWEEN RCAP1 AND RCAP2 FOR UTP-5 MODE

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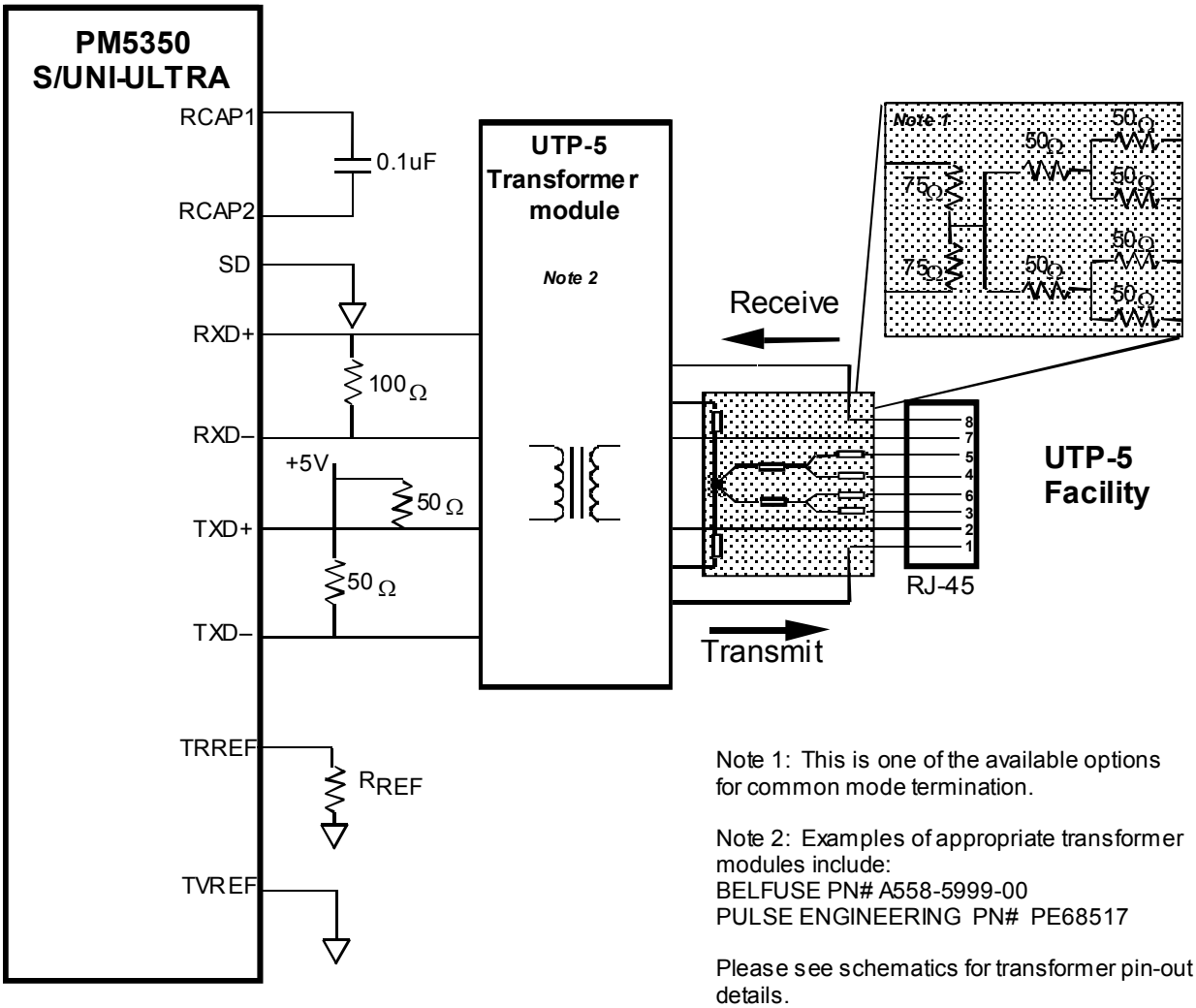
RCAP1 RCAP2	Analog	27 28	~~The RCAP1 and RCAP2 pins should be connected to the RAVS3 analog ground.~~ A non-polarized 0.1 uF capacitor must be connected between RCAP1 and RCAP2 for UTP-5 mode. A proper capacitor C_{RX} must be used to provide proper frequency response for the Twisted-pair baseline wander correction circuit. These inputs can be tied to RAVS3 analog ground for PECL mode operation. Please refer to the APPLICATIONS and the EXTERNAL COMPONENTS sections of this document for a detailed C_{RX} specification.

Figure 17 has been updated with the following diagram:

Figure 17 Interfacing TXD+/- and RXD+/- with UTP-5



Note 1: This is one of the available options for common mode termination.

Note 2: Examples of appropriate transformer modules include:
BELFUSE PN# A558-5999-00
PULSE ENGINEERING PN# PE68517

Please see schematics for transformer pin-out details.

5 PATENT INFORMATION

No patent information in original data sheet.

Note: The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 6,188,692 U.S. Patent No. 6,104,277 U.S. Patent No. 5,987,065 U.S. Patent No. 6,054,884 Canadian Patent No. 2,217,985 Canadian Patent No. 2,227,097 Canadian Patent No. 2,149,076 Canadian Patent No. 2,179,246 UK Patent No. 2,305,541 UK Patent No. 2,290,438 French Patent No. 2,738,953

Relevant patent applications and other patents may also exist.

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
(604) 415-4533
Web Site: http://www.pmc-sierra.com

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