PM5347

S/UNI-155 PLUS

SATURN USER NETWORK INTERFACE

DATASHEET ERRATA

ISSUE 1: JANUARY 1999

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	April 1999	This document contains changes to the datasheet revision 6

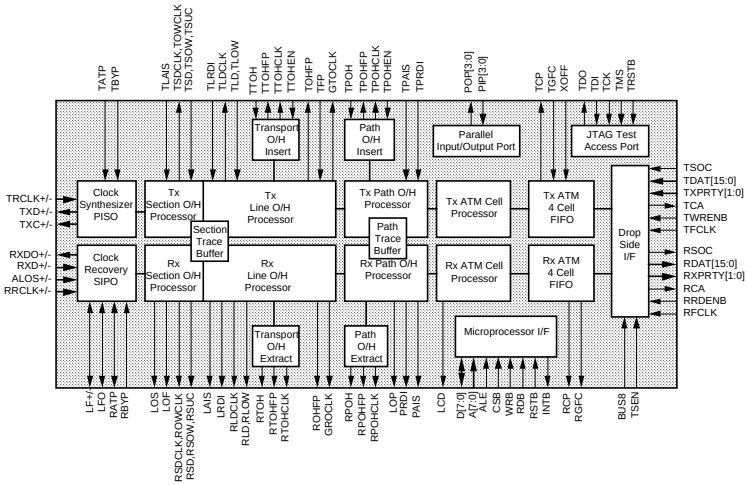
CONTENTS

1 ISSUE 1 ERRATA

This document is the errata notice for Issue 6 of the S/UNI-PLUS datasheet (PMC-941033). Issue 1 of the S/UNI-PLUS errata notice and issue 6 of the datasheet supersedes all prior editions & versions.

2 DATASHEET ISSUE 6 ERRATA

The following details documentation errors in datasheet issue 6.

PAGE	ERROR	DESCRIPTION/CORRECTION
3	*Correction to synthesizer feature.*	The text states: "• Synthesizes the 155.52 MHz or 51.84 MHz transmit clock from a 19.44 MHz or 6.48 MHz reference." The text should have read: "• Synthesizes a 155.52 MHz transmit clock from a 19.44 MHz reference". The rev D S/UNI-PLUS will not synthesize a 51.84 MHz clock. For STS-1 operation the rev D S/UNI-PLUS needs to be in clock bypass mode in both the receive and transmit directions. In STS-3 mode, the 19.44 MHz reference is required when not in bypass, the 6.48 MHz reference is not applicable.
7	*Correction to block diagram.*	The TOWCLK, TSDCLK and TLDCLK signals were incorrectly shown as inputs. The block diagram has been updated to show them as outputs. 
26	*Correction to PIP[3:0] pin description.*	The PIP[3:0] pin description incorrectly states that each input contains an integral pull-down resistor. No input pull-ups or pull-downs are used on these pins.
63	*Clarification of SDH J0/Z0 and TSTBEN description.*	The description of the SDH J0/Z0 states that if the TSTBEN bit is high, the section trace message, stored in the SSTB block, will overwrite the J0 byte regardless of the SDH J0/Z0 state. In fact both the SDH J0/Z0 and TSTBEN bits must be high to enable overwriting the J0 byte.
67	*Applications information for the RXDINV bit.*	In Line Loopback mode (LLE=1) the RXD+ and RXD- inputs are connected to the TXD+ and TXD- outputs respectively. In Line Loopback mode the RXD inputs are not inverted before they are connected to the TXD outputs. Designs requiring RXD to be inverted will not operate correctly in Line Loopback mode. The LOS detection logic is connected to the non-inverted RXD inputs and therefore will not work correctly when the RXD inputs are inverted.
68	*Correction to RRCLKA description.*	The RRCLKA bit is incorrectly titled "TTCLKA". It should be titled "RRCLKA".

<table>
<tr><td>68</td><td>Correction to TRCLKA description.</td><td>The TRCLKA bit description incorrectly states that this bit monitors “for low to high transitions on the TRCLK+ and TRCLK- inputs.
This should be changed to the following:
TTIME[0] bit of Reg. 0x03 selects which clock TRCLKA monitors. If TTIME[0] = 0, then TRCLKA monitors the activity of the TRCLK+/- pins. If TTIME[0] = 1, then TRCLKA monitors the activity of the RRCLK+/- pins</td></tr>
<tr><td>70</td><td>Correction to TREFSEL description.</td><td>The S/UNI-PLUS rev D will not work with a 6.48 MHz reference clock; therefore, TREFSEL should always be a logic zero for correct operation.</td></tr>
<tr><td>71</td><td>Correction to RREFSEL description.</td><td>The S/UNI-PLUS rev D will not work with a 6.48 MHz reference clock; therefore, RREFSEL should always be a logic zero for correct operation.</td></tr>
<tr><td>71</td><td>Applications information for the RDOOLV bit</td><td>While the PLL is locking onto the incoming data, the RDOOLV status will make numerous transitions. Correct interpretation of RDOOLV can be accomplished by polling the RDOOLV and RDOOLI bits at 100 msec intervals. When RROOLV and RROOLI are both polled at logic 0, then the recovered clock and reference are within 488 ppm.</td></tr>
<tr><td>101</td><td>RTIMIE and RTIUIE functions have been added to Register 28H, SSTB Control, description.</td><td>
<table>
<tr><th>Bit</th><th>Type</th><th>Function</th><th>Default</th></tr>
<tr><td>Bit 7</td><td></td><td>Unused</td><td>X</td></tr>
<tr><td>Bit 6</td><td>R/W</td><td>RRAMACC</td><td>0</td></tr>
<tr><td>Bit 5</td><td>R/W</td><td>RTIUIE</td><td>0</td></tr>
<tr><td>Bit 4</td><td>R/W</td><td>RTIMIE</td><td>0</td></tr>
<tr><td>Bit 3</td><td>R/W</td><td>PER5</td><td>0</td></tr>
<tr><td>Bit 2</td><td>R/W</td><td>TNULL</td><td>1</td></tr>
<tr><td>Bit 1</td><td>R/W</td><td>NOSYNC</td><td>0</td></tr>
<tr><td>Bit 0</td><td>R/W</td><td>LEN16</td><td>0</td></tr>
</table>
<u>RTIMIE:</u>
The RTIMIE bit controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state. When RTIMIE is a logic one, changes in match state activates the interrupt (INTB) output.
<u>RTIUIE:</u>
The RTIUIE bit controls the activation of the interrupt output when the receive identifier message changes state. When RTIUIE is a logic one, changes in the received section trace identifier message stable/unstable state will activate the interrupt (INTB) output.
</td></tr>
</table>

103	*RTIMV, RTIMI, RTIUV and RTIUI functions have been added to Register 29H, SSTB Section Trace Identifier Status, description.*	

Bit	Type	Function	Default
Bit 7	R	Busy	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

RTIMV:

The RTIMV bit reports the match/mismatch status of the identifier message framer. RTIMV is a logic one when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is a logic zero when the accepted message matches the expected message.

RTIMI:

The RTIMI bit is a logic one when match/mismatch status of the trace identifier framer changes state. This bit is cleared when this register is read.

RTIUV:

The RTIUV bit reports the stable/unstable status of the identifier message framer. RTIUV is a logic one when the current received section trace identifier message has not matched the previous message for eight consecutive messages. RTIUV is a logic zero when the current message becomes the accepted message as determined by the PER5 bit in the SSTB Control register.

RTIUI:

The RTIUI bit is a logic one when stable/unstable status of the trace identifier framer changes state. This bit is cleared when this register is read.

106	*SSTB Synchronization Message Status Register (Reg. 2D) have been added.* *Note: The current GR-253-CORE (5.4.7.1) requires the byte validation to be done over 8 frames, instead of 5 frames as is done in the S/UNI-PLUS. This, however, is still useful to be included, since it relieves the microprocessor from polling Reg. 0x0E, the Receive S1 register, every frame to validate the synchronization message.*	**Register 0x2D: SSTB Synchronization Message Status** **Bit** / **Type** / **Function** / **Default** Bit 7 / R/W / SMUE / 0 Bit 6 / / Unused / X Bit 5 / / Unused / X Bit 4 / / Unused / X Bit 3 / R / SMUI / X Bit 2 / R / SMUV / X Bit 1 / / Unused / X Bit 0 / / Unused / X This register reports the synchronization message status of the SSTB. SMUV: The SMUV bit reports the unstable status of the received synchronization message. SMUV is a logic one when the received S1 byte differs from the previously received S1 byte for five consecutive frames. SMUV is a logic zero when S1 byte values are identical for five consecutive frames. SMUI: The SMUI bit is a logic one when the synchronization message unstable status changes state. This bit is cleared when this register is read. SMUE: The SMUE bit controls the activation of the interrupt output when the synchronization message unstable status changes state. When SMUE is a logic one, an unstable status state change activates the interrupt (INTB) output.

130-131	*Correction to TPOP Path Status Register Description*	All references to the TPOP Source Control Register should be ignored: G1[1], G1[0]: The G1[1:0] bits are inserted in the unused bit positions in the path status byte when the primary input TPOHEN is low during the unused bit positions in the path overhead input stream, TPOH. APRDI: The APRDI bit controls the insertion of the auxiliary path remote defect indication. When APRDI is a logic one, the APRDI bit position in the path status byte is set high. When APRDI is a logic zero, the APRDI bit position in the path status byte is set low. This bit has no effect if the primary input TPOHEN is high during the path status remote defect indication bit position in the path overhead input stream in which case the value is inserted from TPOH. PRDI: The PRDI bit controls the insertion of the path remote defect indication. This register bit value is logically ORed with the input TPRDI. When PRDI is a logic one, the PRDI bit position in the path status byte is set high. When PRDI is a logic zero, the PRDI bit position in the path status byte is set low. This bit has no effect if the primary input TPOHEN is high during the path status remote defect indication bit position in the path overhead input stream in which case the value is inserted from TPOH. FEBE[3:0]: The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte when the primary input TPOHEN is low during the path status FEBE bit positions in the path overhead input stream, TPOH. The value contained in FEBE[3:0] is cleared after being inserted in the path status byte. Any non-zero FEBE value overwrites the value that would normally have been inserted based on the number of receive B3 errors during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.
140	*Clarification of HCSFTR[1:0].*	For correct operation the HCSFTR[1:0] bits must be set to 00. This condition requires one ATM cell with correct HCS to switch from detection mode to correction mode.
149	*Correction to the description of the DHCS bit.*	The DHCS bit description states that DHCS controls the insertion of single bit errors. The assertion of DHCS causes the next HCS octet to be inverted forcing 8 bit errors not just one.
149	*Application information for the FIFORST bit.*	The FIFORST bit in register 0x60: "TACP Control/Status" initializes the transmit FIFO. For correct operation, a FIFORST should be issued at the end of each initialization cycle (ie. at the end of the reset routine). A transmit FIFORST should also be issued each time TSOC changes boundaries. Boundary changes are identified by TSOCI (bit 6). The FIFORST should be asserted for a minumum of 3.5us. (one cell period at 155Mbps).
179	*Sources for filter caps.*	Surface mount capacitors for these values are available from ATC, AVX, muRata, and NEC.

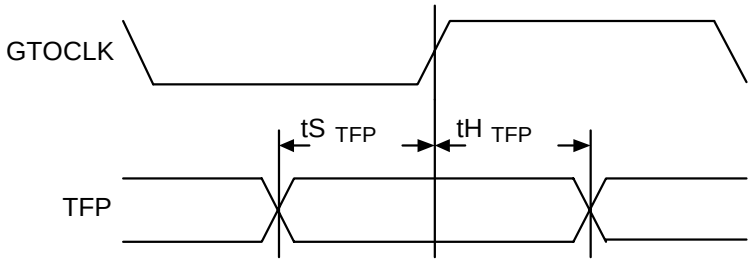
<table>
<tr><td>186</td><td>Changes to Bit Error Rate Monitor Settings</td><td>The recommended register settings for STS-1 mode should be as follows:

<table>
<tr><th>BER</th><th>Reg.0x72</th><th>Reg.0x73</th><th>Reg.0x74</th><th>Reg.0x75</th></tr>
<tr><td>10-4</td><td>A0</td><td>00</td><td>4F</td><td>00</td></tr>
<tr><td>10-5</td><td>B0</td><td>04</td><td>3E</td><td>00</td></tr>
<tr><td>10-6</td><td>E0</td><td>2E</td><td>3E</td><td>00</td></tr>
</table>

The recommended register settings for STS-3c mode should be as follows:

<table>
<tr><th>BER</th><th>Reg.0x72</th><th>Reg.0x73</th><th>Reg.0x74</th><th>Reg.0x75</th></tr>
<tr><td>10-4</td><td>34</td><td>00</td><td>4D</td><td>00</td></tr>
<tr><td>10-5</td><td>90</td><td>01</td><td>3E</td><td>00</td></tr>
<tr><td>10-6</td><td>A0</td><td>0F</td><td>3E</td><td>00</td></tr>
</table>
</td></tr>
<tr><td>203-204</td><td>Clarification of RRDENB</td><td>RRDENB must not be de-asserted during the second to last word (or byte) of a cell. It has been found that de-asserting RRDENB during the second to last word (or byte) of a cell may result in the loss of the last word (or byte).</td></tr>
<tr><td>207</td><td>Addition of VTPIH and VTPIL DC characteristic</td><td>VTPIH is the guaranteed input HIGH voltage of inputs while in TTL mode. See Figure 11 on Page 178 of the datasheet. VTPIL is the guaranteed input LOW voltage when in TTL mode. These specifications apply to the inputs ALOS- and REFCLK- only.
VTPIH minimum voltage is 2.2V. The maximum voltage is V_{DD}+0.5V.
VTPIL minimum voltage is –0.5V. The maximum voltage is 0.8V.</td></tr>
<tr><td>208</td><td>Clarification of the I_{IL} parameter.</td><td>The I_{IL} parameter is not relevant for PECL inputs.</td></tr>
<tr><td>224</td><td>Addition of TFP timing.</td><td>The following timing parameters for the TFP input should be added to figure 38.

<table>
<tr><th>Symbol</th><th>Description</th><th>Min</th><th>Max</th><th>Units</th></tr>
<tr><td>tS_{TFP}</td><td>TFP Set-up time to GTOCLK</td><td>15</td><td></td><td>ns</td></tr>
<tr><td>tH_{TFP}</td><td>TFP Hold time to GTOCLK</td><td>0</td><td></td><td>ns</td></tr>
</table>

</td></tr>
<tr><td>230</td><td>Change to t_{PRCA}, t_{PRDAT}, t_{PRSOC} and $t_{PRXPRTY}$ min delay.</td><td>The t_{PRCA}, t_{PRDAT}, t_{PRSOC} and $t_{PRXPRTY}$ min delays have been changed to 2 ns from 1 ns.</td></tr>
</table>

NOTES

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