ATM/PACKET Traffic Manager and Switch

FEATURES

- ATM (fixed length cell) and packet/ frame traffic manager and switch.
- 2048 line ports, 4 WAN ports, and a high speed microprocessor port. Any port to any port switching for 64k independent connections.
- Manages up to 256k cell (16M byte) data buffer and 4M byte context memory shared over all ports.
- Configurable progressive throttling of buffer consumption, with memory reservation under high consumption. Supports ABR with EFCI marking.
- Buffer congestion controlled via Partial Packet Discard, Early Packet Discard (PPD/EPD). Cell at a time discard also supported.
- For frame/packet flows:
  - Supports external wire speed HDLC processor, SAR, and flow classifier via packet-contiguous queuing and scheduling.
  - Error indication in AAL5 EOM trailer (set by SAR or classifier) can invoke errored packet discard, thereby eliminating need for packet buffers in external devices.
- Traffic queuing algorithm is highly configurable on a per connection, per class, and per port basis.
- Configurable scheduling of 4 classes of service on every port, with rate shaping available for the 4 WAN ports. Configurable traffic parameters enabling a mix of CBR, VBR, GFR, and UBR classes.
- Configurable OAM cell queuing and special handling on all ports.
- VPI/VCI header mapping.
- Supports 700 Mb/s ingress traffic and 700 Mb/s egress traffic aggregated across all ports.
- Low power 3.3/2.5V CMOS.
- Standard 5 pin P1149 JTAG port.
- 352 ball SBGA, 35mm x 35mm.

BUS INTERFACES

- 8/16 bit, 52 MHz UTOPIA L2 bus.
- Line side:
  - Enhanced UTOPIA Tx master supports 2048 ports. Rx master supports 32 ports.
  - Or single port slave.
- WAN side:
  - Master (with optional cell length expansion) supports 4 Tx or Rx ports.
  - Or single port slave.

MICROPROCESSOR INTERFACE

- 66 MHz, 32 bit address/data bus capable of single or burst access to internal registers and cell buffers.
- Supports cell/packet transfer to/from any port, with CRC32 and CRC10 calculation supported in hardware.
- Works seamlessly with S/UNI-VORTEX and S/UNI-DUPLEX to implement a system-wide embedded communication channel.

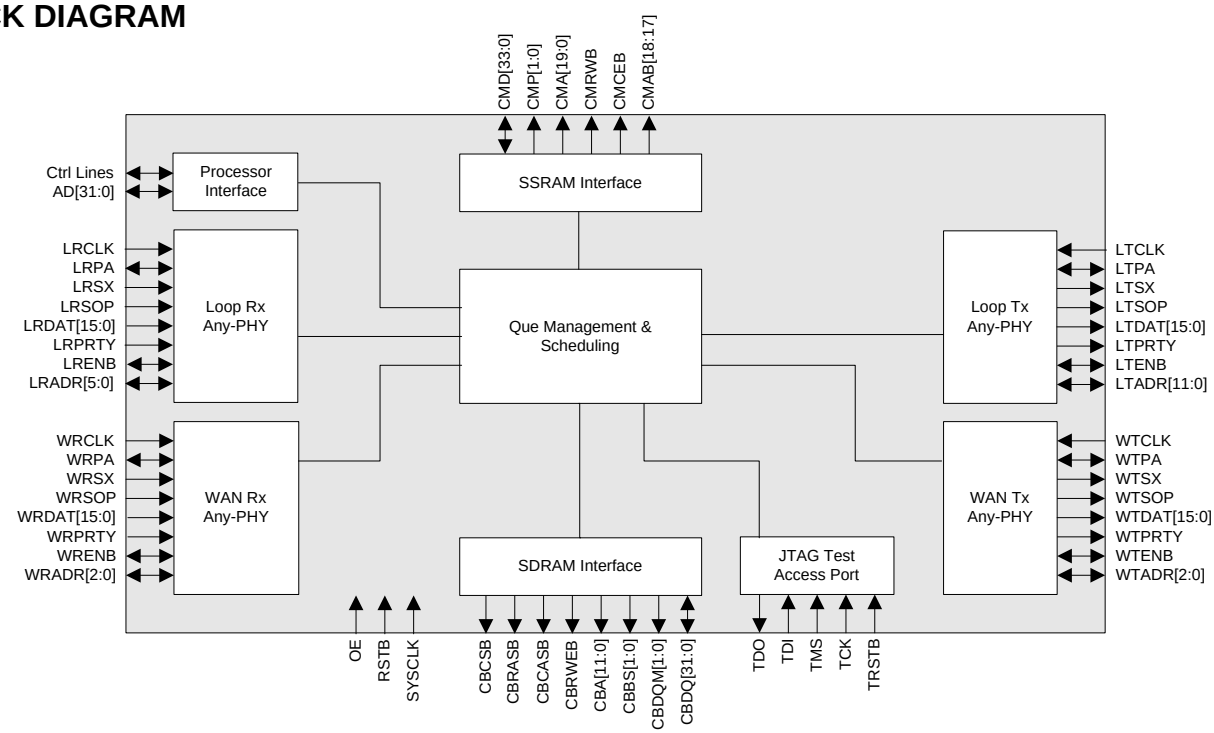
CONGESTION CONTROL

- Traffic discard thresholds configurable per connection (independent CLP0 and CLP1 thresholds), per class, per port, and per direction.
- Guaranteed Frame Rate (GFR) implemented via CLP0 minimum buffer size reservation per connection.

QUEUING & SCHEDULING

- 64k traffic staging queues (one per connection) individually assignable to any CoS on any port.
- 8k + 20 scheduling queues: 4 CoS queues per port, 2048 line ports, 4 WAN ports, and 1 processor port.

BLOCK DIAGRAM



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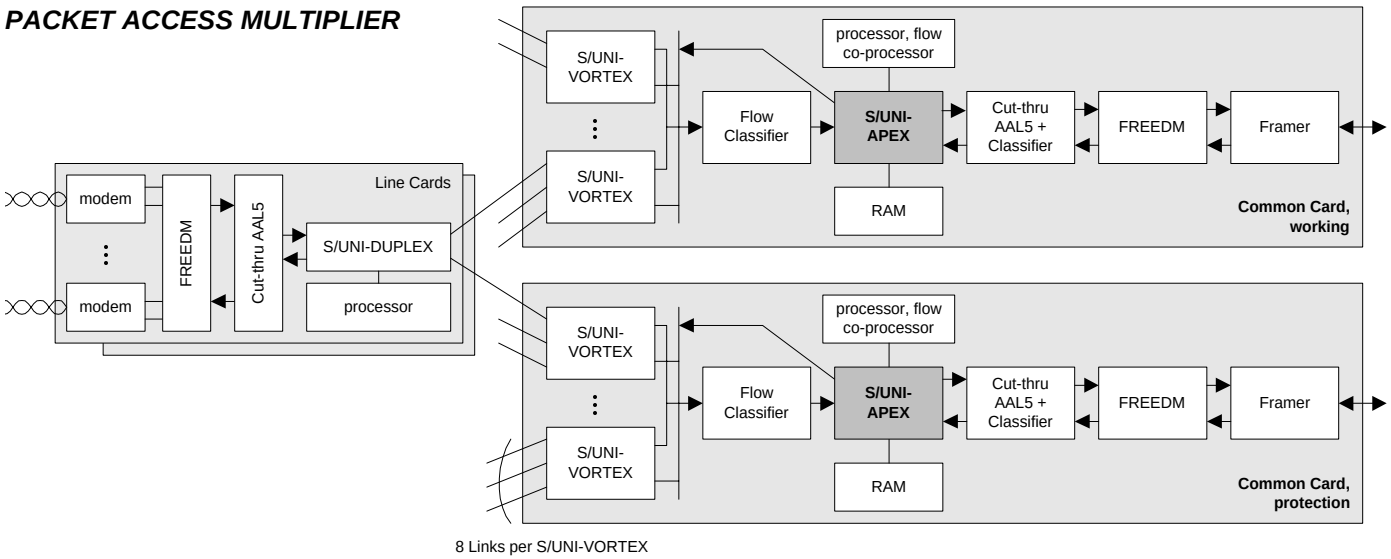
PACKET ACCESS MULTIPLIER



Head Office:
PMC-Sierra, Inc.
#105 - 8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

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