PM7380

FREEDM-32P672

REVISION C DEVICE ERRATA

Issue 3

December 2001

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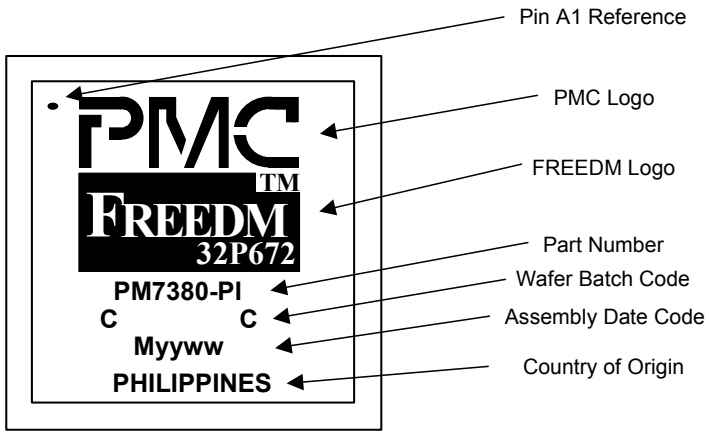
1. Introduction

In this document, Section 2 lists the known functional errata for revision C of PM7380 FREEDM-32P672 and Section 3 lists errors found in Issue 5 of the FREEDM-32P672 datasheet (PMC-1990262).

1.1. Device Identification

The information contained in Section 2 relates to Revision C of PM7380 FREEDM-32P672 only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1.1). PM7380 FREEDM-32P672 Revision C is packaged in a 329-pin Plastic Ball Grid Array (PBGA).

Figure 1.1: PM7380 FREEDM-32P672 Branding Format.



Not to Scale

1.2. Reference

- PMC-1990262, FREEDM-32P672 Long Form Data Sheet, Issue 5.

2. FREEDM-32P672 Revision C Functional Deficiency List

This section lists the known functional deficiencies for Revision C of FREEDM-32P672 (as of the publication date of this document). For each deficiency, the known work-around and the operating constraints, with and without the work-around, are also described.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

2.1. FREEDM may not generate PCI disconnect if host attempts a read multiple command which reads beyond register address 0xFFF.

Description:

If a host incorrectly attempts a read multiple command whose address range spans beyond a point 4K bytes from the start of the FREEDM-32P672 register space, the FREEDM-32P672 may not issue a PCI disconnect and the PCI bus may hang.

Workarounds:

Ensure that the PCI host only accesses valid FREEDM-32P672 register addresses.

Performance with workaround:

FREEDM-32P672 works correctly.

Performance without workaround:

PCI bus may hang necessitating a system reset.

2.2. FREEDM may under-report number of Transmit FIFO underrun events if two such events occur close together.

Description:

The FREEDM-32P672 reports underrun events on a per-channel basis to the host by setting bit STATUS[2] when a TDR is returned to the TDR Free Queue. If a packet underflows near the end of the packet and the next packet on the same channel underflows near the start of the packet, it is possible that only one TDR is returned to the TDR Free Queue with STATUS[2] set even though 2 underrun events occurred.

Workarounds:

None.

Performance without workaround:

Per channel underrun events can occasionally go unreported.

3. Documentation Errors

This section lists the known documentation errors in Issue 5 of PMC-1990262 FREEDM-32P672 Datasheet (as of the publication date of this document).

Please report any documentation errors not covered in this document to PMC-Sierra.

3.1. PROV and DELIN bits in Register 0x204 are Write-Only

PROV and DELIN bits in Register 0x204 are write-only and not read/write. Changes to the register table are shown below.

Register 0x204 : RHDL Indirect Channel Data Register #1

Bit	Type	Function	Default
Bit 15	~~R/W~~ **W**	PROV	0
Bit 14	R/W	STRIP	0
Bit 13	~~R/W~~ **W**	DELIN	0
Bit 12	R	TAVAIL	X
Bit 11	W	Reserved	X
Bit 10	W	FPTR[10]	X
Bit 9	W	FPTR[9]	X
Bit 8	W	FPTR[8]	X
Bit 7	W	FPTR[7]	X
Bit 6	W	FPTR[6]	X
Bit 5	W	FPTR[5]	X
Bit 4	W	FPTR[4]	X
Bit 3	W	FPTR[3]	X
Bit 2	W	FPTR[2]	X
Bit 1	W	FPTR[1]	X
Bit 0	W	FPTR[0]	X

3.2. 7BIT, INVERT, CRC[1], and CRC[0] bits in Register 0x208 are Write-Only

7BIT, INVERT, CRC[1], and CRC[0] bits in Register 0x208 are write-only and not read/write. Changes to the register table are shown below.

Register 0x208 : RHDL Indirect Channel Data Register #2

Bit	Type	Function	Default
Bit 15	~~R/W~~ **W**	7BIT	0
Bit 14	R/W	PRIORITY	0
Bit 13	~~R/W~~ **W**	INVERT	0
Bit 12		Unused	X
Bit 11	~~R/W~~ **W**	CRC[1]	0
Bit 10	~~R/W~~ **W**	CRC[0]	0
Bit 9	R/W	OFFSET[1]	0
Bit 8	R/W	OFFSET[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	XFER[3]	0
Bit 2	R/W	XFER[2]	0
Bit 1	R/W	XFER[1]	0
Bit 0	R/W	XFER[0]	0

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NOTES

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