Ordering number : EN4742

CMOS LSI

LC72P32

One-Time Programmable ROM Single-Chip PLL Plus Microcontroller

Overview

The LC72P32 is a version of the LC7232N single-chip PLL plus microcontroller product that provides an 8 Kbyte (4096 words × 16 bits) one-time programmable ROM on chip. The LC72P32 has identical functions and the same pin assignment and packaging as the LC7232N, which is a mask ROM product. The LC72P32 can contribute to bringing up the first production run of a new product quickly and to reducing the switchover period when specifications change.

Features

- Option selection according to PROM data
  The LC7232N optional functions can be specified with PROM data. This allows mass-production products to be tested and evaluated.
- On-chip 8 Kbyte (4096 words × 16 bits) PROM
  This is a one-time programmable 8 Kbyte (4096 words × 16 bits) ROM.
- Packaging and pin assignments are identical to those of the LC7232N mask ROM version, i.e., these products are pin compatible.

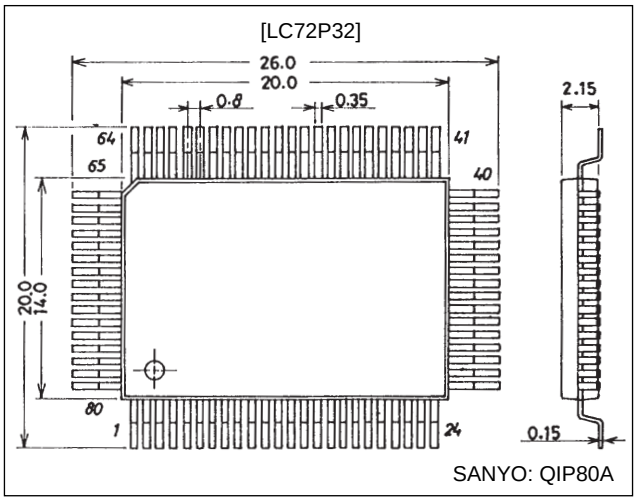
Sanyo PROM Writing Service

Sanyo provides custom PROM writing, printing, screening and read-back testing (for fee) services for our one-time programmable ROM microcontroller products. Contact your Sanyo sales representative for pricing and other details.

Package Dimensions

unit: mm

3044B-QFP80A



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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.5	V
Input voltage	$V_{IN}1$	$\overline{HOLD}$, $\overline{INT}$, $\overline{RES}$, ADI, $\overline{SNS}$, and the G port	–0.3 to +13	V
	$V_{IN}2$	Inputs other than $V_{IN}1$	–0.3 to V_{DD} + 0.3	V
Output voltage	$V_{OUT}1$	H port	–0.3 to +15	V
	$V_{OUT}2$	Outputs other than $V_{OUT}1$	–0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	D and H port pins	0 to 5	mA
	$I_{OUT}2$	E and F port pins	0 to 3	mA
	$I_{OUT}3$	B and C port pins	0 to 1	mA
	$I_{OUT}4$	S1 to S28 and I port pins	0 to 1	mA
Allowable power dissipation	Pd max	Topg = –30 to +70°C	400	mW
Operating temperature	Topg		–30 to +70	°C
Storage temperature	Tstg		–45 to +125	°C

Note: This IC has reduced resistance to damage from static discharges and therefore requires special care in handling.

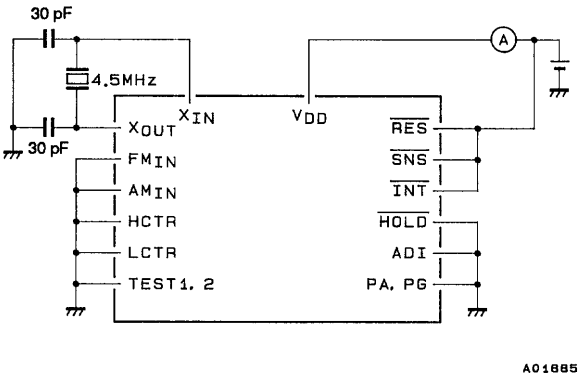
Allowable Operating Ranges at Ta = –30 to +70°C, V_{DD} = 4.0 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	CPU and PLL operating	4.5		5.5	V
	$V_{DD}2$	CPU operating	4.0		5.5	V
	$V_{DD}3$	Memory hold	1.3		5.5	V
Input high level voltage	$V_{IH}1$	G port	0.7 V_{DD}		8.0	V
	$V_{IH}2$	$\overline{RES}$, $\overline{INT}$, $\overline{HOLD}$	0.8 V_{DD}		8.0	V
	$V_{IH}3$	$\overline{SNS}$	2.5		8.0	V
	$V_{IH}4$	A port	0.6 V_{DD}		V_{DD}	V
	$V_{IH}5$	E and F ports	0.7 V_{DD}		V_{DD}	V
	$V_{IH}6$	LCTR (period measurement), $V_{DD}1$	0.8 V_{DD}		V_{DD}	V
Input low level voltage	$V_{IL}1$	G port	0		0.3 V_{DD}	V
	$V_{IL}2$	$\overline{RES}$, $\overline{INT}$	0		0.2 V_{DD}	V
	$V_{IL}3$	$\overline{SNS}$	0		1.3	V
	$V_{IL}4$	A port	0		0.2 V_{DD}	V
	$V_{IL}5$	E and F port	0		0.3 V_{DD}	V
	$V_{IL}6$	LCTR (period measurement), $V_{DD}1$	0		0.2 V_{DD}	V
	$V_{IL}7$	$\overline{HOLD}$	0		0.4 V_{DD}	V
Input frequency	$f_{IN}1$	XIN	4.0	4.5	5.0	MHz
	$f_{IN}2$	FMIN, $V_{IN}2$, $V_{DD}1$	10		130	MHz
	$f_{IN}3$	FMIN, $V_{IN}3$, $V_{DD}1$	10		150	MHz
	$f_{IN}4$	AMIN (L), $V_{IN}4$, $V_{DD}1$	0.5		10	MHz
	$f_{IN}5$	AMIN (H), $V_{IN}5$, $V_{DD}1$	2.0		40	MHz
	$f_{IN}6$	HCTR, $V_{IN}6$, $V_{DD}1$	0.4		12	MHz
	$f_{IN}7$	LCTR (frequency measurement), $V_{IN}7$ and $V_{DD}1$	100		500	kHz
	$f_{IN}8$	LCTR (period), $V_{IH}6$, $V_{IL}6$ and $V_{DD}1$	1		20×10^3	Hz
Input amplitude	$V_{IN}1$	XIN	0.50		1.5	Vrms
	$V_{IN}2$	FMIN	0.10		1.5	Vrms
	$V_{IN}3$	FMIN	0.15		1.5	Vrms
	$V_{IN}4$, 5	AMIN	0.10		1.5	Vrms
	$V_{IN}6$, 7	LCTR, HCTR	0.10		1.5	Vrms
Input voltage range	$V_{IN}8$	ADI	0		V_{DD}	V

Electrical Characteristics for the Allowable Operating Ranges

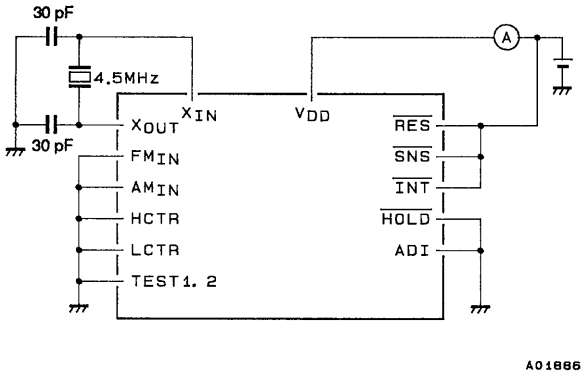
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	LCTR (period), $\overline{RES}$, $\overline{INT}$	0.1 V_{DD}			V
Reject pulse width	P_{REJ}	$\overline{SNS}$			50	µs
Power-down detection voltage	V_{DET}		3.0	3.5	4.0	V
Input high level current	$I_{IH}1$	$\overline{HOLD}$, $\overline{INT}$, $\overline{RES}$, ADI, $\overline{SNS}$, and the G port: V_I = 5.5 V			3.0	µA
	$I_{IH}2$	A, E and F ports: E and F ports output off, A port with no R_{PD}: $V_I = V_{DD}$			3.0	µA
	$I_{IH}3$	XIN: $V_I = V_{DD}$ = 5.0 V	2.0	5.0	15	µA
	$I_{IH}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD}$ = 5.0 V	4.0	10	30	µA
	$I_{IH}5$	A port: with R_{PD}: $V_I = V_{DD}$ = 5.0 V		50		µA
Input low level current	$I_{IL}1$	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, and the G port: $V_I = V_{SS}$			3.0	µA
	$I_{IL}2$	A, E and F ports: E and F ports output off, A port with no R_{PD}: $V_I = V_{SS}$			3.0	µA
	$I_{IL}3$	XIN: $V_{IN} = V_{SS}$	2.0	5.0	15	µA
	$I_{IL}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$	4.0	10	30	µA
Input floating voltage	V_{IF}	A port: with R_{PD}			0.05 V_{DD}	V
Pull-down resistance	R_{PD}	A port: with R_{PD}, V_{DD} = 5.0 V	75	100	200	kΩ
Output high level off leakage current	$I_{OFFH}1$	EO1, EO2: $V_O = V_{DD}$		0.01	10	nA
	$I_{OFFH}2$	B, C, D, E, F, and I ports: $V_O = V_{DD}$			3.0	µA
	$I_{OFFH}3$	H port: V_O = 13 V			5.0	µA
Output low level off leakage current	$I_{OFFL}1$	EO1, EO2: $V_O = V_{SS}$		0.01	10	nA
	$I_{OFFL}2$	B, C, D, E, F, and I ports: $V_O = V_{SS}$			3.0	µA
Output high level voltage	$V_{OH}1$	B and C ports: I_O = –1 mA	V_{DD} – 2.0	V_{DD} – 1.0	V_{DD} – 0.5	V
	$V_{OH}2$	E and F ports: I_O = –1 mA	V_{DD} – 1.0			V
	$V_{OH}3$	EO1, EO2: I_O = –500 µA	V_{DD} – 1.0			V
	$V_{OH}4$	XOUT: I_O = –200 µA	V_{DD} – 1.0			V
	$V_{OH}5$	S1 to S28 and I port: I_O = –0.1 mA	V_{DD} – 1.0			V
	$V_{OH}6$	D port: I_O = –5 mA	V_{DD} – 1.0			V
	$V_{OH}7$	COM1, COM2: I_O = –25 µA	V_{DD} – 0.75	V_{DD} – 0.5	V_{DD} – 0.3	V
Output low level voltage	$V_{OL}1$	B and C ports: I_O = 50 µA	0.5	1.0	2.0	V
	$V_{OL}2$	E and F ports: I_O = 1 mA			1.0	V
	$V_{OL}3$	EO1, EO2: I_O = 500 µA			1.0	V
	$V_{OL}4$	XOUT: I_O = 200 µA			1.0	V
	$V_{OL}5$	S1 to S28 and I port: I_O = 0.1 mA			1.0	V
	$V_{OL}6$	D port: I_O = 5 mA			1.0	V
	$V_{OL}7$	COM1, COM2: I_O = 25 µA	0.3	0.5	0.75	V
	$V_{OL}8$	H port: I_O = 5 mA	(150 Ω) 0.75		(400 Ω) 2.0	V
Output middle level voltage	V_M1	COM1, COM2: V_{DD} = 5.0 V, I_O = 20 µA	2.0	2.5	3.0	V
A/D conversion error		ADI, $V_{DD}1$	–1/2		1/2	LSB
Current drain	$I_{DD}1$	$V_{DD}1$, $f_{IN}2$ = 130 MHz		15	20	mA
	$I_{DD}2$	V_{DD} = 5.0 V, PLL stopped, CT = 2.67 µs (HOLD mode, Figure 1)		2.7		mA
	$I_{DD}3$	V_{DD} = 5.0 V, PLL stopped, CT = 13.33 µs (HOLD mode, Figure 1)		1.7		mA
	$I_{DD}4$	V_{DD} = 5.0 V, PLL stopped, CT = 40.00 µs (HOLD mode, Figure 1)		1.5		mA
	$I_{DD}5$	V_{DD} = 5.5 V, oscillator stopped, Ta = 25°C (BACKUP mode, Figure 2)			5	µA
		V_{DD} = 2.5 V, oscillator stopped, Ta = 25°C (BACKUP mode, Figure 2)			1	µA

Test Circuits



Note: With PB to PF, PH and PI all open. Note that output mode is selected for PE and PF.

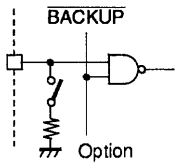
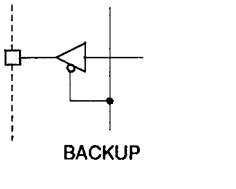
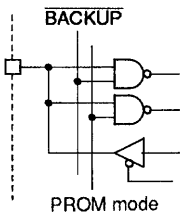
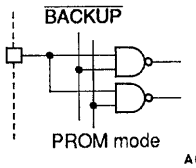
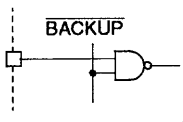
Figure 1 $I_{DD}2$ to $I_{DD}4$ in HOLD Mode



Note: With PA to PI, S1 to S24, COM1 and COM2 open.

Figure 2 $I_{DD}5$ in BACKUP Mode

Pin Functions

Pin	Pin No.	Function	I/O	Circuit type	PROM mode function
PA0 PA1 PA2 PA3	35 34 33 32	Low threshold type dedicated input port These pins can be used, for example, for key data acquisition. Built-in pull-down resistors can be specified as an option. This option is in 4-pin units, and cannot be specified for individual pins. Input through these pins is disabled in BACKUP mode.	Input		
PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	30 29 28 27 26 25 24 23	Dedicated output ports Since the output transistor impedances are unbalanced CMOS, these pins can be effectively used for functions such as key scan timing. These pins go to the output high-impedance state in BACKUP mode. These pins go to the low level during a reset, i.e., when the $\overline{RES}$ pin is low.	Output		
PD0 PD1 PD2 PD3	22 21 20 19	Dedicated output port These are normal CMOS outputs. These pins go to the output high-impedance state in BACKUP mode. These pins go to the low level during a reset, i.e., when the $\overline{RES}$ pin is low.			
PE0 PE1 PE2 PE3	18 17 16 15	I/O port These pins are switched between input and output as follows. Once an input instruction (IN, TPT, or TPF) is executed, these pins latch in the input mode. Once an output instruction (OUT, SPB, or RPB) is executed, they latch in the output mode. These pins go to the input mode during a reset, i.e., when the $\overline{RES}$ pin is low. In BACKUP mode these pins go to the input mode with input disabled.	I/O		Data I/O PE0: D0 PE1: D1 PE2: D2 PE3: D3 PF0: D4 PF1: D5 PF2: D6 PF3: D7
PF0 PF1 PF2 PF3	14 13 12 11	I/O port These pins are switched between input and output by the FPC instruction. The I/O states of this port can be specified for individual pins. These pins go to the input mode during a reset, i.e., when the $\overline{RES}$ pin is low. In BACKUP mode these pins go to the input mode with input disabled.			
PG0 PG1	6 5	Dedicated input port Input through these pins is disabled in BACKUP mode.	Input		PROM control signal inputs PG0: $\overline{CE}$ PG1: $\overline{OE}$
PG2 PG3	4 3				

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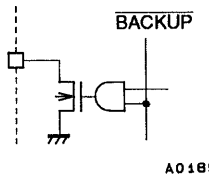
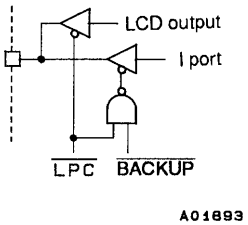
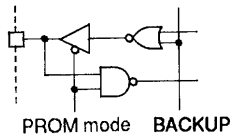
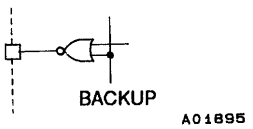
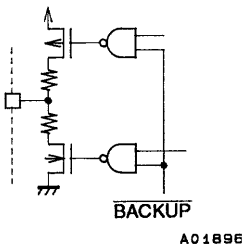
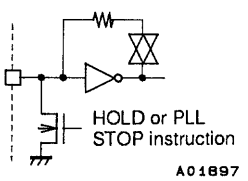
Pin	Pin No.	Function	I/O	Circuit type	PROM mode function
PH0 PH1 PH2 PH3	10 9 8 7	Dedicated output port Since these pins are high breakdown voltage n-channel transistor open-drain outputs, they can be effectively used for functions such as band power supply switching. Note that PH2 and PH3 also function as the DAC1 and DAC2 outputs. These pins go to the high impedance state during a reset, i.e., when the $\overline{RES}$ pin is low, and in BACKUP mode.	Output		
PI0/S25 PI1/S26 PI2/S27 PI3/S28	39 38 37 36	Dedicated output port While these pins have a CMOS output circuit structure, they can be switched to function as LCD drivers. Their function is switched by the SS and RS instructions. These pins cannot be switched individually. The LCD driver function is selected and a segment off signal is output when power is first applied or when $\overline{RES}$ is low. These pins are held at the low level in BACKUP mode. Note that when the general-purpose port use option is specified, these pins output the contents of IPORT when LPC is 1, and the contents of the general-purpose output port LATCH when LPC is 0.	Output		
S1 to S14	63 to 50	LCD driver segment outputs A frame frequency of 100 Hz and a 1/2 duty, 1/2 bias drive type are used. A segment off signal is output when power is first applied or when $\overline{RES}$ is low. These pins are held at the low level in BACKUP mode. The use of these pins as general-purpose output ports can be specified as an option.	I/O		Address input S: A0 to S14: A13
S15 to S24	49 to 40		Output		
COM1 COM2	65 64	LCD driver common outputs A 1/2 duty, 1/2 bias drive type is used. The output when power is first applied or when $\overline{RES}$ is low is identical to the normal operating mode output. These pins are held at the low level in BACKUP mode.	Output		
FMIN	74	FM VCO (local oscillator) input The input must be capacitor-coupled. The input frequency range is from 10 to 130 MHz.	Input		
AMIN	75	AM VCO (local oscillator) input The input should be capacitor-coupled. The band supported by this pin can be selected using the PLL instruction. High (2 to 40 MHz) → SW Low (0.5 to 10 MHz) → LW and MW			

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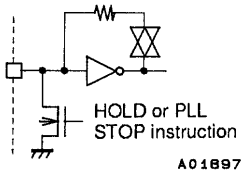
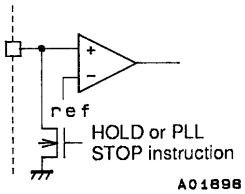
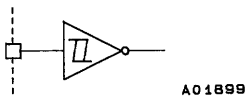
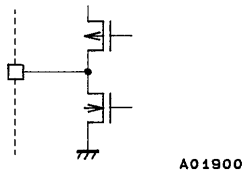
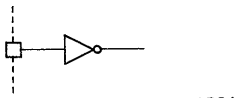
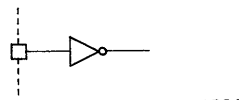
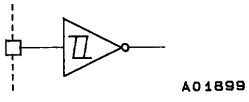
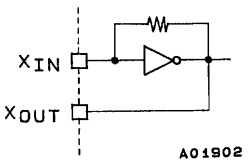
Pin	Pin No.	Function	I/O	Circuit type	PROM mode function
HCTR	70	Universal counter input The input should be capacitor-coupled. The input frequency range is from 0.4 to 12 MHz. This input can be effectively used for FM IF or AM IF counting.	Input		
LCTR	71	Universal counter input The input should be capacitor-coupled for input frequencies in the range 100 to 150 kHz. Capacitor coupling is not required for input frequencies from 1 to 20 Hz. This input can be effectively used for AM IF counting.			
ADI	69	A/D converter input A 1.28 ms period is required for a 6-bit sequential comparison conversion. The full scale input is ((63/96) · V_{DD}) for a data value of 3FH.	Input		
$\overline{INT}$	66	Interrupt request input An interrupt is generated when the INTEN flag is set (by an SS instruction) and a falling edge is input.	Input		
EO1 EO2	77 78	Reference frequency and programmable divisor phase comparison error outputs Charge pump circuits are built in. EO1 and EO2 are the same.	Output		
$\overline{SNS}$	72	Input pin used to determine if a power outage has occurred in BACK UP mode This pin can also be used as a normal input port.	Input		
$\overline{HOLD}$	67	Input pin used to force the LC72E32 to HOLD mode The LC72E32 goes to HOLD mode when the HOLDEN flag is set (by an SS instruction) and the $\overline{HOLD}$ input goes low. A high breakdown voltage circuit is used so that this input can be used in conjunction with the normal power switch.	Input		
$\overline{RES}$	68	System reset input This signal should be held low for 75 ms after power is first applied to effect a power-up reset. The reset starts when a low level has been input for at least six reference clock cycles.	Input		
XIN XOUT	1 80	Crystal oscillator connections (4.5 MHz) A feedback resistor is built in.	Input Output		
TEST1 TEST2	79 2	LSI test pins. These pins must be connected to V_{SS}.			
V_{DD}	31, 73	Power supply + connections. Both pins must be connected.			Programming voltage Vpp
V_{SS}	76	Power supply – connection.			

Option

No.	Description	Selections
1	WDT (watchdog timer) inclusion selection	WDT included
		No WDT
2	Port A pull-down resistor inclusion selection	Pull-down resistors included
		No pull-down resistors
3	Cycle time selection	2.67 µs
		13.33 µs
		40.00 µs
4	LCD port/general-purpose port selection	LCD ports
		General-purpose output ports

Usage Notes

The LC72P32 is provided for use in early production runs of products designed for the LC7232N. Please keep the following points in mind when using this product.

1. Differences between the LC72P32 and the LC7232N

Parameter		LC72P32	LC7232N
Operating temperature (Topr)		–30 to +70 °C	–40 to +85°C
Operation immediately following power on		After the 75 ms power-on reset period, the LSI internal option settings are set up during a period of about 1 ms. After that operation completes, program execution starts with the program counter set to location 0.	After the 75 ms power-on reset period, program execution starts with the program counter set to location 0.
Input type of the A port immediately following power on*		No pull-down resistors	Pull-down resistors are included or not according to the option specifications.
Output type of the S1 to S28 outputs immediately following power on*		LCD ports	These pins function as either LCD ports or general-purpose output ports according to the option specifications.
Power-down detection voltage (V_{DET})		Minimum: 3.0 V Typical 3.5 V Maximum: 4.0 V	Minimum: 2.7 V Typical: 3.0 V Maximum: 3.3 V
Current drain	$I_{DD}2$	Conditions: V_{DD} = 5.0 V, PLL stopped CT = 2.67 µs (HOLD mode, Figure 1) Typical: 2.7 mA	Conditions: $V_{DD}2$, PLL stopped CT = 2.67 µs (HOLD mode, Figure 1) Typical: 1.5 mA
	$I_{DD}3$	Conditions: V_{DD} = 5.0 V, PLL stopped CT = 13.33 µs (HOLD mode, Figure 1) Typical: 1.7 mA	Conditions: $V_{DD}2$, PLL stopped CT = 13.33 µs (HOLD mode, Figure 1) Typical: 1.0 mA
	$I_{DD}4$	Conditions: V_{DD} = 5.0 V, PLL stopped CT = 40.00 µs (HOLD mode, Figure 1) Typical: 1.5 mA	Conditions: $V_{DD}2$, PLL stopped CT = 40.00 µs (HOLD mode, Figure 1) Typical: 0.7 mA
The TEST1 and TEST2 pins		These are LSI test pins and must be connected to V_{SS}.	These are LSI test pins and must be either left open or connected to V_{SS}.
Supply voltage	$V_{DD}2$	Conditions: CPU operating Minimum: 4.0 V	Conditions: CPU operating Minimum: 3.5 V

Note: * This refers to the option setup time of about 1 ms that occurs following the period of about 75 ms from power application.

2. PLA and options

The LC72P32 uses locations 2000H to 201FH as program memory for PLA pattern specification, and locations 2020H to 2033H for option specification. This option specification allows the LC72P32 to support option setups identical to those available with the LC7232N.

- **LC72P32 Option Types**

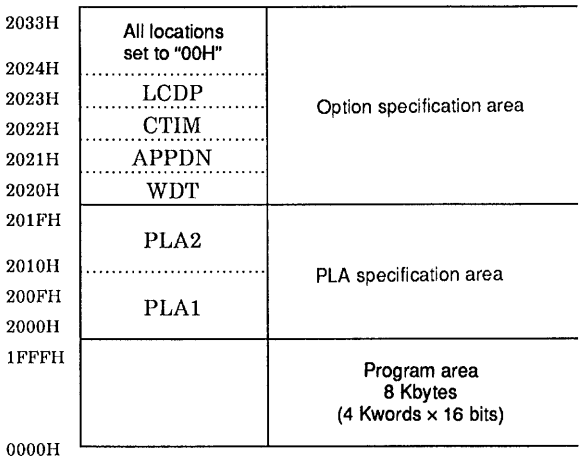
Symbol	Option Type	Selections
WDT	WDT (watchdog timer) inclusion selection	WDT included
		No WDT
APPDN	A port pull-down resistor inclusion selection	Pull-down resistors included
		No pull-down resistors
CTIM	Cycle time selection	2.67 µs
		13.33 µs
		40.00 µs
LCDP	LCD port/general-purpose port selection	LCD ports
		General-purpose output ports

Note that these options are not determined until the option setting period of about 1 ms, which follows a period of about 75 ms from power application, has passed.

3. Use of the mass-produced unit printed circuit board

When using the printed circuit board for the massed produced end product with the LC72P32, be sure to connect the TEST1 and TEST2 pins to V_{SS} and be sure to connect both pins 31 and 73 (the V_{DD} pins) to the plus side of the power supply.

4. PROM address space



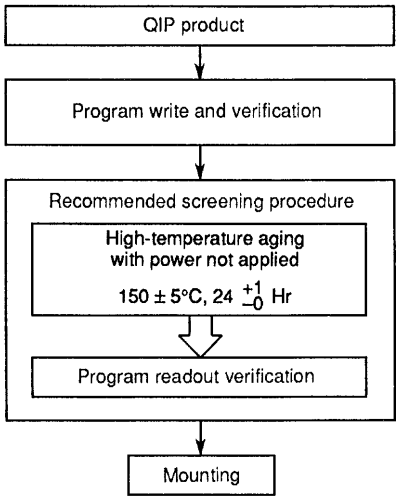
5. Notes on ordering ROM when using Sanyo's (for fee) PROM writing service

- When ordering one-time programmable and mask ROM versions at the same time
  The customer must provide a PROM to which the mask ROM version program and option data have been written. The customer must also provide ordering forms for both the mask ROM version and one-time programmable version products.

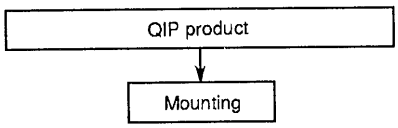
- When ordering only one-time programmable versions
  The customer must provide a PROM to which the one-time programmable version program and option data have been written. The customer must also provide ordering forms for the one-time programmable version product.

6. Conditions prior to mounting

- Use the procedure below for mounting unwritten PROM products.



- When Sanyo's (for fee) PROM writing service is used



Note: Due to the structure of microcontrollers with built-in one-time programmable PROM (unwritten PROM products), complete testing prior to shipment is not possible. Thus there are cases where the writing yield may be lower.

Usage Techniques

1. Writing the built-in PROM

The following two techniques can be used to write the LC72P32's built-in PROM.

- Using a general-purpose EPROM programmer

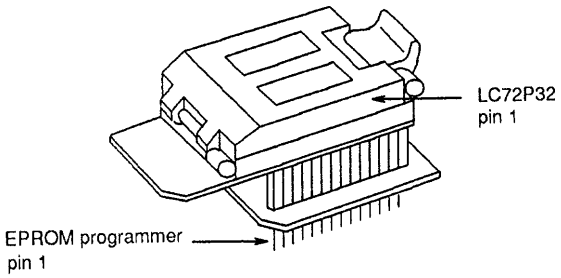
If a general-purpose EPROM programmer is used, the built-in PROM can be written by using a dedicated writing adapter available from Sanyo (product name: LC72E32 ADAPTER FOR EPROM PROGRAMMER). Note that the 27512 (Vpp = 12.5 V) Intel fast writing method should be used, and the address range should be set to locations 0 to 2033H.

- Using the RE32 in-circuit emulator

If the RE32 in-circuit emulator is used, the built-in PROM can be written by using a dedicated writing adapter available from Sanyo (product name: LC72E32 ADAPTER FOR RE32). Use the PGOTP command to write data to the PROM.

2. Dedicated writing adapter

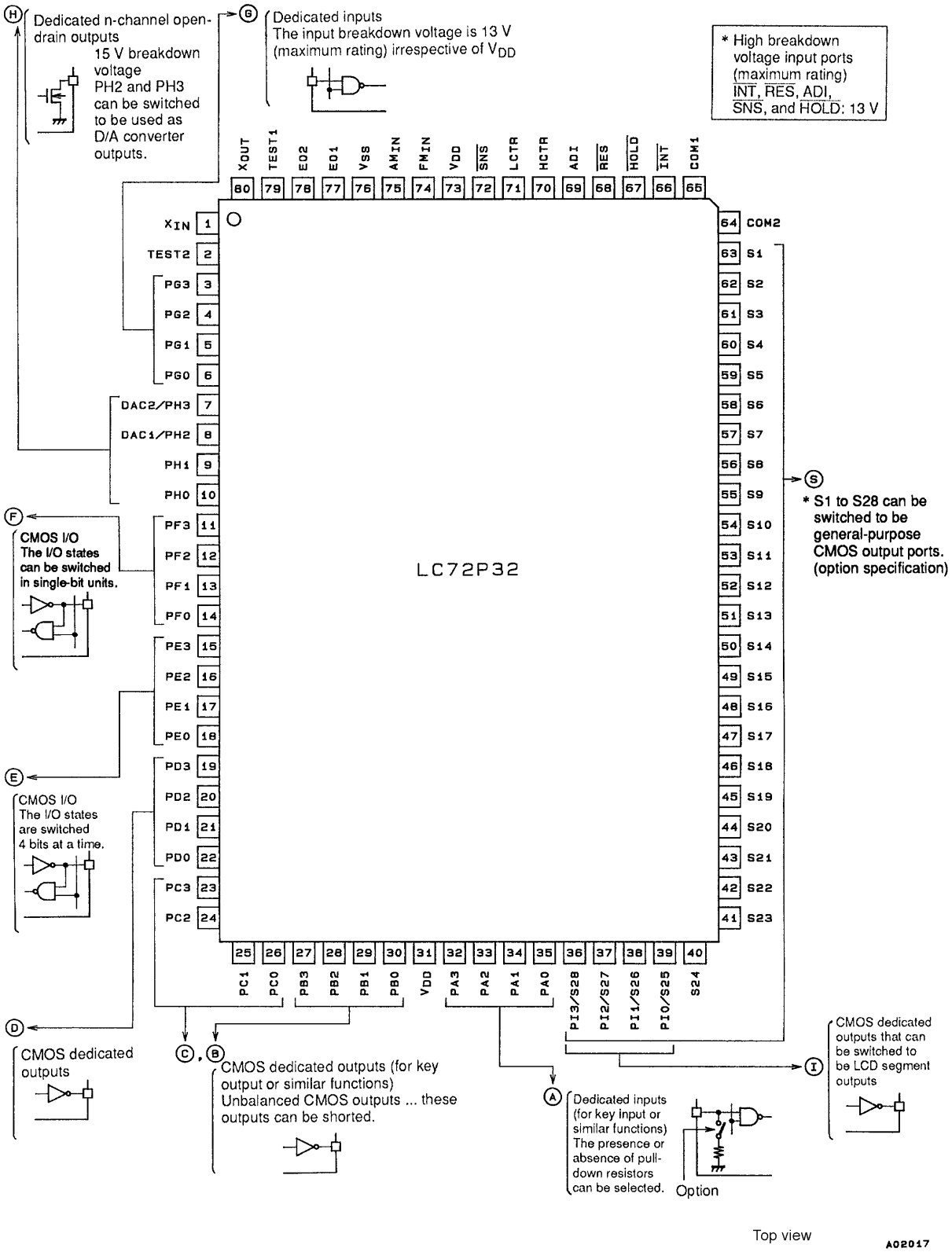
There are two writing adapters available for use with the LC72P32. These adapters are not interchangeable and each adapter must be used only for its intended purpose.



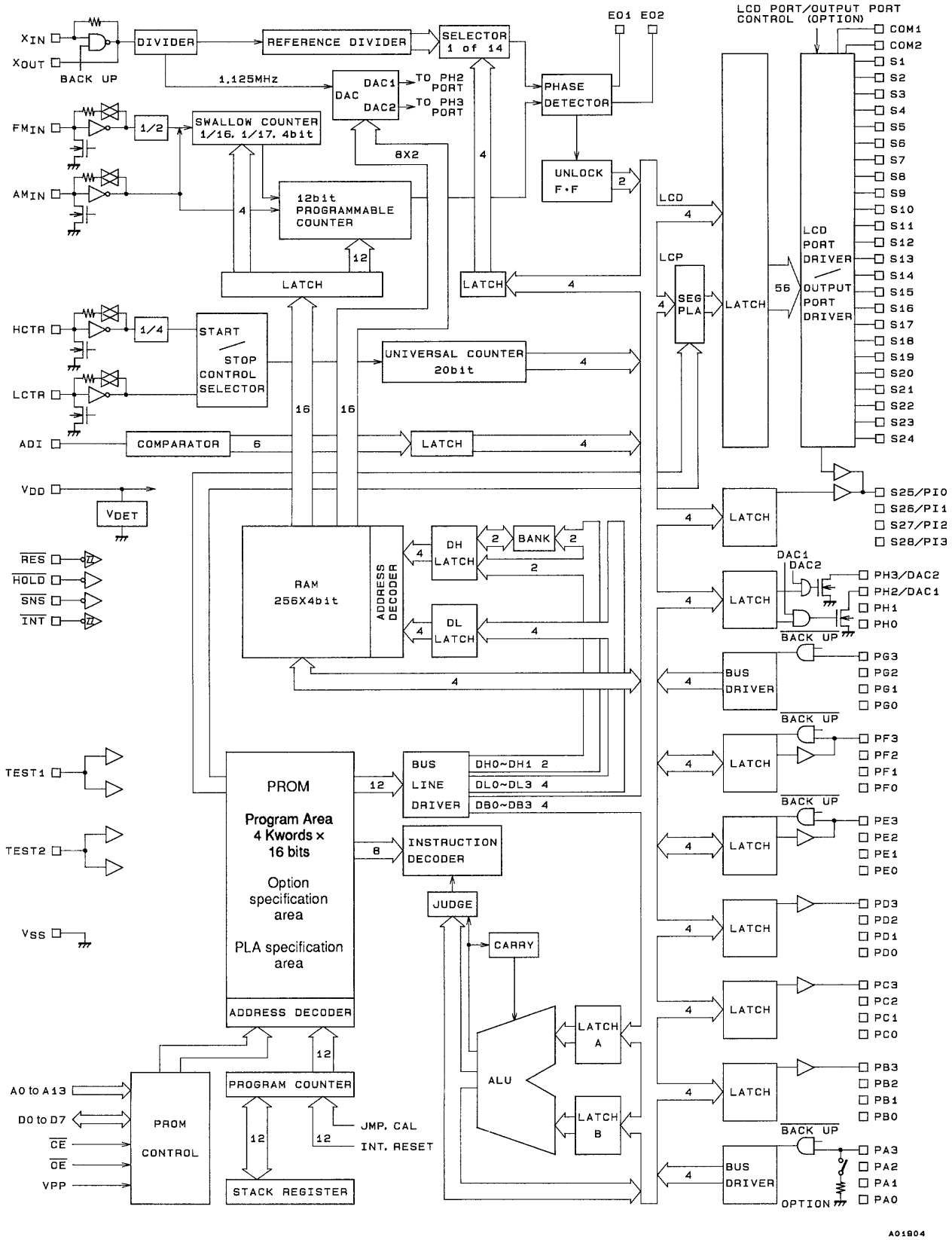
Note: The two writing adapters have essentially identical external appearances.

General-purpose EPROM programmer adapter:
Product name: LC72E32 Adapter for EPROM Programmer
Product code: NDK-DC-001-A
RE32 in-circuit emulator adapter:
Product name: LC72E32 Adapter for RE32
Product code: NDK-DC-003-A

Pin Assignment



Block Diagram



LC72P32 Instruction Table

Abbreviations:
ADDR: Program memory address [12 bits]
b: Borrow
B: Bank number [2 bits]
C: Carry
DH: Data memory address high (row address) [2 bits]
DL: Data memory address low (column address) [4 bits]
I: Immediate data [4 bits]
M: Data memory address
N: Bit position [4 bits]
Pn: Port number [4 bits]
r: General register (one of the locations 00 to 0FH in bank 0)
Rn: Register number [4 bits]
( ): Contents of register or memory
( )n: Contents of bit N of register or memory

Instruction Group	Mnemonic	Operand		Function	Operation	Machine code															
		1st	2nd			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0
Addition instructions	AD	r	M	Add M to r	r ← (r) + (M)	0	1	0	0	0	0	DH		DL				Rn			
	ADS	r	M	Add M to r, then skip if carry	r ← (r) + (M) skip if carry	0	1	0	0	0	1	DH		DL				Rn			
	AC	r	M	Add M to r with carry	r ← (r) + (M) + C	0	1	0	0	1	0	DH		DL				Rn			
	ACS	r	M	Add M to r with carry, then skip if carry	r ← (r) + (M) + C skip if carry	0	1	0	0	1	1	DH		DL				Rn			
	AI	M	I	Add I to M	M ← (M) + I	0	1	0	1	0	0	DH		DL				I			
	AIS	M	I	Add I to M, then skip if carry	M ← (M) + I skip if carry	0	1	0	1	0	1	DH		DL				I			
	AIC	M	I	Add I to M with carry	M ← (M) + I + C	0	1	0	1	1	0	DH		DL				I			
	AICS	M	I	Add I to M with carry, then skip if carry	M ← (M) + I + C skip if carry	0	1	0	1	1	1	DH		DL				I			
Subtraction instructions	SU	r	M	Subtract M from r	r ← (r) – (M)	0	1	1	0	0	0	DH		DL				Rn			
	SUS	r	M	Subtract M from r, then skip if borrow	r ← (r) – (M) skip if borrow	0	1	1	0	0	1	DH		DL				Rn			
	SB	r	M	Subtract M from r with borrow	r ← (r) – (M) – b	0	1	1	0	1	0	DH		DL				Rn			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	r ← (r) – (M) – b skip if borrow	0	1	1	0	1	1	DH		DL				Rn			
	SI	M	I	Subtract I from M	M ← (M) – I	0	1	1	1	0	0	DH		DL				I			
	SIS	M	I	Subtract I from M, then skip if borrow	M ← (M) – I skip if borrow	0	1	1	1	0	1	DH		DL				I			
	SIB	M	I	Subtract I from M with borrow	M ← (M) – I – b	0	1	1	1	1	0	DH		DL				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M ← (M) – I – b skip if borrow	0	1	1	1	1	1	DH		DL				I			
Comparison instructions	SEQ	r	M	Skip if r equals M	r – M skip if zero	0	0	0	0	0	1	DH		DL				Rn			
	SGE	r	M	Skip if r is greater than or equal to M	r – M skip if not borrow (r) ≥ (M)	0	0	0	0	1	1	DH		DL				Rn			
	SEQI	M	I	Skip if M equal to I	M – I skip if zero	0	0	1	1	0	1	DH		DL				I			
	SGEI	M	I	Skip if M is greater than or equal to I	M – I skip if not borrow (M) ≥ I	0	0	1	1	1	1	DH		DL				I			

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 D0
Logical operation instructions	AND	M	I	AND I with M	M ← (M) ∧ I	0 0 1 1	0 0	DH	DL	I
	OR	M	I	OR I with M	M ← (M) ∨ I	0 0 1 1	1 0	DH	DL	I
	EXL	r	M	Exclusive OR M with r	r ← (r) ⊕ (M)	0 0 1 0	0 0	DH	DL	Rn
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 0 0 0	0 0	DH	DL	Rn
	ST	M	r	Store r to M	M ← (r)	1 0 0 0	0 1	DH	DL	Rn
	MVRD	r	M	Move M to destination M referring to r in the same row	[DH, Rn] ← (M)	1 0 0 0	1 0	DH	DL	Rn
	MVRS	M	r	Move source M referring to r to M in the same row	M ← [DH, Rn]	1 0 0 0	1 1	DH	DL	Rn
	MVSR	M1	M2	Move M to M in the same row	[DH, DL1] ← [DH, DL2]	1 0 0 1	0 0	DH	DL1	DL2
	MVI	M	I	Move I to M	M ← I	1 0 0 1	0 1	DH	DL	I
	PLL	M	r	Load M to PLL registers	PLL r ← PLL DATA	1 0 0 1	1 0	DH	DL	Rn
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all “1”, then skip	1 0 1 0	0 1	DH	DL	N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all “0”, then skip	1 0 1 0	1 1	DH	DL	N
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 1 1	ADDR (12 bits)			
	CAL	ADDR		Call subroutine	PC ← ADDR Stack ← (PC) + I	1 1 0 0	ADDR (12 bits)			
	RT			Return from subroutine	PC ← Stack	1 1 0 1	0 1	0 0	0 0 0 0	0 0 0 0
	RTI			Return from interrupt	PC ← Stack	1 1 0 1	0 1	0 1	0 0 0 0	0 0 0 0
F/F test instructions	TTM	N		Test timer F/F then skip if it has not been set	if timer F/F = “0”, then skip	1 1 0 1	0 1	1 0	0 0 0 0	N
	TUL	N		Test unlock F/F then skip if it has not been set	if UL F/F = “0”, then skip	1 1 0 1	0 1	1 1	0 0 0 0	N
Status register instructions	SS	N		Set status register	(Status register 1) N ← 1	1 1 0 1	1 1	0 0	0 0 0 0	N
	RS	N		Reset status register	(Status register 1) N ← 0	1 1 0 1	1 1	0 1	0 0 0 0	N
	TST	N		Test status register true	if (Status register 2) N = all “1”, then skip	1 1 0 1	1 1	1 0	0 0 0 0	N
	TSF	N		Test status register false	if (Status register 2) N = all “0”, then skip	1 1 0 1	1 1	1 1	0 0 0 0	N
Bank switching instructions	BANK	B		Select bank	BANK ← B	1 1 0 1	0 0	B	0 0 0 0	0 0 0 0

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0
I/O instructions	LCD	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1 1 1 0	0 0 DH	DL	DIGIT
	LCP	M	I	Output segment pattern to LCD digit through PLA	LCD (DIGIT) ← PLA ← M	1 1 1 0	0 1 DH	DL	DIGIT
	IN	M	P	Input port data to M	M ← (Port (P))	1 1 1 0	1 0 DH	DL	P
	OUT	M	P	Output contents of M to port	(Port (P)) ← M	1 1 1 0	1 1 DH	DL	P
	SPB	P	N	Set port bits	(Port (P)) N ← 1	1 1 1 1	0 0 0 0	P	N
	RPB	P	N	Reset port bits	(Port (P)) N ← 0	1 1 1 1	0 1 0 1	P	N
	TPT	P	N	Test port bits, then skip if all bits specified are true	if (Port (P)) N = all “1”, then skip	1 1 1 1	1 0 1 0	P	N
	TPF	P	N	Test port bits, then skip if all bits specified are false	if (Port (P)) N = all “0”, then skip	1 1 1 1	1 1 1 1	P	N
Universal counter instructions	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0	0 0 0 1	0 0 0 0	I
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0	0 0 1 1	0 0 0 0	I
Other instructions	FPC	N		F port I/O control	FPC latch ← N	0 0 0 1	0 0 0 0	0 0 0 0	N
	CKSTP			Clock stop	Stop clock if $\overline{\text{HOLD}}$ = 0	0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 0
	DAC	I		Load M to D/A registers	DAreg ← DAC DATA	0 0 0 0	0 0 1 0	0 0 0 0	I
	NOP			No operation		0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0