



LA4571MB

Low-voltage Headphone Amplifier for Stereo Audio

Overview

The LA4571MB is a low-voltage, stereo headphone amplifier incorporating both tape head preamplifiers and headphone power amplifiers in a single chip, making it ideal for portable battery-powered equipment. It features logic-level controlled output signal muting, excellent noise characteristics and easy interconnection with signal sources, such as an AM/FM tuner IC.

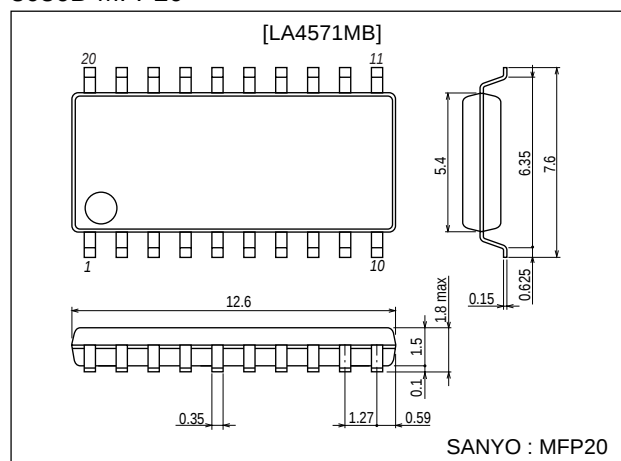
The LA4571MB requires no input or output coupling capacitors. A buffer amplifier with 10Ω output impedance reduces the size of the virtual-earth decoupling capacitor. The preamplifier and power amplifier inputs only require the addition of an external capacitor to provide high-frequency noise filtering.

The LA4571MB operates from a 3V supply and is available in 20-pin MFPs.

Package Dimensions

unit:mm

3036B-MFP20



Features

- Stereo tape head preamplifiers and headphone power amplifiers on chip.
- Output signal muting.
- Low noise.
- 8Ω speaker driver.
- 3V supply.
- 20-pin MFP.

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		4.5	V
Allowable power dissipation	P_d max		400	mW
Operating temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		3.0	V
Supply voltage range	V_{CC} op		1.8 to 3.6	V

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LA4571MB

Electrical Characteristics

Preamplifier and power amplifier at $T_a = 25^\circ\text{C}$, $V_{CC}=3.0\text{V}$, $f=1\text{kHz}$, R_L (pre)= $10\text{k}\Omega$, R_L (power)= 16Ω , 0dBm at 0.775V unless otherwise noted

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent supply current	I_{CCO}	$R_g=2.2\text{k}\Omega$, $V_I=0\text{V}$		17	27	mA
Total voltage gain	V_{GT}	$V_O=-5\text{dBm}$	65	68	71	dB

Preamplifier at $T_a = 25^\circ\text{C}$, $V_{CC}=3.0\text{V}$, $f=1\text{kHz}$, R_L (pre)= $10\text{k}\Omega$, R_L (power)= 16Ω , 0dBm at 0.775V unless otherwise noted

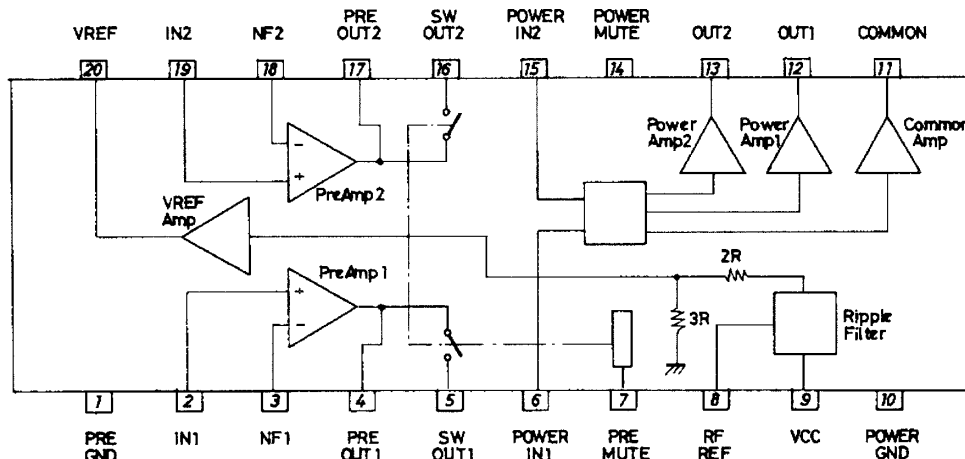
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Open-loop voltage gain	V_{GO}	$V_O=-5\text{dBm}$	70	80		dB
Closed-loop voltage gain	V_{G1}	$V_O=-5\text{dBm}$		40		dB
Maximum output voltage	$V_{O\text{ max}}$	$\text{THD}=1\%$, $V_{CC}=1.8\text{V}$	0.1	0.2		V
Total harmonic distortion	THD_1	$V_O=0.2\text{V}$, $V_G=40\text{dB}$ (NAB standard)		0.05	0.5	%
Input conversion noise voltage	V_{NI}	$R_g=2.2\text{k}\Omega$, bandwidth= 20Hz to 20kHz		1.3	2.0	μV
Channel crosstalk	CT_1	$R_g=2.2\text{k}\Omega$, 1kHz tune	60	80		dB
Ripple rejection	R_{r1}	$R_g=2.2\text{k}\Omega$, $V_{CC}=1.8\text{V}$, $V_I=-20\text{dBm}$, $f=100\text{Hz}$	40	50		dB

Power amplifier at $T_a = 25^\circ\text{C}$, $V_{CC}=3.0\text{V}$, $f=1\text{kHz}$, R_L (pre)= $10\text{k}\Omega$, R_L (power)= 16Ω , 0dBm at 0.775V unless otherwise noted

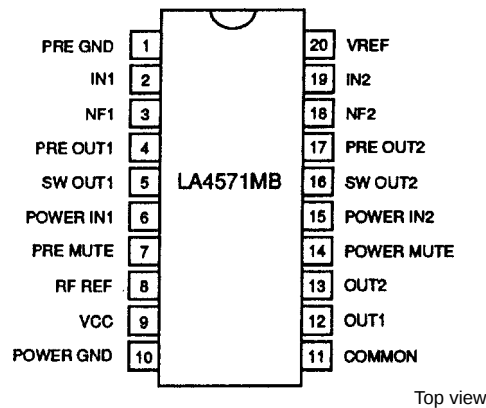
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output power	P_O	$\text{THD}=10\%$	23	32		mW
Closed-loop voltage gain	V_{G2}	$V_O=-5\text{dBm}$	25	28	31	dB
Total harmonic distortion	THD_2	$P_O=1\text{mW}$		0.4	1.0	%
Channel crosstalk	CT_T	$V_O=-5\text{dBm}$, $R_V=0\Omega$	30	40		dB
Output noise voltage	V_{NO}	$R_g=0\Omega$, $\text{BPF}=20\text{Hz}$ to 20kHz		24	40	μV
Ripple rejection	R_{r2}	$R_g=0\Omega$, $V_I=-20\text{dB}$, $f=100\text{Hz}$, $V_{CC}=1.8\text{V}$	45	60		dB
Input resistance	R_i		22	30	38	$\text{k}\Omega$
Output DC offset voltage	$V_{ODC\text{ off}}$		-90		+90	mV

Note : The maximum and minimum values for the power amplifiers closed-loop voltage gain (V_{G2}) increase by 1dB when the load resistance (R_L) is 32Ω .

Block Diagram



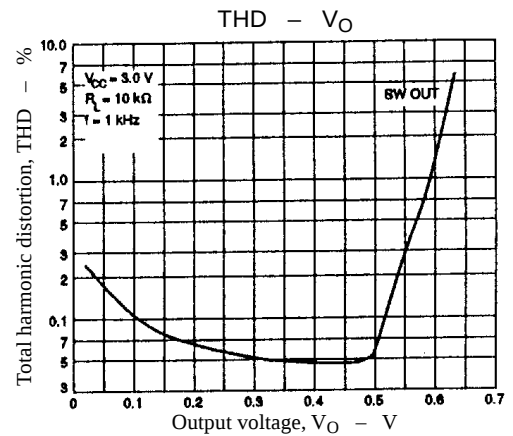
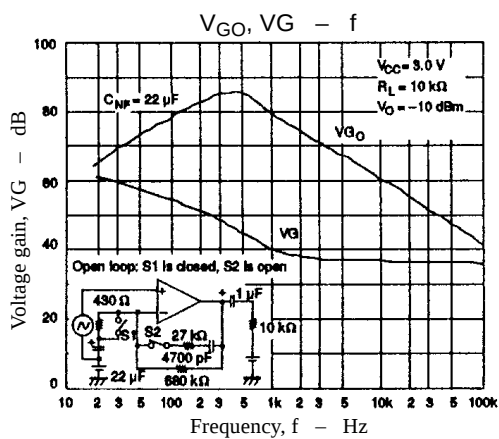
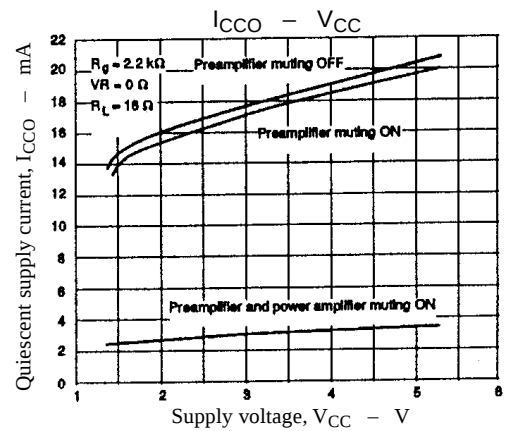
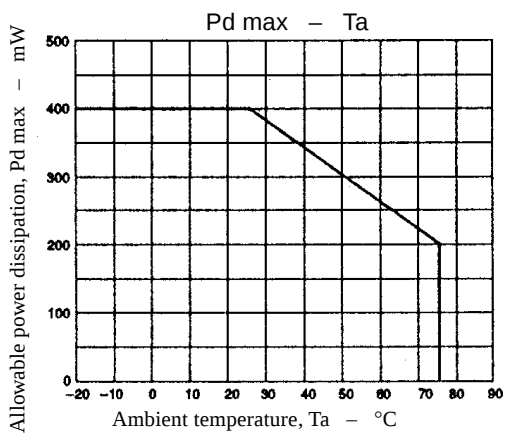
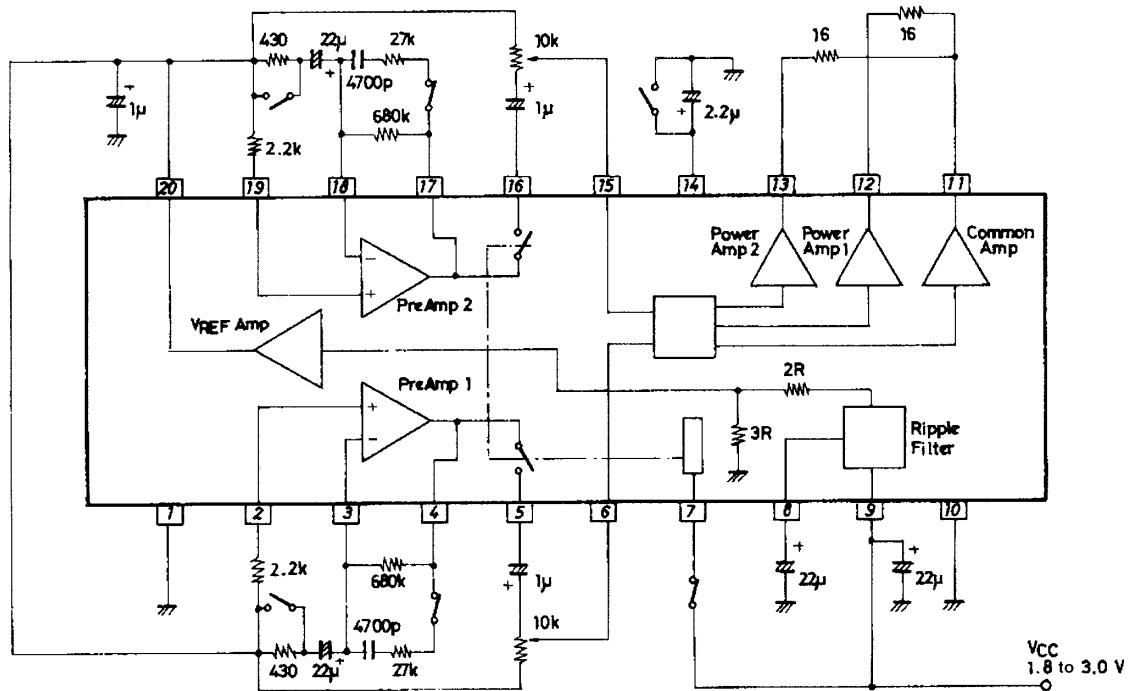
Pin Assignment

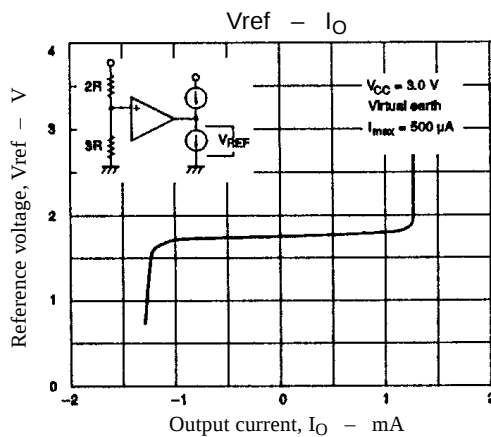
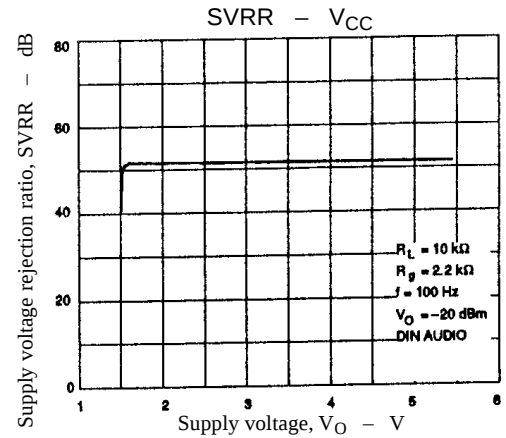
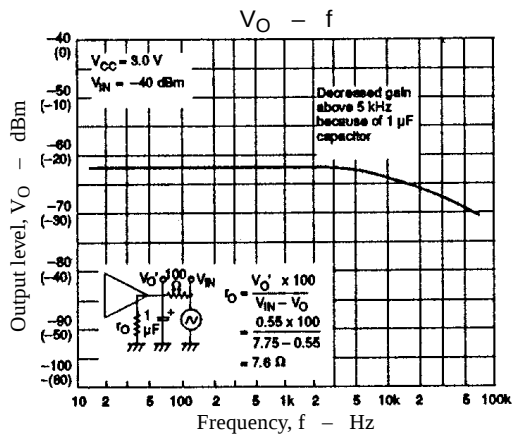
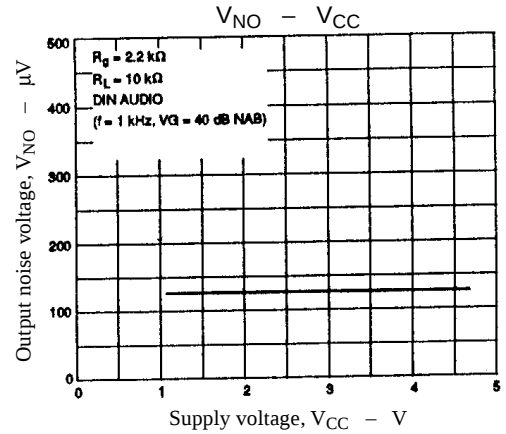
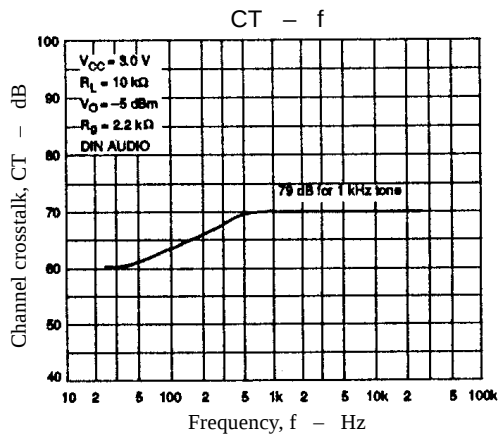
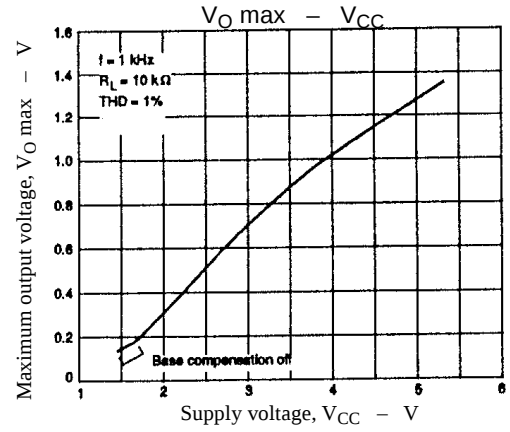
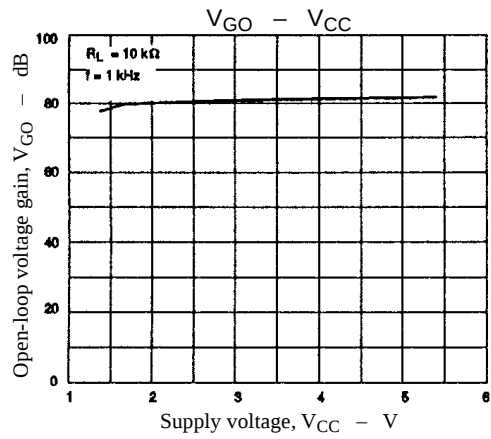


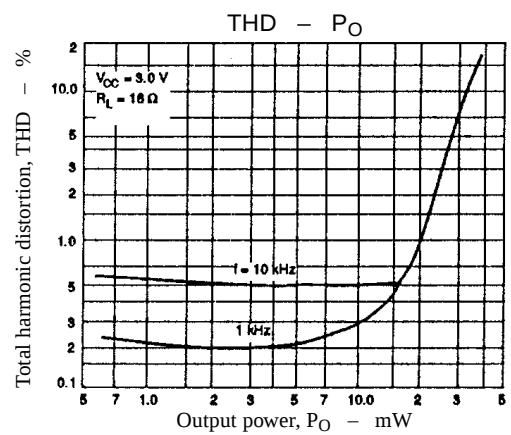
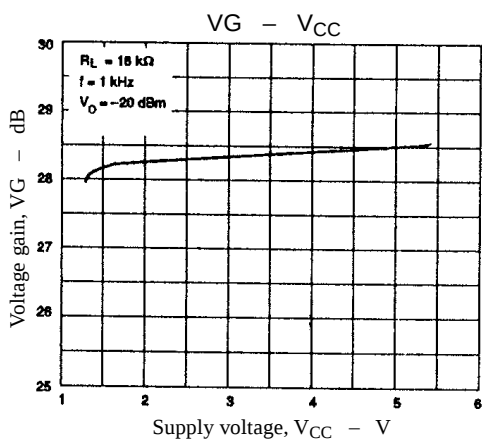
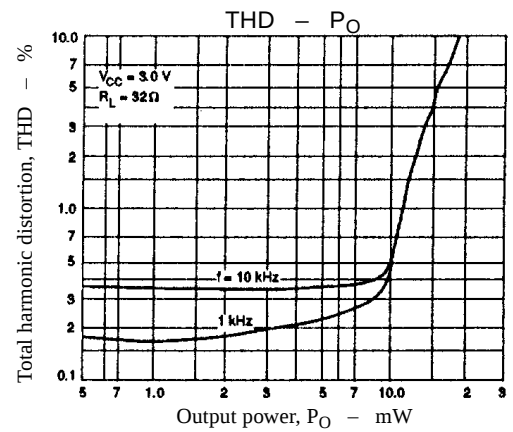
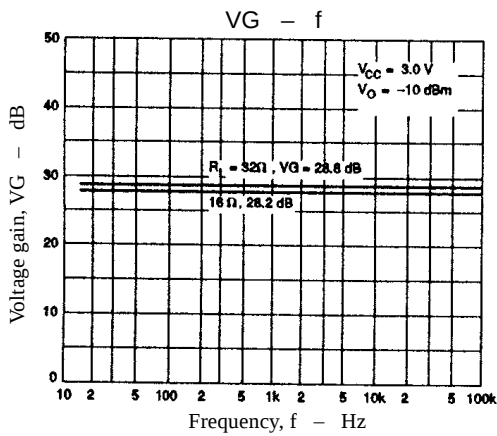
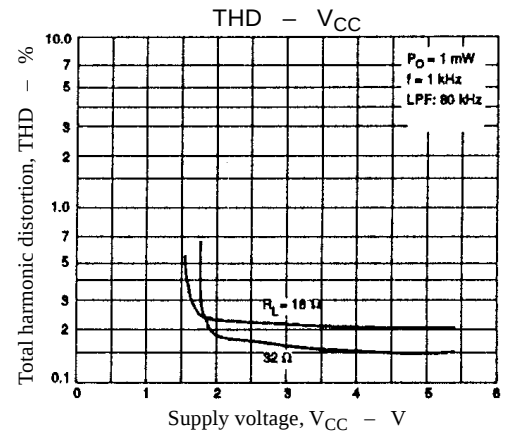
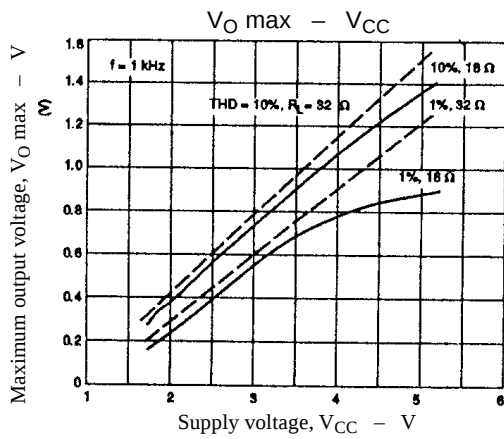
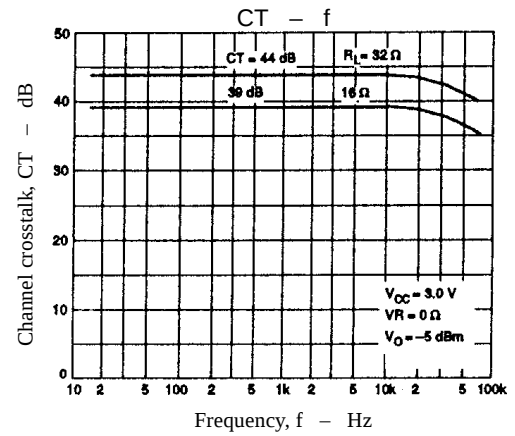
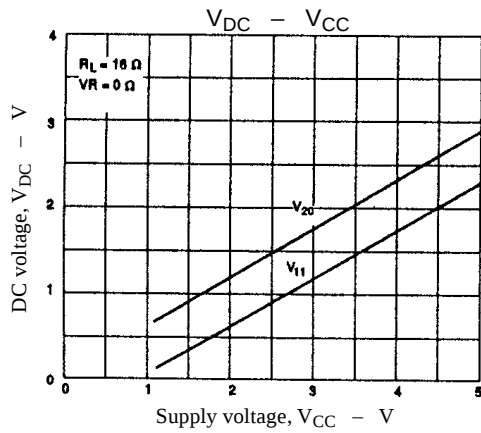
Pin Description

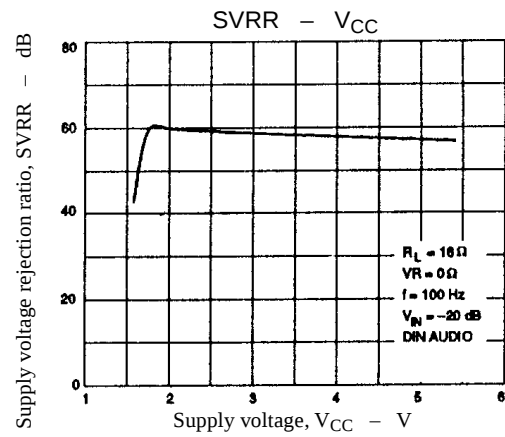
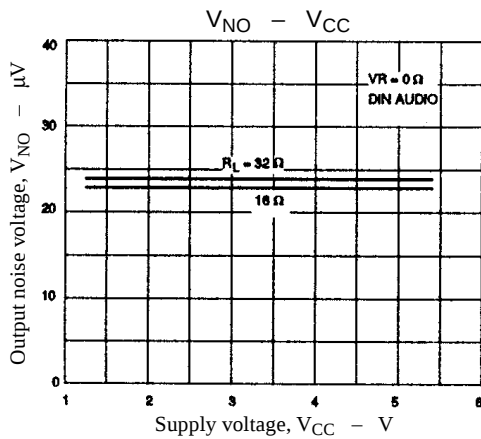
Number	Name	Description
1	PRE GND	Preamplifier ground
2	IN1	Channel 1 preamplifier input
3	NF1	Channel 1 preamplifier negative feedback input
4	PRE OUT1	Channel 1 preamplifier output
5	SW OUT1	Channel 1 preamplifier mute-control switched output $R_{IN} \geq 500k\Omega$
6	POWER IN1	Channel 1 power amplifier input. $R_{IN} \approx 30k\Omega$
7	PRE MUTE	Preamplifier mute control
8	RF REF	Ripple-filter capacitor connection
9	V _{CC}	Supply voltage
10	POWER GND	Power amplifier ground
11	COMMON	Common amplifier output
12	OUT1	Channel 1 power amplifier output
13	OUT2	Channel 2 power amplifier output
14	POWER MUTE	Power amplifier mute control
15	POWER IN2	Channel 2 power amplifier input. $R_{IN} \approx 30k\Omega$
16	SW OUT2	Channel 2 preamplifier mute-control switched output. $R_{IN} \geq 500k\Omega$
17	PRE OUT2	Channel 2 preamplifier output
18	NF2	Channel 2 preamplifier negative feedback input
19	IN2	Channel 2 preamplifier input
20	VREF	Reference-voltage amplifier output. $I_{max} = \pm 500\mu A$

Test Circuit









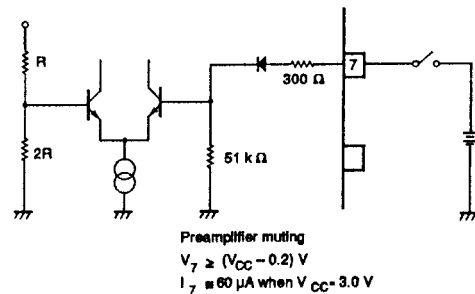
Functional Description (channel 1 only)

Tape Head Preamplifier

Tape head signal source are connected to the non-inverting input of the op-amp, negative feedback preamplifier.

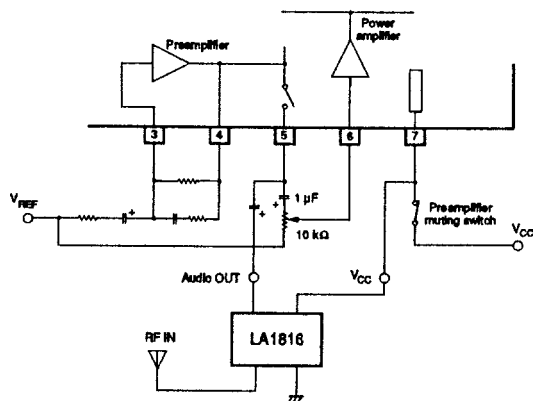
When PRE MUTE is open, the preamplifier output is connected to SW OUT1, and when PRE MUTE is HIGH ($V_{CC} \pm 0.2V$ at $60\mu A$ input current), SW OUT1 is open. This can be used to switch, or mute, the preamplifier output.

The internal circuit of the PRE MUTE pin is shown in the following figure.



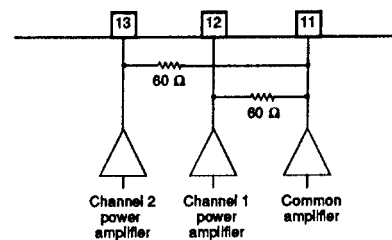
The output pins, PRE OUT1 and SW OUT1, can both drive a $10k\Omega$ load resistance.

The preamplifier input pin, IN1, the negative feedback input pin, NF1, and the output pin, PRE OUT, are biased at $1.8V$.



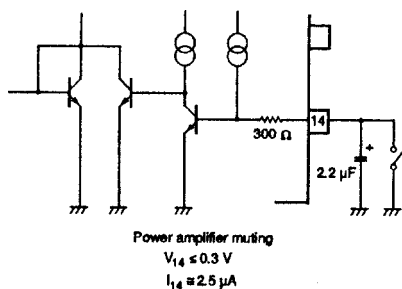
Power Amplifier

The power amplifier stage comprises an amplifier for each channel and a common amplifier. The power amplifier outputs are connected internally by 60Ω resistors to prevent oscillation, as shown in the following figure.



When POWER MUTE is LOW (less than $0.3V$ at $2.5\mu A$ input current), the power amplifier output signal is muted. The power amplifier mute release time is set by an external capacitor.

The internal circuit of the POWER MUTE pin is shown in the following figure.



The power amplifier input pin, POWER IN1, is biased at 1.8V, and the output pins at 1.2V

Design Notes

The preamplifier inputs should be connected to V_{REF} through a $2.2k\Omega$ resistor if there is no tape head input signal source.

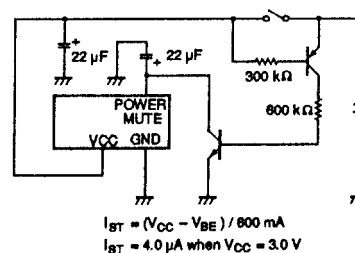
The mute release time capacitor of the power amplifier should be between 1.0 and $4.7\mu F$. For $V_{CC}=3.0V$ and $C=2.2\mu F$, the mute release time is 0.7s.

The ripple rejection ratio setting capacitor should be between 2.2 and $33\mu F$. For $2.2\mu F$, the ripple rejection ratio is 35dB, and for $22\mu F$, it is 55dB.

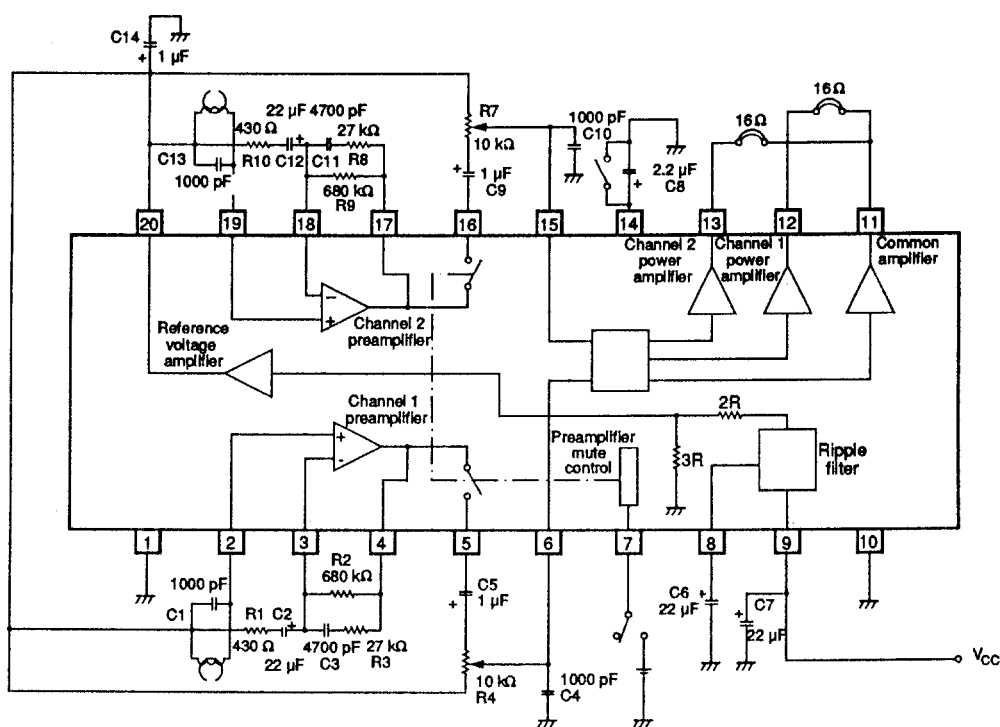
When the output amplifier turns OFF, the protection circuit shown in the following figure detects the falling supply voltage and then mutes the power amplifier to protect the device.

Reference Voltage

The input to the voltage reference amplifier is a voltage divided level from the supply voltage ripple filter. The reference voltage is given by $0.6 \times V_{CC}$. The supply voltage ripple filter requires the connection of an external filter capacitor to RF REF. A large capacitance results in a high ripple rejection ratio. Noise filtering is achieved by the addition of a single capacitor to V_{REF} . Since the reference voltage amplifier has a buffered output, this capacitor can be as low as $1\mu F$.



Sample Application Circuit



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