
2SJ543

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

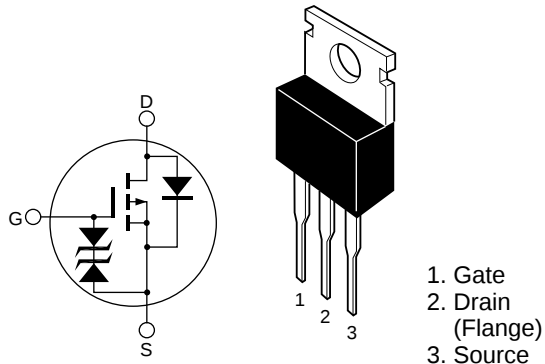
ADE-208-652B (Z)
3rd. Edition
June 1, 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.042\Omega$ typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

Outline

TO-220AB



2SJ543

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	−60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	−20	A
Drain peak current	I _{D(pulse)} ^{Note1}	−80	A
Body-drain diode reverse drain current	I _{DR}	−20	A
Avalanche current	I _{AP} ^{Note3}	−20	A
Avalanche energy	E _{AR} ^{Note3}	34	mJ
Channel dissipation	P _{ch} ^{Note2}	75	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	−55 to +150	°C

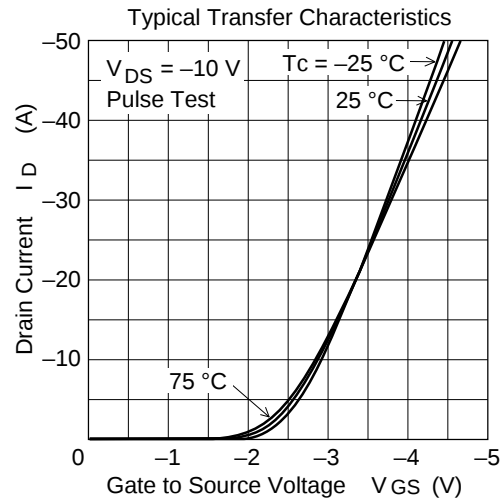
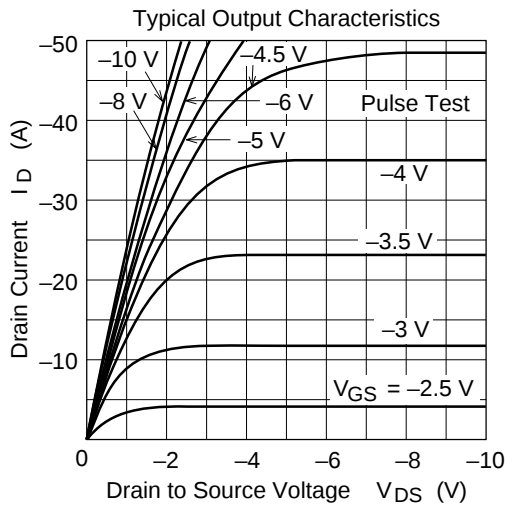
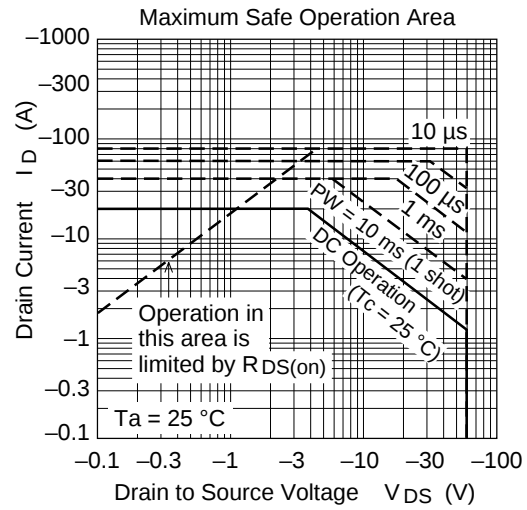
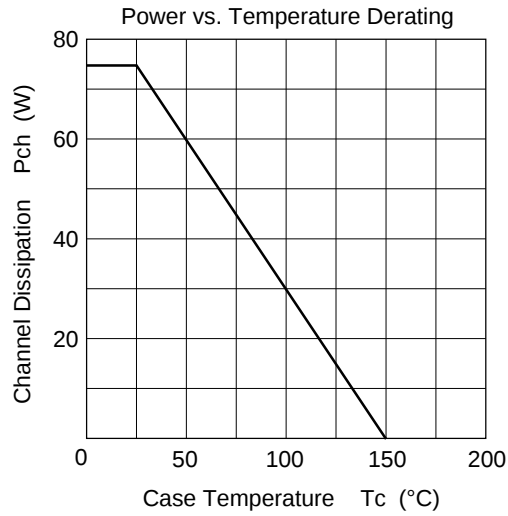
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

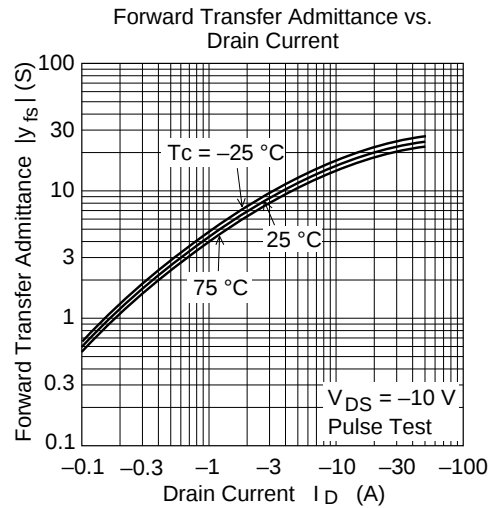
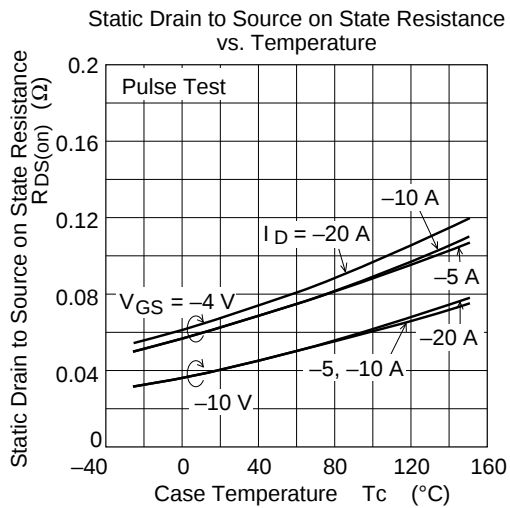
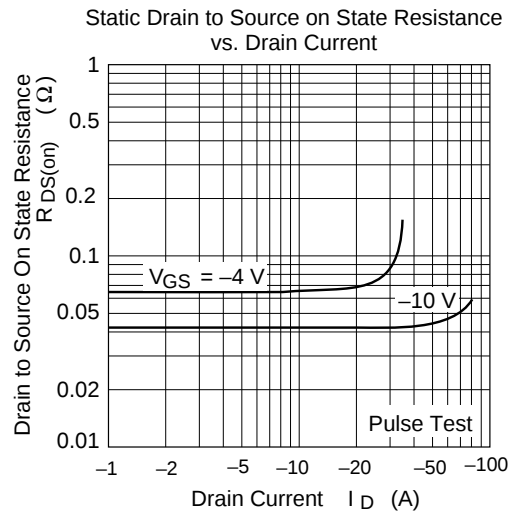
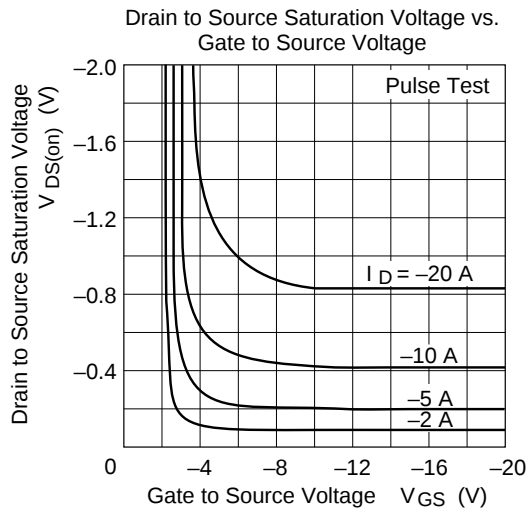
Electrical Characteristics (Ta = 25°C)

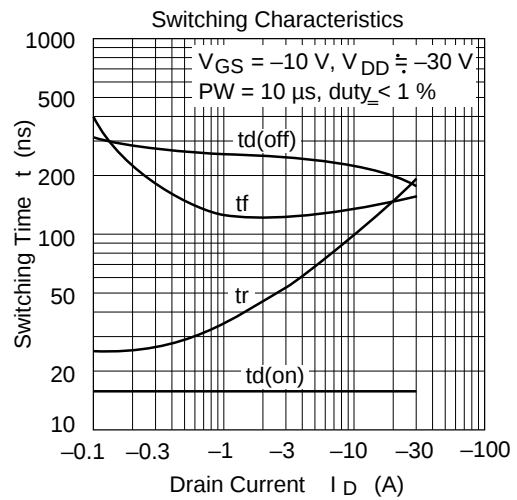
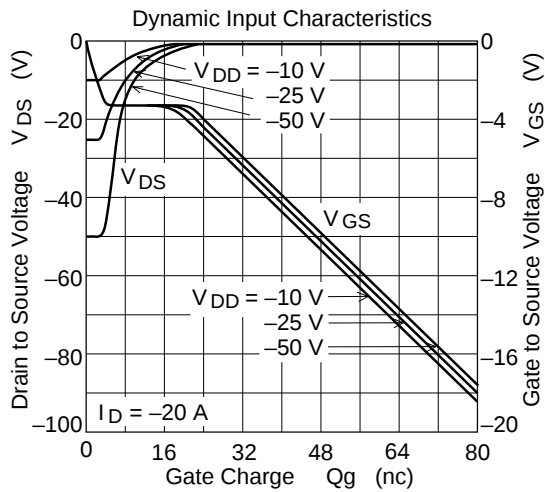
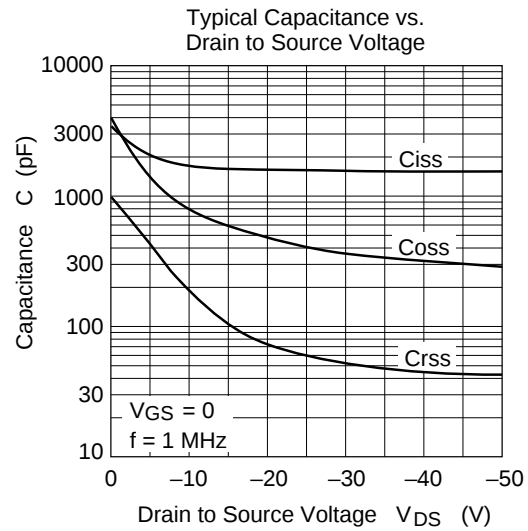
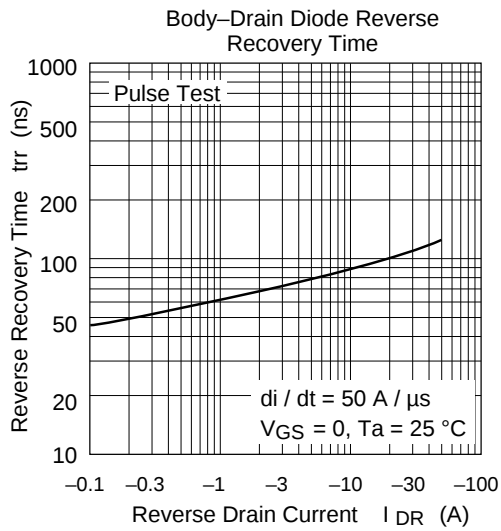
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}$, $V_{DS} = -10\text{V}$
Static drain to source on state	$R_{DS(on)}$	—	0.042	0.055	Ω	$I_D = -10\text{A}$, $V_{GS} = -10\text{V}$ ^{Note4}
resistance	$R_{DS(on)}$	—	0.065	0.095	Ω	$I_D = -10\text{A}$, $V_{GS} = -4\text{V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	10	16	—	S	$I_D = -10\text{A}$, $V_{DS} = -10\text{V}$ ^{Note4}
Input capacitance	C_{iss}	—	1750	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	C_{oss}	—	800	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	180	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	16	—	ns	$V_{GS} = -10\text{V}$, $I_D = -10\text{A}$
Rise time	t_r	—	100	—	ns	$R_L = 3\Omega$
Turn-off delay time	$t_{d(off)}$	—	230	—	ns	
Fall time	t_f	—	140	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-1.0	—	V	$I_F = -20\text{A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	100	—	ns	$I_F = -20\text{A}$, $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

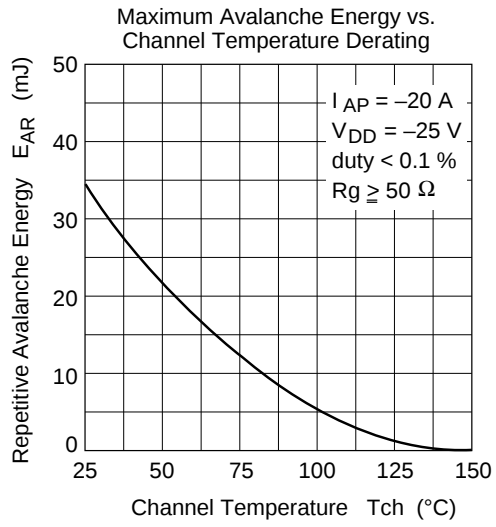
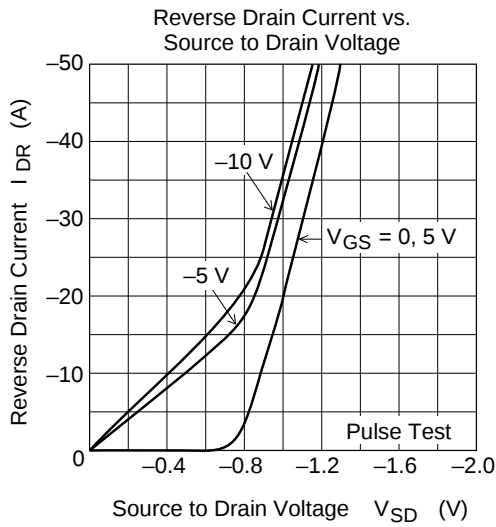
Note: 4. Pulse test

Main Characteristics

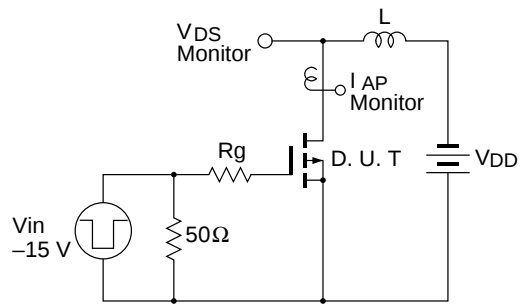






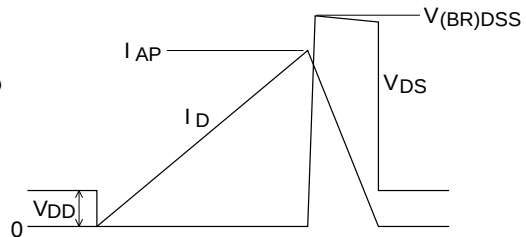


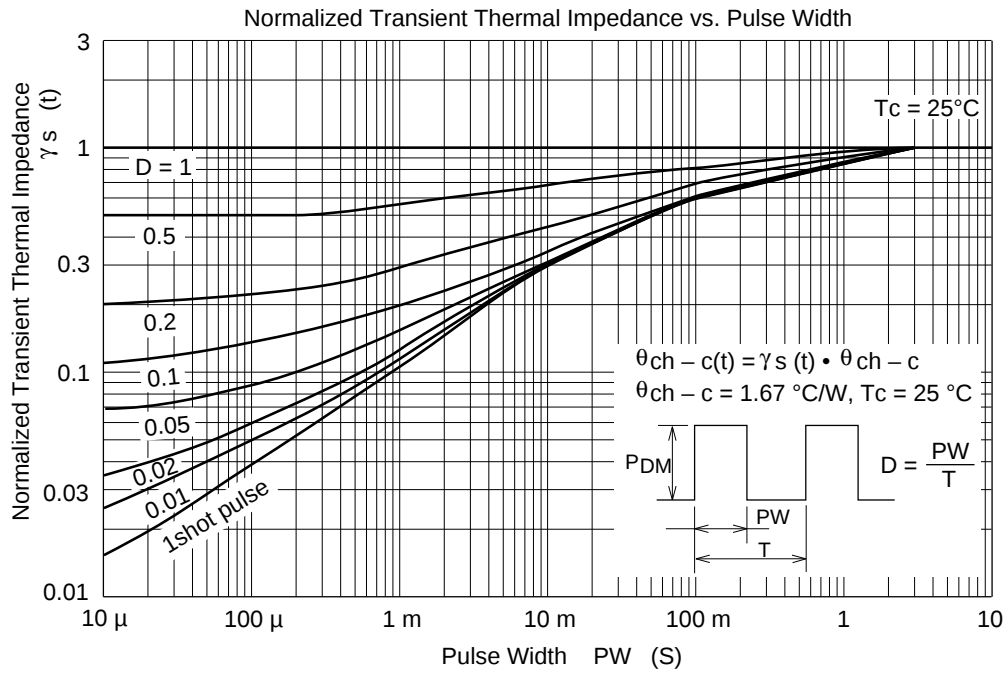
Avalanche Test Circuit



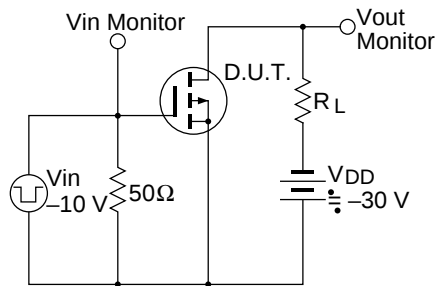
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

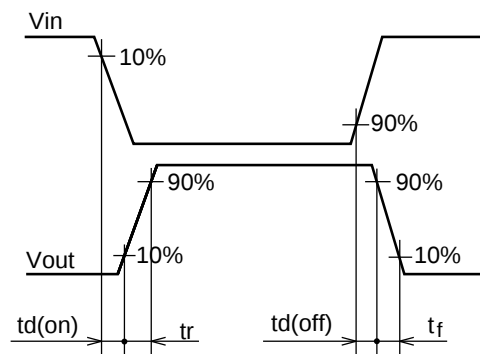




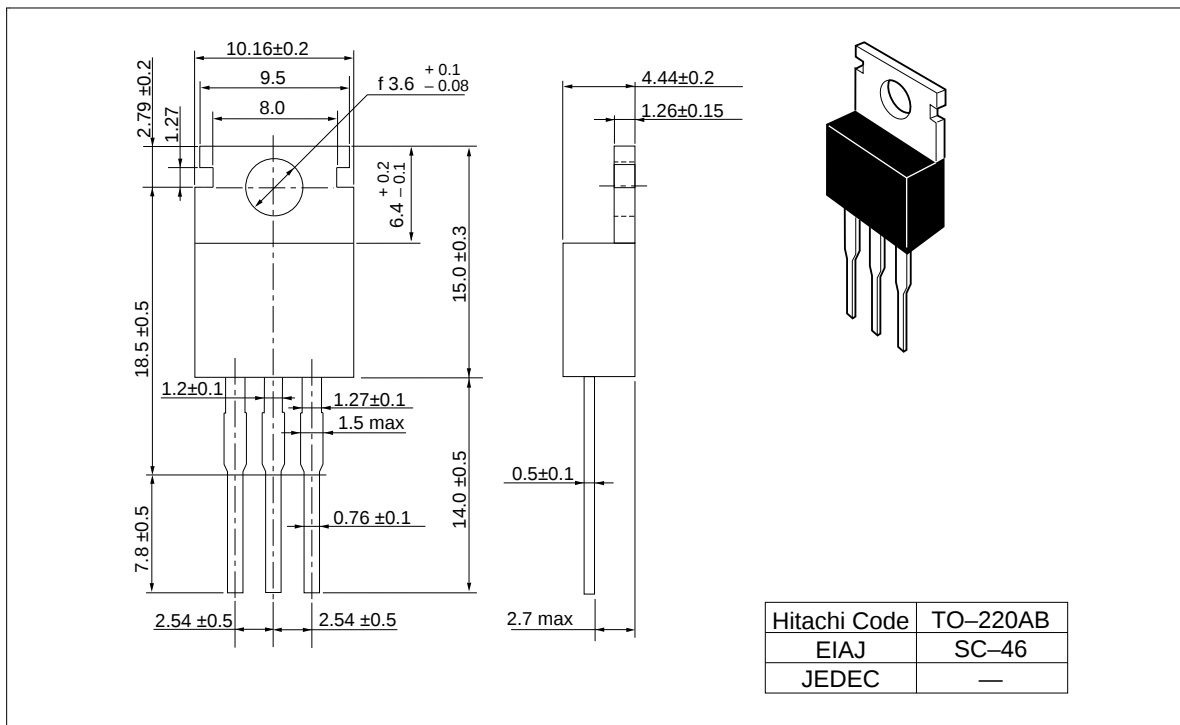
Switching Time Test Circuit



Waveform



Package Dimensions (Unit: mm)



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