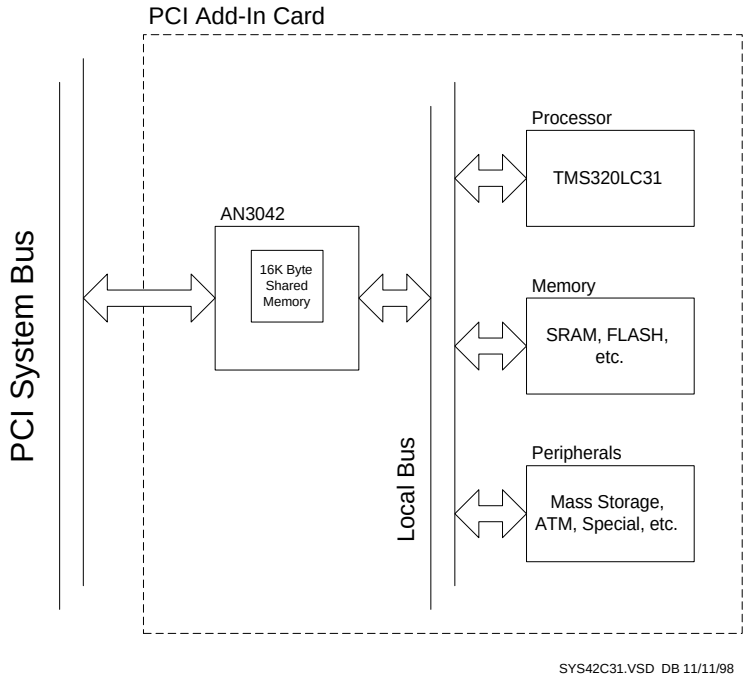
Overview

The AN3042Q interfaces directly to the TI TMS320LC31 Digital Signal Processor. The interface described in this application note connects a 32-bit, 40 MHz TMS320LC31 to the AN3042Q.

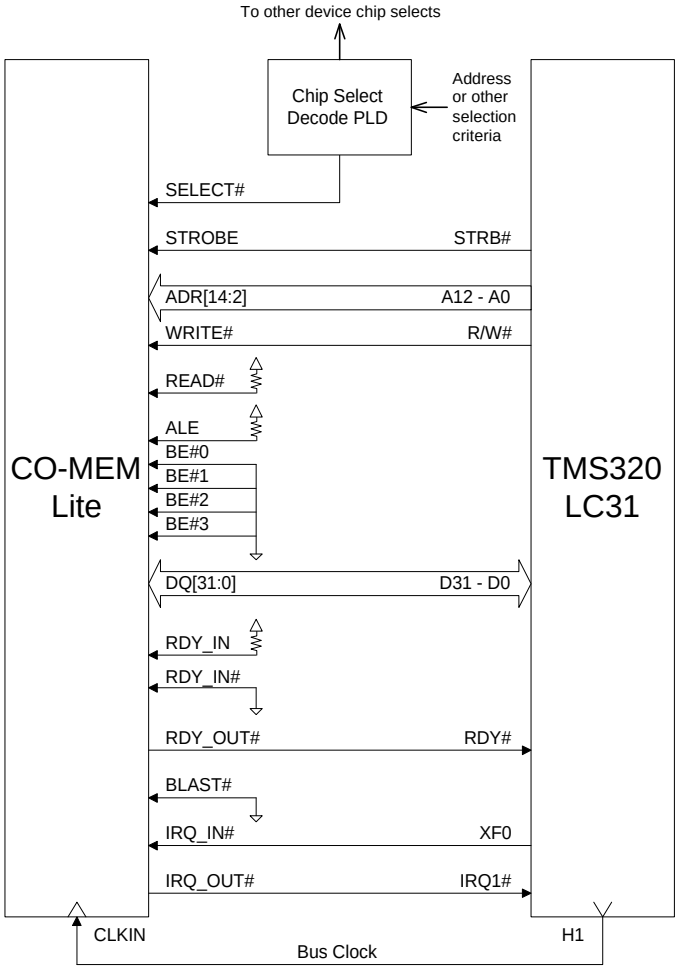
System Block Diagram

The AN3042Q connects the primary bus of a TMS320LC31 to the PCI system bus.



Wiring Diagram

Wiring the AN3042Q to the TMS320LC31 is simple. A programmable logic device (PLD) is used to generate the chip select for the AN3042Q. This PLD may contain chip select decoding for other devices in the TMS320LC31 system. The interrupt connections in the diagram are not required for the bus interface; they are only included by illustrative purposes.



AN3042Q Configuration Programming

The AN3042Q Local Bus Configuration register must be programmed to support the TMS320LC31 external bus architecture. This may be loaded either at power-up from a PROM via the I2C interface or from the PCI system host. The value for the register is:

LBUSCFG = 0x0A91

Timing

This section includes timing diagrams for the processor bus interface between the TMS320LC31 and the AN3042Q. The interface is based on a 40 MHz TMS320LC31 component.

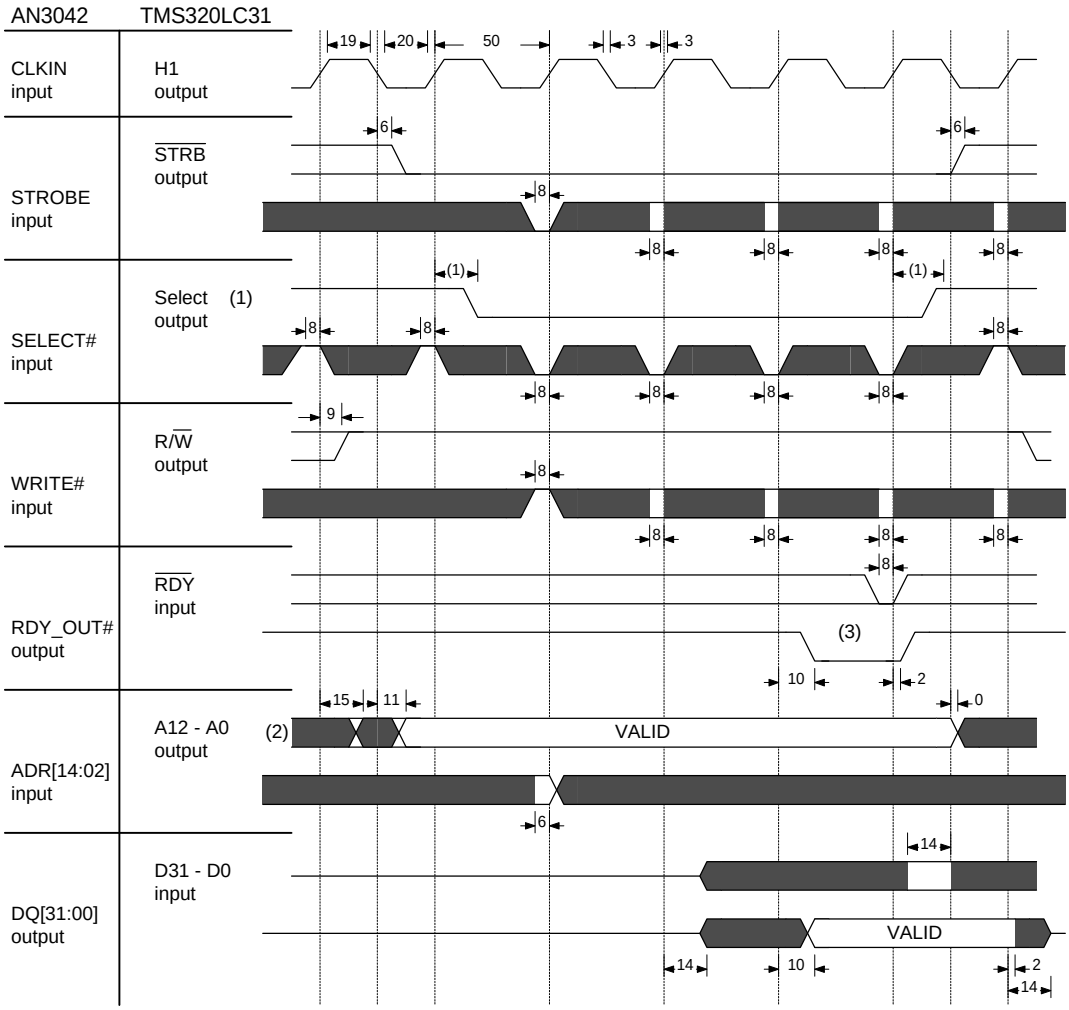
In this application note, the chip select to the AN3042Q is generated by circuits other than the TMS320LC31. For example, a 7.5 nsec programmable logic device (PLD) could be used to decode the processor's address lines to generate a select to the AN3042Q. The decoded signal should be clocked on the rising edge of the H1 clock before presentation to the AN3042Q SELECT# input. Chip selects for other devices in the TMS320LC31 system could be generated by this PLD.

In order to support back-to-back operations, the SELECT# input to the AN3042Q must deactivate for at least one cycle after the RDY_OUT# output is asserted. This function can be performed by the PLD. If back-to-back cycles are not to occur and a faster decoding is desired, one choice is to use the most significant address bit of the TMS320LC31 as a chip select. This would speed the access by one cycle.

Explanation and key to reading timing diagrams --

- Timing data are taken from the TMS320LC31 and AN3042Q specifications; see References.
- Timing numbers are in nanoseconds and worst case commercial environment.
- Clock pulse widths and clock cycle time are minimum values.
- All input hold times are 0 nsec. minimum; if relevant, minimum data hold times for outputs are shown.
- Where relevant, maximum data valid output timing is shown to support setup calculations.
- Where relevant, minimum data input setup timing is shown to support setup calculations.

The following is the timing diagram for TMS320LC31 read access to the AN3042Q.



NOTES --

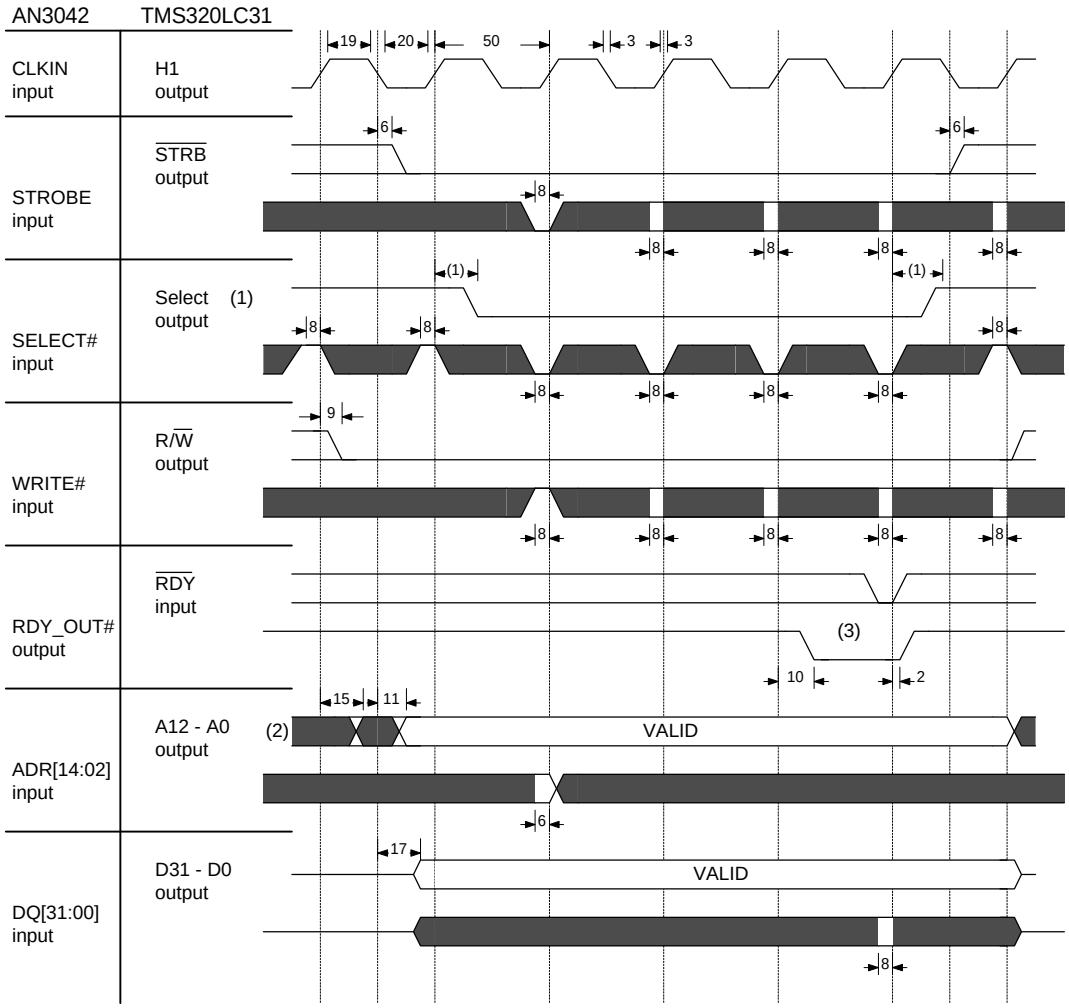
(1) The chip select to the AN3042 is application dependent. It may come from several sources. In this timing diagram, it is assumed to be clocked from an address decode. A faster method is discussed in the text.

(2) The address change leading into current cycle may occur on a rising or falling edge. If the immediately prior cycle was a write access, the TMS320LC31 address will change on the clock's rising edge. If the immediately prior cycle was a read access, the TMS320LC31 address will change on the clock's falling edge.

(3) Wait states occur when the AN3042Q delays assertion of RDY_OUT# to later cycles. Zero wait states are illustrated here.

C31RD.VSD
11/20/98

The following is the timing diagram for TMS320LC31 write access to the AN3042Q.



NOTES --

(1) The chip select to the AN3042 is application dependent. It may come from several sources. In this timing diagram, it is assumed to be clocked from an address decode. A faster method is discussed in the text.

(2) The address change leading into current cycle may occur on a rising or falling edge. If the immediately prior cycle was a write access, the TMS320LC31 address will change on the clock's rising edge. If the immediately prior cycle was a read access, the TMS320LC31 address will change on the clock's falling edge.

(3) Wait states occur when the AN3042Q delays assertion of RDY_OUT# to later cycles. Zero wait states are illustrated here.

C31WT.VSD 11/24/98

From the two diagrams, timing margin for a TMS320LC31 to AN3042 bus interconnect can be extracted. The timing shown is worst case commercial environment. Loading beyond the specification, signal line lengths, and other environmental constraints beyond commercial worst case can use this margin and still comply to specification. Some timings will have margin spanning more than one cycle. This is because in some cycles the signal is not used but the output signal remains valid across cycles. Timing margin is listed here in terms of input setup times.

Read and Write Access to the AN3042

AN3042 STROBE input setup, first cycle	56 nsec	
AN3042 STROBE input setup, last cycle	6 nsec	
AN3042 SELECT# input setup	34 nsec	(assumes an 8 nsec PLD)
AN3042 WRITE# input setup, first cycle	83 nsec	
TMS320LC31 RDY# input setup	32 nsec	
AN3042 ADR[14:02] input setup	53 nsec	

Data Bus for Read Access to the AN3042	
TMS320LC31 D31-D0 input setup	45 nsec
Data Bus for Write Access to the AN3042	
AN3042 DQ[31:00] input setup	195 nsec

Performance

Throughput between the TMS320LC31 and the shared memory of the AN3042Q is 16MB/sec. Throughput can be increased to 20MB/sec if an address line is used directly for the chip select; see the Timing section for more discussion. Access to the AN3042Q Operation Registers or FIFO may incur wait states.

AN3042Q mastered DMA bursting from the AN3042Q shared memory to system host memory has been measured to be approximately 120MB/sec on an unloaded PCI bus. Anchor Chips Incorporated has an application note concerning PCI bursting that can provide more insight into AN3042Q performance on a loaded PCI bus. It includes ways to tune your system to maximize PCI throughput.

References

Specifications used as input to this application note are listed below.

CO-MEM Lite, AN3042Q Integrated Circuit Technical Reference Manual, Version 1.1, October 19, 1998, Anchor Chips Incorporated.

TMS320C3x User's Guide, revision L, July 1997, Literature Number SPRU031E, Texas Instruments Incorporated.

TMS320C31, TMS320LC31 Digital Signal Processors, Revised July 1997, Literature Number SPRS035A, Texas Instruments Incorporated.

Additional component literature may be downloaded from web sites at Anchor Chips Incorporated and Texas Instruments Incorporated. The two main sites are listed below.

Anchor Chips PCI Developer's Home	http://www.anchorchips.com/pcidev/
TI Digital Signal Processing Solutions - Literature	http://www.ti.com/sc/docs/dsps/literatu.htm

The PCI 2.1 specification may be purchased from the PCI Special Interest Group (SIG) or other sources. The web site for the PCI SIG is:

PCI SIG Home Page	http://www.pcisig.com/

Some related Anchor Chips Incorporated application notes are listed below.

How to Do DMA
PCI Bus Mastering for System Performance