

FEATURES

1000 MHz Toggle Rate

Driver/Comparator/Active Load and Dynamic Clamp
Included

Inhibit Mode Function

100-Lead LQFP Package with Built-In Heat Sink

Driver

48 Ω Output Resistance

800 ps Tr/Tf for a 3 V Step

Comparator

1.1 ns Propagation Delay at 3 V

Load

± 40 mA Voltage Programmable Current Range

50 ns Settling Time to 15 mV

APPLICATIONS

Automatic Test Equipment

Semiconductor Test Systems

Board Test Systems

Instrumentation and Characterization Equipment

PRODUCT DESCRIPTION

The AD53522 is a complete, high-speed, single-chip solution that performs the pin electronics functions of driver, comparator, and active load (DCL) for ATE applications. In addition, the driver contains a dynamic clamp function and the active load contains an integrated Schottky diode bridge.

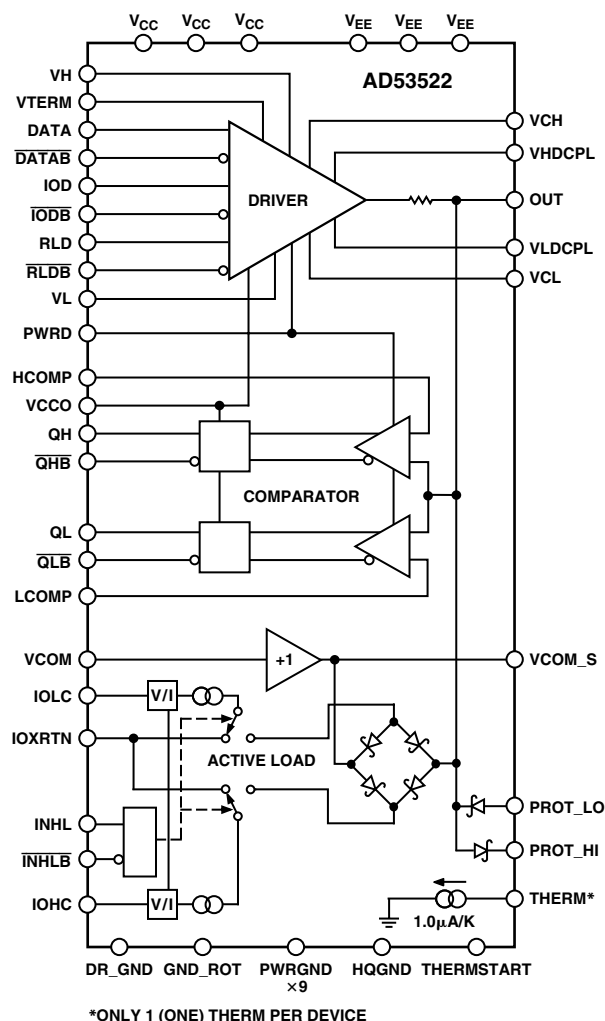
The driver is a proprietary design that features three active states: Data High Mode, Data Low Mode, and Term Mode, as well as an Inhibit State. In conjunction with the integrated dynamic clamp this facilitates the implementation of a high-speed active termination. The output voltage range is -0.5 V to $+6.5$ V to accommodate a wide variety of test devices.

The dual comparator, with an input range equal to the driver output range, features PECL compatible outputs. Signal tracking capability is in the range of 3 V/ns.

The active load can be set for up to 40 mA load current. I_{OH} , I_{OL} , and the buffered VCOM are independently adjustable. On-board Schottky diodes provide high-speed switching and low capacitance.

Also included on the chip is an on-board temperature sensor that gives an indication of the silicon surface temperature of the DCL. This information can be used to measure θ_{JC} and θ_{JA}

FUNCTIONAL BLOCK DIAGRAM



or flag an alarm if proper cooling is lost. Output from the sensor is a current sink that is proportional to absolute temperature. The gain is trimmed to a nominal value of $1.0 \mu\text{A}/\text{k}\Omega$. As an example, the output current can be sensed by using a $10 \text{ k}\Omega$ resistor connected from 10 V to the THERM (I_{OUT}) pin. A voltage drop across the resistor will be developed that equals: $10 \text{ k}\Omega \times 1 \mu\text{A}/\text{k}\Omega = 10 \mu\text{V}/\text{k}\Omega = 2.98 \text{ V}$ at room temperature.

REV. 0

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AD53522—SPECIFICATIONS

DRIVER¹ ($T_J = 85^\circ\text{C} \pm 5^\circ\text{C}$, $+V_S = +10.5\text{ V} \pm 1\%$, $-V_S = -4.5\text{ V} \pm 1\%$, $V_{CC0} = 3.3\text{ V}$ unless otherwise noted.)

Spec No.	Parameter	Conditions	Min	Typ ²	Max	Unit	Spec ³ Perf
DIFFERENTIAL INPUT CHARACTERISTICS (DATA to DATAb, IOD to IODb, RLD to RLDb)							
1	Voltage Range	Note: Inputs are from Same Logic Type Family	0		+3.3	V	N
2	Differential Voltage with LVPECL levels	Note: AC Tests Performed	± 400	± 600	± 1000	mV	P
3	Bias Current	$V_{IN} = 1.5\text{ V}, 2.5\text{ V}$	-250		+250	μA	P
REFERENCE INPUTS							
4	Bias Currents	Max Value Measured During Linearity Tests	-50		+50	μA	P
OUTPUT CHARACTERISTICS							
10	Logic High Range	Data = H, $V_H = -0.4\text{ V}$ to $+6.5\text{ V}$, $V_L = -0.5\text{ V}$ ($V_T = 0\text{ V}$, V_H meets test 20, 21, and 22 specs)	-0.4		+6.5	V	P
11	Logic Low Range	Data = L, $V_L = -0.5\text{ V}$ to $+6.4\text{ V}$, $V_H = 6.5\text{ V}$ ($V_T = 0\text{ V}$, V_L meets test 30, 31, and 32 specs)	-0.5		+6.4	V	P
12	Amplitude [$V_H - V_L$]	$V_L = -0.05\text{ V}$, $V_H = +0.05\text{ V}$, $V_T = 0\text{ V}$ and $V_L = -0.5\text{ V}$, $V_H = +6.5\text{ V}$, $V_T = 0\text{ V}$	+0.1		+7.0	V	P
ABSOLUTE ACCURACY							
20	V_H Offset	Data = H, $V_H = 0\text{ V}$, $V_L = -0.5\text{ V}$, $V_T = +3\text{ V}$	-50		+50	mV	P
21	V_H Gain Error	Data = H, $V_H = -0.4\text{ V}$ to $+6.5\text{ V}$, $V_L = -0.5\text{ V}$, $V_T = +3\text{ V}$	-0.3		+0.3	% of V_H	P
22	Linearity Error	Data = H, $V_H = -0.4\text{ V}$ to $+6.5\text{ V}$, $V_L = -0.5\text{ V}$, $V_T = +3\text{ V}$	-5		+5	mV	P
30	V_L Offset	Data = L, $V_L = 0\text{ V}$, $V_H = 6.5\text{ V}$, $V_T = 3\text{ V}$	-50		+50	mV	P
31	V_L Gain Error	Data = L, $V_L = -0.5\text{ V}$ to $+6.4\text{ V}$, $V_H = +6.5\text{ V}$, $V_T = +3\text{ V}$	-0.3		+0.3	% of V_L	P
32	Linearity Error	Data = L, $V_L = -0.5\text{ V}$ to $+6.4\text{ V}$, $V_H = +6.5\text{ V}$, $V_T = +3\text{ V}$	-5		+5	mV	P
33	Offset Temperature Coefficient	$V_L = 0\text{ V}$, $V_H = 5\text{ V}$, $V_T = 0\text{ V}$		0.5		mV/ $^\circ\text{C}$	N
OUTPUT RESISTANCE							
40	$V_H = -0.3\text{ V}$	$V_L = -0.5\text{ V}$, $V_T = 0\text{ V}$, $I_{OUT} = +1, +30\text{ mA}$	+46		+50	Ω	N
41	$V_H = +6.5\text{ V}$	$V_L = -0.5\text{ V}$, $V_T = 0\text{ V}$, $I_{OUT} = -1, -30\text{ mA}$	+46		+50	Ω	P
42	$V_L = -0.5\text{ V}$	$V_H = +6.5\text{ V}$, $V_T = 0\text{ V}$, $I_{OUT} = +1, +30\text{ mA}$	+46		+50	Ω	P
43	$V_L = +6.4\text{ V}$	$V_H = +6.5\text{ V}$, $V_T = 0\text{ V}$, $I_{OUT} = -1, -30\text{ mA}$	+46		+50	Ω	N
44	$V_H = +2.5\text{ V}$	$V_L = 0\text{ V}$, $V_T = 0\text{ V}$, $I_{OUT} = -30\text{ mA}$ (Trim Point)		+47.5		Ω	P
50	Dynamic Current Limit	$C_{byp} = 39\text{ nF}$, $V_H = +6.5\text{ V}$, $V_L = -0.5\text{ V}$, $V_T = 0\text{ V}$	+100			mA	N
51	Static Current Limit	Output to -0.5 V , $V_H = +6.5\text{ V}$, $V_L = -0.5\text{ V}$, $V_T = 0\text{ V}$, DATA = H	-120		-60	mA	P
52	Static Current Limit	Output to $+6.5\text{ V}$, $V_H = +6.5\text{ V}$, $V_L = -0.5\text{ V}$, $V_T = 0\text{ V}$, DATA = L	+60		+120	mA	P

Spec No.	Parameter	Conditions	Min	Typ ²	Max	Unit	Spec ³ Perf
60	VTERM Voltage Range	TERM MODE, VTERM = -0.3 V to +6.3 V, VL = 0 V, VH = +3 V (VTERM meets test 61, 62, and 63 specs)	-0.3		+6.3	V	P
61	VTERM Offset	TERM MODE, VTERM = 0 V, VL = 0 V, VH = 3 V	-50		+50	mV	P
62	VTERM Gain Error	TERM MODE, VTERM = -0.3 V to +6.3 V, VL = 0 V, VH = +3 V	-0.3		+0.3	% of V _{SET}	P
63	VTERM Linearity Error	TERM MODE, VTERM = -0.3 V to +6.3 V, VL = 0 V, VH = +3 V	-5		+5	mV	P
64	Offset Temperature Coefficient	VTERM = 0 V, VL = 0 V, VH = 3 V		+0.5		mV/°C	N
70	Output Resistance DC	I _{OUT} = +30 mA, -1 mA, VTERM = -0.3 V, VH = 3 V, VL = 0 V I _{OUT} = -30 mA, +1 mA, VTERM = +6.3 V, VH = 3 V, VL = 0 V I _{OUT} = ±30 mA, ±1 mA, VTERM = +2.5 V, VH = 3 V, VL = 0 V	+46		+50	Ω	N
72	PSRR, Drive, or TERM Mode	+V _S , -V _S ± 1%		17.8		mV/V	N
73	Static Current Limit	Output to -0.3 V, VTERM = +6.3 V	-120		-60	mA	P
74	Static Current Limit	Output to +6.3 V, VTERM = -0.3 V	+60		+120	mA	P
DYNAMIC PERFORMANCE, DRIVE (VH and VL)							
80	Propagation Delay Time	Measured at 50%, VL = 0 V, VH = 3 V, into 500 Ω	1.25	1.4	1.55	ns	P
81	Propagation Delay T.C.	Measured at 50%, VL = 0 V, VH = 3 V, into 500 Ω		2		ps/°C	N
82	Delay Matching, Edge-to-Edge	Measured at 50%, VL = 0 V, VH = 3 V, into 500 Ω			200	ps	P
RISE AND FALL TIMES							
90	200 mV Swing	Measured 20%–80%, VL = -0.1 V, VH = +0.1 V, into 50 Ω		0.25		ns	N
91	1 V Swing	Measured 20%–80%, VL = 0 V, VH = 1 V, into 50 Ω		0.3		ns	N
92	3 V Swing	Measured 10%–90%, VL = 0 V, VH = 3 V, into 50 Ω		0.8		ns	N
93	3 V Swing	Measured 10%–90%, VL = 0 V, VH = 3 V, into 500 Ω		0.8		ns	N
93A	3 V Swing	Measured 20%–80%, VL = 0 V, VH = 3 V, into 500 Ω	0.450	0.560	0.670	ns	P
94	5 V Swing	Measured 10%–90%, VL = 0 V, VH = 5 V, into 500 Ω		1.2	1.5	ns	N
RISE AND FALL TIME TEMPERATURE COEFFICIENT							
100	1 V Swing	(per test 91)		±2		ps/°C	N
101	3 V Swing	(per test 92)		±2		ps/°C	N
102	5 V Swing	(per test 94)		±4		ps/°C	N
110	Overshoot and Preshoot	VL, VH = -0.1 V, +0.1 V, Driver Terminated into 50 Ω	0 – 50		0 + 50	% of Step + mV	N
		VL, VH = 0.0 V, 3 V, Driver Terminated into 50 Ω	-6.0 – 50		+6.0 + 50	% of Step + mV	N
SETTING TIME							
120	to 15 mV	VL = 0 V, VH = 0.5 V, Driver Terminated into 50 Ω		50		ns	N
121	to 4 mV	VL = 0 V, VH = 0.5 V		10		μs	N

SPECIFICATIONS (continued)

DRIVER¹ (continued)

Spec No.	Parameter	Conditions	Min	Typ ²	Max	Unit	Spec ³ Perf
130	Delay Change vs. Pulsewidth 30 ns/90 ns, DC = 25%	VL/VH = 0/3, PW = 2.5 ns/7.5 ns,		25	75	ps	N
131	Delay Change vs. Duty Cycle	VL = 0 V, VH = 3 V, Duty Cycle (DC) 5 to 95%, T = 40 ns		25		ps	N
140	MINIMUM WIDTH PULSE 1 V Swing	Meas 50% point width V _{OUT} AC Swing = 0.9 × V _{OUT} DC		0.6		ns	N
141	3 V Swing	Swing Terminated, 50 Ω Load on Transmission Line		1.5		ns	N
142	Toggle Rate	VH = 1 V, VL = 0 V, Terminated to 50 Ω, V _{OUT} > 300 mV p-p		1000		MHz	N
DYNAMIC PERFORMANCE, INHIBIT							
150	Delay Time, Active to Inhibit	Measured at 50%, VH = 4 V, VL = 0 V, VTT = 2		1.7	2.0	ns	P
151	Delay Time, Inhibit to Active	Measured at 50%, VH = 4 V, VL = 0 V, VTT = 2		1.7	2.2	ns	P
152	Delay Time Matching, Inhibit to Active	Measured at 50%, VH = 4 V, VL = 0 V, VTT = 2		150	250	ps	P
153	Delay Time Matching, Active to Inhibit	Measured at 50%, VH = 4 V, VL = 0 V, VTT = 2		150	250	ps	P
160	I/O Spike	VH = 0 V, VL = 0 V			200	mV p-p	N
170	Rise, Fall Time, Active to Inhibit	VL = 0 V, VTT = 2 (20%/80% of 1 V Output)			1.2	ns	N
171	Rise, Fall Time, Inhibit to Active	VH = 4 V, VL = 0 V, VTT = 2 (20%/80% of 1 V Output)			0.6	ns	N
DYNAMIC PERFORMANCE, VTERM							
180	Delay Time, VH to VTERM	Measured at 50%, VL = VH = 2 V, VTERM = 0 V, VTT = 0 V		1.5	1.9	ns	P
181	Delay Time, VL to VTERM	Measured at 50%, VL = VH = 0 V, VTERM = 2 V, VTT = 0 V		1.6	1.9	ns	P
182	Delay Time, VTERM to VH	Measured at 50%, VL = VH = 2 V, VTERM = 0 V, VTT = 0 V		1.6	2.0	ns	P
183	Delay Time, VTERM to VL	Measured at 50%, VL = VH = 0 V, VTERM = 2 V, VTT = 0 V		1.6	2.0	ns	P
190	Overshoot and Preshoot	VH/VL, VTERM = (0 V, 2 V), (0 V, 6 V)	-6.0 + 50		+6.0 + 50	% of Step + mV	N
191A	VTERM Rise Time, VL to VT, Normal Mode	VL, VH = 0 V, VTERM = 2 V, 20%–80%			1.0	ns	N
191B	VTERM Rise Time, VT to VH, Normal Mode	VL, VH = 2 V, VTERM = 0 V, 20%–80%			0.6	ns	N
192A	VTERM Fall Time, VT to VL, Normal Mode	VL, VH = 0 V, VTERM = 2 V, 20%–80%			0.6	ns	N
192B	VTERM Fall Time, VH to VT, Normal Mode	VL, VH = 2V, VTERM = 0 V, 20%–80%			1.0	ns	N

COMPARATOR¹

Spec No.	Parameter	Conditions	Min	Typ ²	Max	Unit	Spec ³ Perf
DC INPUT CHARACTERISTICS							
200	VCCO Range		2.0		4.5		N
201	Offset Voltage (V_{OS})	Common-Mode Voltage = 0 V	-25		+25	mV	P
202	Offset Voltage Drift	Common-Mode Voltage = 0 V		50		$\mu\text{V}/^{\circ}\text{C}$	N
203	HCOMP, LCOMP	Over Linearity Range	-50		+50	μA	P
BIAS CURRENTS							
206	Voltage Range (V_{CM})		-0.5		+6.5	V	P
207	Differential Voltage (V_{DIFF})				+7	V	P
208	Gain Error	$V_{IN} = -0.5 \text{ V to } +6.5 \text{ V}$	-0.25		0.0	%FSR	N
209	Linearity Error	$V_{IN} = -0.5 \text{ V to } +6.5 \text{ V}$	-2		+2	mV	N
210	Extended Range Operation	HCOMP, LCOMP = -1, output toggle V_{OUT} from -0.9 V to -1.1 V	-1.0			V	P
DIGITAL OUTPUTS							
220	Logic "1" Voltage QX	Q or Qb, 150 Ω to GND, 150 Ω from Q to Qb	$V_{CCO} - 1.05$		$V_{CCO} - 0.85$	V	P
221	Logic "0" Voltage QXb	Q or Qb, 150 Ω to GND, 150 Ω from Q to Qb	$V_{CCO} - 2.2$		$V_{CCO} - 1.5$	V	P
222	Logic Differential, QX-QXb	Q or Qb, 150 Ω to GND, 150 Ω from Q to Qb	0.65	0.9	1.15	V	P
225	Slew Rate	Q or Qb (20 – 80% of output, 150 Ω from Q to Qb)		380		ps	N
CHANNEL COMPARATOR SWITCHING PERFORMANCE							
PROPAGATION DELAY							
240	Input to Output	$V_{IN} = 3 \text{ V p-p, } 2 \text{ V/ns}$	0.7		1.1	ns	P
241	Propagation Delay Temp. Co.	$V_{IN} = 3 \text{ V p-p, } 2 \text{ V/ns}$		1.0		ps/ $^{\circ}\text{C}$	N
PROP DELAY CHANGE WITH RESPECT TO:							
250	Slew Rate: 1, 2, 3 V/ns	$V_{IN} = 0 \text{ V to } 3 \text{ V}$		120		ps	N
260	Amplitude: 500 mV, 1.0 V, 3.0 V	$V_{IN} = 1.0 \text{ V/ns}$		100		ps	N
270	Equivalent Input Rise Time	$V_{IN} = 0 \text{ V to } 2 \text{ V, } < 80 \text{ ps, } 20\% - 80\% \text{ Rise Time}$		275		ps	N
DRIVER IN VTERM = 0 V							
280	Pulsewidth Linearity	$V_{IN} = 0 \text{ V to } 3 \text{ V, } 2 \text{ V/ns, PW} = 3, 4, 5, 10 \text{ ns, Driver Hi-Z mode}$			50	ps	N
281	Settling Time	Settling to $\pm 8 \text{ mV, } V_{IN} = 0 \text{ V to } 3 \text{ V, Driver Hi-Z mode}$		25		ns	N
282	Hysteresis			6		mV	N
290	Comparator Propagation Delay Matching, HCOMP to LCOMP	$V_{IN} = 0 \text{ V to } 3 \text{ V, } 2 \text{ V/ns}$			125	ps	P
INPUT CHARACTERISTICS							
300	INHL, INHLb Input Voltage	See Driver Spec No. 1 $V_{IOH} = 1 \text{ V, } V_{IOL} = 1 \text{ V, } V_{COM} = 2 \text{ V, } V_{DUT} = 0 \text{ V}$	0		3.3	V	P
301	INHL, INHLb Bias Current	INHL, INHLb = 0 V, 3.3 V, AC Tests 0.2 V and 0.8 V	-250		+250	μA	P
302	V_{IOH} Current Program Range, IOH = 0 mA to -40 mA	$V_{DUT} = 0.8 \text{ V, } 6.5 \text{ V}$	0		4.0	V	P

AD53522

SPECIFICATIONS (continued)

ACTIVE LOAD¹

Spec No.	Parameter	Conditions	Min	Typ ²	Max	Unit	Spec ³ Perf
303	BIAS CURRENT VIOL Current Program Range, IOL = 0 mA to 40 mA	VIOH = 0 V, 4 V VDUT = -0.5 V, +5.2 V	0		4.0	V	P
304	IOH, VIOL Input	VIOL = 0 V, 4 V and	-300	+300		μA	P
305	IOXRTN Range	IOL = +40 mA, IOH = -40 mA, VDUT = -0.5 V, +6.5 V		-0.5, +6.5		V	N
310	VDUT Range	IOL = +40 mA, IOH = -40 mA, VDUT - VCOM > 1.3 V	-0.5		+6.5	V	P
311	VDUT Range, IOH = 0 mA to -40 mA	VDUT - VCOM > 1.3 V	0.8		6.5	V	P
312	VDUT Range, IOL = 0 mA to +40 mA	VCOM - VDUT > 1.3 V	-0.5		+5.2	V	P
320	OUTPUT CHARACTERISTICS Accuracy Gain Error, Load Current, Normal Range Calculated at 1 mA and 40 mA points ²	IOL, IOH = 25 μA - 40 mA, VCOM = 0 V, VDUT = ±2 V and IOL = 25 μA to 40 mA, VCOM = +6.5 V, VDUT = +5.2 V and IOH = 25 μA to 40 mA, VCOM = -0.5 V, VDUT = +0.8 V	-0.35		+0.35	%I _{SET}	P
321	Load Offset	Calculated from Intercept of 1 mA and 40 mA Points	-300		+300	μA	P
322	Load Nonlinearity	IOL, IOH from 25 μA to 40 mA	-80		+80	μA	P
323	Output Current Temperature	Measured at IOH, IOL = 200 μA		< ±3		μA/°C	N
324	COEFFICIENT IOH Extended Range	Driver Inhibited, IOH = 1 mA, Change in IOH from VTT = 0 V to VTT = -1.0 V	2			%	P
330	VCOM BUFFER VCOM Buffer Offset Error	IOL, IOH = 40 mA, VCOM = 0 V	-50		+50	mV	P
331	VCOM Buffer Bias Current	VCOM = 0 V	-20		+20	μA	P
332	VCOM Buffer Gain Error	IOL, IOH = 40 mA, VCOM = -0.5 V to +6.5 V	-4		+4	%	P
333	VCOM Buffer Linearity Error	IOL, IOH = 40 mA, VCOMI = -0.5 V to +6.5 V	-10		+10	mV	P
340	DYNAMIC PERFORMANCE Propagation Delay ± I _{MAX} to INHIBIT	VTT = +2 V, VCOM = +4/0 V, IOL = +20 mA, IOH = -20 mA	1.0	1.3	2.0	ns	P
341	INHIBIT to ± I _{MAX}	VTT = +2 V, VCOM = +4/0 V, IOL = +20 mA, IOH = -20 mA	1.2	1.8	2.4	ns	P
342	Propagation Delay Matching	Matching = (Test 340 Value) - (Test 341 Value)	-1.0		+1.0	ns	P
350	I/O Spike	VCOM = 0 V, IOL = +20 mA, IOH = -20 mA		250		mV	N
360	Settling Time to 15 mV	IOL = +20 mA, IOH = -20mA, 50 Ω Load, to ±15 mV		50		ns	N
361	Settling Time to 4 mV	IOL = +20 mA, IOH = -20 mA, 50 Ω Load, to ±4 mV		10		μs	N

DYNAMIC CLAMP PART¹

Spec No.	Parameter	Conditions	Min	Typ ²	Max	Unit	Spec ³ Perf
400	Input Voltage VCH	Over range spec #401, 402 $I_{TEST} = 1 \text{ mA}$	2		7.5	V	P
401	Input Voltage VCL		-1.5		+4	V	P
402	Input Bias Current VCH/VCL		-250		+250	μA	P
410	VCH, VCL Offset Error		-250		+250	mV	P
411	VCH, VCL Gain Error		0.96		1.01	V/V	P
420	Static Current Capability	11 mA to 21 mA	50		75	mA	N
430	Incremental Resistance		45	48	52	Ω	P
440	VCHP, VCLP Protection		0.52		0.64	V	P
441	Diodes Vf @ 500 μ Protection Diodes Max Current	For information only			2	mA	N
TOTAL FUNCTION POWER DOWN							
500	PWRD Input Voltage	PWRD trip point $1.4 \text{ V} \pm 0.15 \text{ V}$ $V_{IOH} = 0 \text{ V}$, $V_{IOL} = 0 \text{ V}$	0		5	V	P
501	PWRD Bias Current		-250		+250	μA	P
503	Power-Down Supply Reduction		35		60	%	P
504	Power-Down Output Leakage Current		-20		+20	nA	P
505	Power-Down Output Leakage Current	$V_{IOH} = 0 \text{ V}$, $V_{IOL} = 0 \text{ V}$, $V_{OUT} = -0.5 \text{ V}$ to $+5.5 \text{ V}$	-500		+500	nA	P
600	Output Leakage Current, $V_{OUT} = -0.5 \text{ V}$ to $+6.5 \text{ V}$	$V_{IOH} = 0 \text{ V}$, $V_{IOL} = 0 \text{ V}$, $V_{OUT} = 5.5 \text{ V}$ to 6.5 V	-1		+1	μA	P
601	Output Leakage Current, $V_{OUT} = 0 \text{ V}$ to 5 V		-500		+500	nA	P
602	Output Leakage Current, $V_{OUT} = -1 \text{ V}$		-5		+5	μA	P
605	Output Capacitance			9.2		pF	N
606	Output Capacitance Term	Driver and Load INHIBITED Driver VTERM = 0 V, Load INHIBITED		2.5		pF	N
POWER SUPPLIES							
610	Total Supply Range	Driver = Inhibit, I_{LOAD} program = 40 mA, Load = Active		15		V	N
620	Positive Supply, VCC			+10.5		V	N
630	Negative Supply, VEE			-4.5		V	N
640	Positive Supply Current, VCC			465	570	mA	P
650	Negative Supply Current, VEE	Driver = Inhibit, I_{LOAD} program = 40 mA, Load = Active		475	600	mA	P
651	Comparator Supply Current Overhead, VCCO	Driver = Inhibit, I_{LOAD} program = 40 mA, Load = Active (I_{VCCO} - (comparator logic output currents))			45	mA	P
660	Total Power Dissipation	Driver = Inhibit, I_{LOAD} program = 40 mA, Load = Active		7.2	7.9	W	P
661	Total Power Dissipation	Driver = Inhibit, I_{LOAD} program = 0 mA		5.2	5.9	W	P
700	Temperature Sensor Gain Factor	$R_{LOAD} = 10 \text{ k}\Omega$, $V_{SOURCE} = 10.5 \text{ V}$		1		$\mu\text{A/K}$	N

NOTES

¹All temperature coefficients are measured at $T_J = 75^\circ\text{C}$ – 95°C . In test figures, voltmeter loading is 1 M Ω or greater, scope probe loading is 100 k Ω in parallel with 0.6 pF.

²Typical Values are not tested or guaranteed. Nominal values are generated from design or simulation analyses and/or limited bench evaluations and are not tested or guaranteed.

³Spec Perf: N = Nominal, O = Operating Condition, T = Typical, P = Production, Max Min

⁴VTERM Linearity over the following condition: $V_L - 6 \text{ V} < V_{TERM} < V_H + 6 \text{ V}$

⁵All ac input values are referred to the source end of transmission line input.

⁶All ac tests are performed with Driver in VTERM mode except where noted.

⁷Rise time is calculated $\text{SQRT}((\text{comp out rt})^2 - (\text{comp in rt})^2)$

Specifications are subject to change without notice.

AD53522

ABSOLUTE MAXIMUM RATINGS¹

POWER SUPPLY VOLTAGE

V _{CC} to GND	11.3 V
V _{EE} to GND	−7 V
V _{CC} to V _{EE}	18 V
V _{CCO} to GND	5.5 V
PWRGND, DRGND, GND_ROT, or HQGND	±0.4 V

OUTPUTS

V _{OUT} Short Circuit Duration	Indefinite ²
V _{OUT} , Inhibit Mode	+8.5 V, −2 V
V _{OUT} , Inhibit Mode	VL − 5.5 V < V _{OUT} < VH + 5.5 V
VHDCPL	Do Not Connect Except for Cap to V _{CC}
VLDCPL	Do Not Connect Except for Cap to V _{EE}
QH, QHb, QL, QLb Maximum I _{OUT} :	

Continuous	50 mA
Surge	100 mA
THERM	11 V, 0 V
Driver output capacitance, maximum	10 pF

INPUTS

DATA, DATAb, IOD, IODb, RLD, RLDB	(V _{CCO} + 1.5 V, V _{CCO} − 4.5 V)
INHL, INHLb, CMPD	−0.4 V to +5.5 V
PWRD	−0.4 V to +4.5 V
DATA to DATAb, IOD to IODb, RLD to RLDB	±3 V

INHL to INHLb	±6 V
VH, VL, VTERM to GND (R _{series} < 500 Ω)	+7.5 V, −1.1 V
VH to VL	+8 V, −3.5 V
(VH − VTERM) and (VTERM − VL)	±8 V
Reflection Clamps High/Low	+8.5 V, −2 V
Protection Clamp Breakdown Voltage	12 V
Protection Clamps Current	±5 mA
V _{OUT} to HCOMP or LCOMP	±7.8 V

ENVIRONMENTAL

Operating Temperature (Junction)	175°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec) ³	260°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Output short circuit protection is guaranteed as long as proper heat sinking is employed to ensure compliance with the operating temperature limits.

³To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C ±5°C (75°F ±10°F) with relative humidity not to exceed 65%.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD53522JSQ	0°C to 70°C	100-Lead LQFP-EDQUAD with Integral Heat Slug	SQ-100

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53522 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table I. Driver Truth Table

DATA	DATAb	IOD	IODb	RLD	RLDb	Output State
0	1	1	0	X	X	VL
1	0	1	0	X	X	VH
X	X	0	1	0	1	INH and CLAMP
X	X	0	1	1	0	VTERM

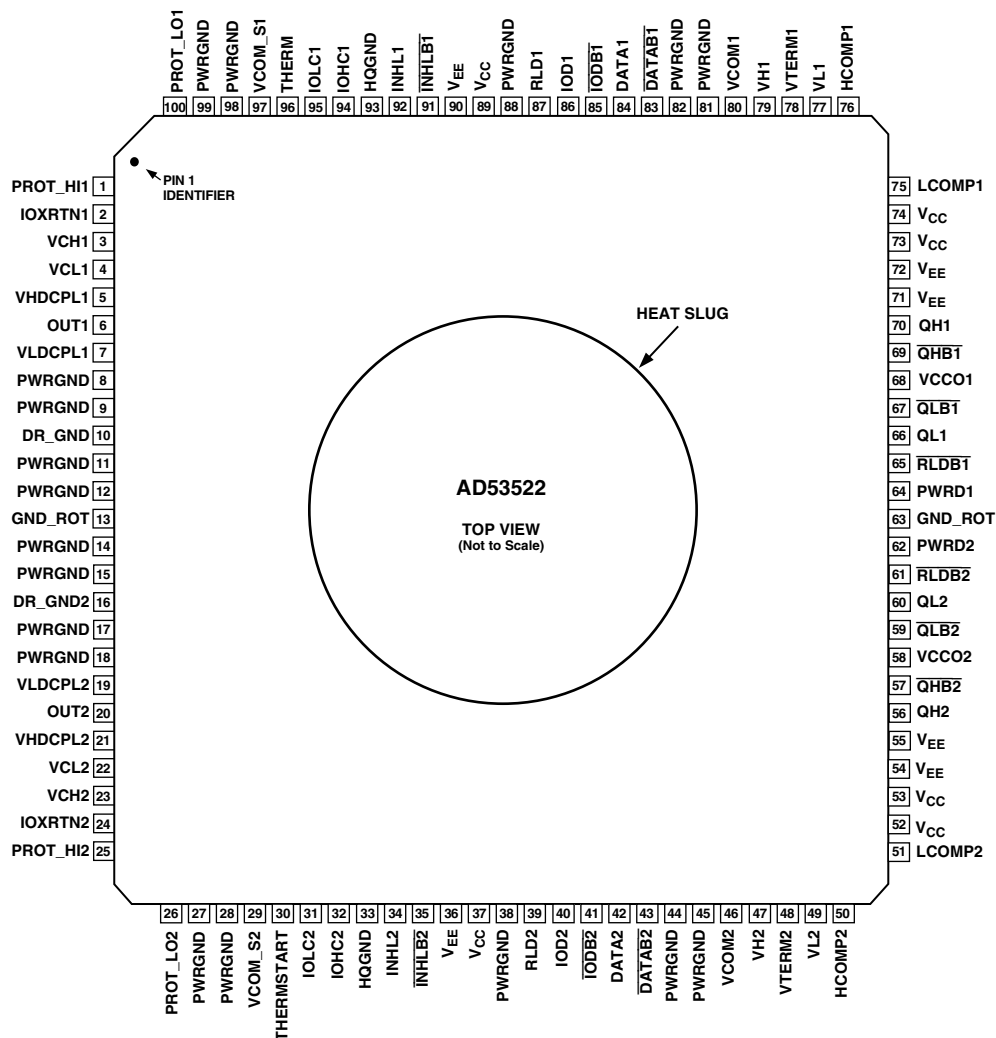
Table II. Comparator Truth Table

V _{OUT}		Output States			
		QH	QHb	QL	QLb
> HCOMP	> LCOMP	1	0	1	0
> HCOMP	< LCOMP	1	0	0	1
< HCOMP	> LCOMP	0	1	1	0
< HCOMP	< LCOMP	0	1	0	1

Table III. Active Load Truth Table

VDUT	INHL	INHLb	Output States (including diode bridge)		
			IOH	IOL	I(V _{OUT})
<VCOM	0	1	V(IOHC) × +10 mA	V(IOLC) × −10 mA	IOL
>VCOM	0	1	V(IOHC) × +10 mA	V(IOLC) × −10 mA	IOH
X	1	0	0	0	0

PIN CONFIGURATION



NOTE
DIE IS MOUNTED TO THE BACK OF THE HEAT SLUG.
THE PACKAGE IS MOUNTED TO THE BOARD, HEAT SLUG UP.

PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Description
1	PROT_HI1	Channel 1, output voltage sensing diode
2	IOXRTN1	Current return path for the active load for channel 1. Typically connected to a power ground.
3	VCH1	Analog input voltage that sets the reflection clamp high level of channel 1
4	VCL1	Analog input voltage that sets the reflection clamp low level of channel 1
5	VHDCPL1	Internal supply decoupling for the driver output stage of channel 1. This pin needs to be connected to V_{CC} through a 39 nF (minimum) capacitor.
6	OUT1	Input/output for the driver, window comparator, reflection clamp, and the active load of channel 1
7	VLDCPL1	Internal supply decoupling for the driver output stage of channel 1. This pin needs to be connected to V_{EE} through a 39 nF (minimum) capacitor.
8	PWRGND	Power ground
9	PWRGND	Power ground
10	DR_GND	Analog ground

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Pin Number	Mnemonic	Description
11	PWRGND	Power ground
12	PWRGND	Power ground
13	GND_ROT	Analog ground
14	PWRGND	Power ground
15	PWRGND	Power ground
16	DR_GND	Analog ground
17	PWRGND	Power ground
18	PWRGND	Power ground
19	VLDCPL2	Internal supply decoupling for the driver output stage of channel 2. This pin needs to be connected to V_{EE} through a 39 nF (minimum) capacitor.
20	OUT2	Input/output for the driver, window comparator, reflection clamp, and the active load of channel 2
21	VHDCPL2	Internal supply decoupling for the driver output stage of channel 2. This pin needs to be connected to V_{CC} through a 39 nF (minimum) capacitor.
22	VCL2	Analog input voltage that sets the reflection clamp high level of channel 2
23	VCH2	Analog input voltage that sets the reflection clamp high level of channel 2
24	IOXRTN2	Current return path for the active load for channel 2. Typically connected to a power ground.
25	PROT_HI2	Channel 2, output voltage sensing diode
26	PROT_LO2	Channel 2, output voltage sensing diode
27	PWRGND	Power ground
28	PWRGND	Power ground
29	VCOM_S2	Analog output voltage that represents a buffered VCOM1 input
30	THERMSTART	Temperature sensor startup pin. Normally not connected
31	IOLC2	Analog input voltage that programs the channel 2 active load source current
32	IOHC2	Analog input voltage that programs the channel 2 active load sink current
33	HQGND	Clean analog ground for the active load for channel 2
34	INHL2	One of two complementary inputs that control the inhibit mode for the active load bridge of channel 2
35	$\overline{\text{INHLB2}}$	One of two complementary inputs that control the inhibit mode for the active load bridge of channel 2
36	V_{EE}	Negative supply terminal
37	V_{CC}	Positive supply terminal
38	PWRGND	Power ground
39	RLD2	One of two complementary inputs that control, in conjunction with IOD2 and IODB2, the operating mode of the channel 2 driver. Refer to the Driver Truth Table for specific conditions.
40	IOD2	One of two complementary inputs that control, in conjunction with RLD2 and RLDB2, the operating mode of the channel 2 driver. Refer to the Driver Truth Table for specific conditions.
41	$\overline{\text{IODB2}}$	One of two complementary inputs that control, in conjunction with RLD2 and RLDB2, the operating mode of the channel 2 driver. Refer to the Driver Truth Table for specific conditions.
42	DATA2	One of two complementary input that determine the high and low state of the channel 2 driver. Driver output is high for $\text{DATA2} > \text{ATAB2}$. Refer to the Driver Truth Table for specific conditions.
43	$\overline{\text{ATAB2}}$	One of two complementary input that determine the high and low state of the channel 2 driver. Driver output is high for $\text{DATA2} > \text{ATAB2}$. Refer to the Driver Truth Table for specific conditions.
44	PWRGND	Power ground
45	PWRGND	Power ground
46	VCOM2	Analog input voltage that establishes the commutation voltage for the active load diode bridge for channel 2
47	VH2	Analog input voltage that sets the Logic 1 level of the driver output limit for channel 2. Determines the driver output for $\text{DATA2} > \text{ATAB}$

Pin Number	Mnemonic	Description
48	VTERM2	Analog input voltage that sets the termination voltage level of the channel 2 driver when in VTERM mode
49	VL2	Analog input voltage that sets the Logic 0 level of the driver output limit for channel 2. Determines the driver output for $DATA2 > DATA2$.
50	HCOMP2	Analog input voltage that sets the Logic 1 compare reference for the window comparator of channel 2
51	LCOMP2	Analog input voltage that sets the Logic 0 compare reference for the window comparator of channel 2
52	V _{CC}	Positive supply terminal
53	V _{CC}	Positive supply terminal
54	V _{EE}	Negative supply terminal
55	V _{EE}	Negative supply terminal
56	QH2	One of two complementary outputs for the Logic 1 window comparator of channel 1
57	$\overline{QHB2}$	One of two complementary outputs for the Logic 1 window comparator of channel 1
58	VCCO2	Input supply voltage for QH2, QHB2, QL2, and QLB2 signals and reference voltage for DATA2, DATAB2, IOD2, IODB2, RLD2, and RLDB2
59	$\overline{QLB2}$	One of two complementary outputs for the Logic 0 window comparator of channel 2
60	QL2	One of two complementary outputs for the Logic 0 window comparator of channel 2
61	$\overline{RLDB2}$	One of two complementary inputs that control, in conjunction with IOD2 and IODB2, the operating mode of the channel 2 driver. Refer to the Driver Truth Table for specific conditions.
62	PWRD2	Power-down control for channel 2
63	GND_ROT	Analog ground
64	PWRD1	Power-down control for channel 1
65	$\overline{RLDB1}$	One of two complementary inputs that control, in conjunction with IOD1 and IODB1, the operating mode of the channel 1 driver
66	QL1	One of two complementary outputs for the Logic 0 window comparator of channel 1
67	$\overline{QLB1}$	One of two complementary outputs for the Logic 0 window comparator of channel 1
68	VCCO1	Input supply voltage for QH1, QHB1, QL1, and QLB1 signals and reference voltage for DATA1, DATAB1, IOD1, IODB1, RLD1, and RLDB1
69	$\overline{QHB1}$	One of two complementary outputs for the Logic 1 window comparator of channel 1
70	QH1	One of two complementary outputs for the Logic 1 window comparator of channel 1
71	V _{EE}	Negative supply terminal
72	V _{EE}	Negative supply terminal
73	V _{CC}	Positive supply terminal
74	V _{CC}	Positive supply terminal
75	LCOMP1	Analog input voltage that sets the Logic 0 compare reference for the window comparator of channel 1
76	HCOMP1	Analog input voltage that sets the Logic 1 compare reference for the window comparator of channel 1
77	VL1	Analog input voltage that sets the Logic 0 level of the driver output limit for channel 1. Determines the driver output for $DATA1 > DATA1$.
78	VTERM1	Analog input voltage that sets the termination voltage level of the channel 1 driver when in VTERM mode
79	VH1	Analog input voltage that sets the Logic 1 level of the driver output limit for channel 1. Determines the driver output for $DATA1 > DATA1$.
80	VCOM1	Analog input voltage that establishes the commutation voltage for the active load diode bridge for channel 1
81	PWRGND	Power ground
82	PWRGND	Power ground
83	$\overline{DATAB1}$	One of two complementary inputs that determine the high and low state of the channel 1 driver. Driver output is high for $DATA1 > DATAB1$. Refer to the Driver Truth Table for specific conditions.
84	DATA1	One of two complementary inputs that determine the high and low state of the channel 1 driver. Driver output is high for $DATA1 > DATAB1$. Refer to the Driver Truth Table for specific conditions.

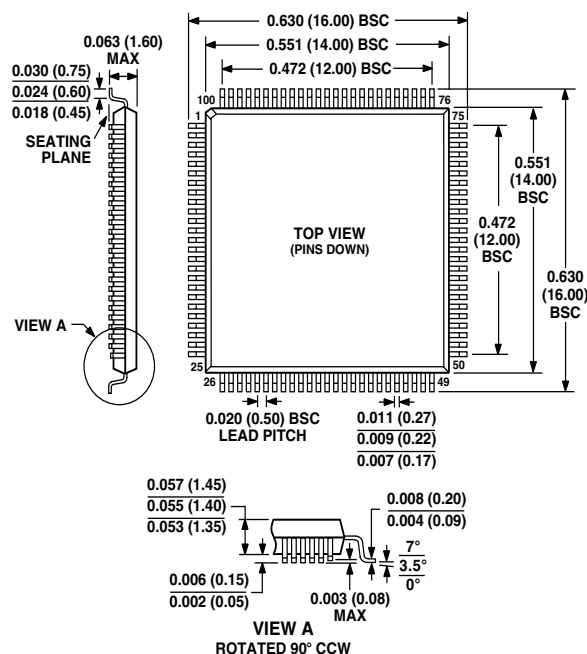
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Pin Number	Mnemonic	Description
85	$\overline{\text{IODB1}}$	One of two complementary inputs that control, in conjunction with RLD1 and RLDB1, the operating mode of the channel 1 driver. Refer to the Driver Truth Table for specific conditions.
86	IOD1	One of two complementary inputs that control, in conjunction with RLD1 and RLDB1, the operating mode of the channel 1 driver. Refer to the Driver Truth Table for specific conditions.
87	RLD1	One of two complementary inputs that controls, in conjunction with IOD1 and IODB1, the operating mode of the channel 1 driver. Refer to the Driver Truth Table for specific conditions.
88	PWRGND	Power ground
89	V _{CC}	Positive supply terminal
90	V _{EE}	Negative supply terminal
91	$\overline{\text{INHLB1}}$	One of two complementary inputs that control the inhibit mode for the active load bridge of channel 1
92	INHL1	One of two complementary inputs that control the inhibit mode for the active load bridge of channel 1
93	HQGND	Clean analog ground for the active load for channel 1
94	IOHC1	Analog input voltage that programs the channel 1 active load sink current
95	IOLC1	Analog input voltage that programs the channel 1 active load source current
96	THERM	Temperature sensor output pin. A resistor (10 KW) should be connected between THERM and V _{CC} . The approximate die temperature can be determined by measuring the current through the resistor. The typical scale factor is 1 μ A/K.
97	VCOM_S1	Analog output voltage that represents a buffered VCOM1 input
98	PWRGND	Power ground
99	PWRGND	Power ground
100	PROT_LO1	Channel 1 output voltage sensing diode

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

100-Lead LQFP-EDQUAD (SQ-100)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS.