Features

- **Dual ADC with 8-bit Resolution**
- **500 Msps Sampling Rate per Channel, 1 Gsps in Interlaced Mode**
- **Single or 1:2 Demultiplexed Output**
- **LVDS Output Format (100Ω)**
- **500 mVpp Analog Input (Differential Only)**
- **Differential or Single-ended 50Ω PECL/LVDS Compatible Clock Inputs**
- **Power Supply: 3.3V (Analog), 3.3V (Digital), 2.25V (Output)**
- **LQFP144 Package**
- **Temperature Range:**
  - **0°C < TA < 70°C (Commercial Grade)**
  - **-40°C < TA < 85°C (Industrial Grade)**
- **3-wire Serial Interface**
  - **16-bit Data, 3-bit Address**
  - **1:2 or 1:1 Output Demultiplexer Ratio Selection**
  - **Full or Partial Standby Mode**
  - **Analog Gain (±1.5 dB) Digital Control**
  - **Input Clock Selection**
  - **Analog Input Switch Selection**
  - **Binary or Gray Logical Outputs**
  - **Synchronous Data Ready Reset**
  - **Data Ready Delay Adjustable on Both Channels**
  - **Interlacing Functions:**
    - **Offset and Gain (Channel to Channel) Calibration**
    - **Digital Fine SDA (Fine Sampling Delay Adjust) on One Channel**
  - **Internal Static or Dynamic Built-In Test (BIT)**

Performance

- Low Power Consumption: 0.7W Per Channel
- Power Consumption in Standby Mode: 120 mW
- 1 GHz Full Power Input Bandwidth (-3 dB)
- SNR = 43 dB Typ (7.0 ENOB), THD = -53 dBc, SFDR = -55 dBc at Fs = 500 Msps Fin = 250 MHz
- 2-tone IMD3: -54 dBc (249 MHz, 5251 MHz) at 500 Msps
- DNL = 0.25 LSB, INL = 0.5 LSB
- Channel to Channel Input Offset Error: 0.5 LSB Max (After Calibration)
- Gain Matching (Channel to Channel): 0.5 LSB Max (After Calibration)
- Low Bit Error Rate (10^{-15}) at 500 Msps

Application

- Instrumentation
- Satellite Receivers
- Direct RF Down Conversion
- WLAN

Dual 8-bit 500 Msps ADC

AT84AD004 Smart ADC

Summary

5390AS–BDC–05/04

Description

The AT84AD004 is a monolithic dual 8-bit analog-to-digital converter, offering low 1.4W power consumption and excellent digitizing accuracy. It integrates dual on-chip track/holds that provide an enhanced dynamic performance with a sampling rate of up to 500 Msps and an input frequency bandwidth of 1 GHz. The dual concept, the integrated demultiplexer and the easy interleaving mode make this device user-friendly for all dual channel applications, such as direct RF conversion or data acquisition. The *smart* function of the 3-wire serial interface eliminates the need for external components, which are usually necessary for gain and offset tuning and setting of other parameters, leading to space and power reductions as well as system flexibility.

Functional Description

The AT84AD004 is a dual 8-bit 500 Msps ADC based on advanced high-speed BiCMOS technology.

Each ADC includes a front-end analog multiplexer followed by a Sample and Hold (S/H), and an 8-bit flash-like architecture core analog-to-digital converter. The output data is followed by a switchable 1:1 or 1:2 demultiplexer and LVDS output buffers (100Ω).

Two over-range bits are provided for the adjustment of the external gain control on each channel.

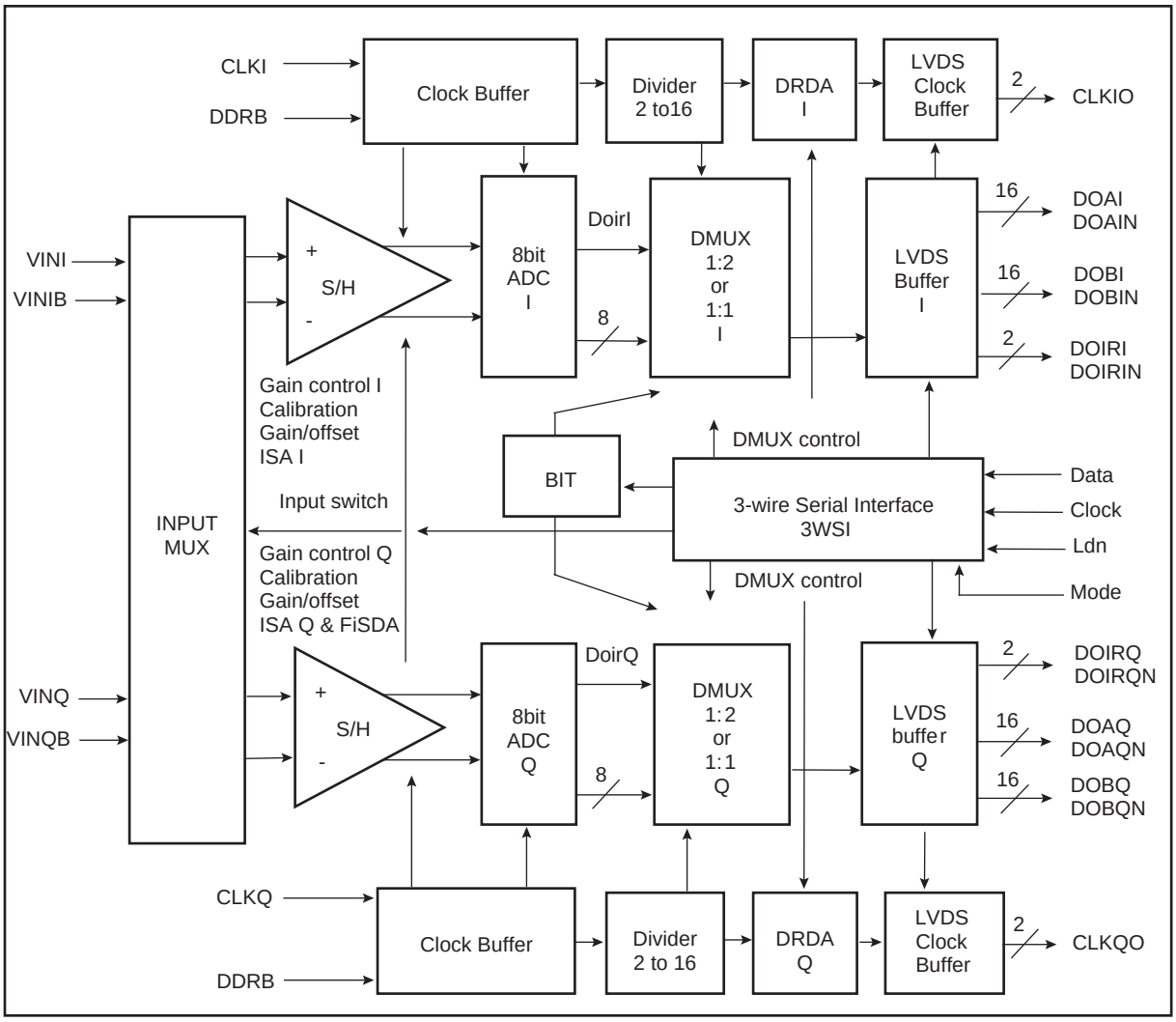
A 3-wire serial interface (3-bit address and 16-bit data) is included to provide several adjustments:

- Analog input range adjustment (±1.5 dB) with 8-bit data control using a 3-wire bus interface (steps of 0.18 dB)
- Analog input switch: both ADCs can convert the same analog input signal I or Q
- Gray or binary encoder output. Output format: DMUX 1:1 or 1:2 with control of the output frequency on the data ready output signal
- Partial or full standby on channel I or channel Q
- Clock selection:
  - Two independent clocks: CLKI and CLKQ
  - One master clock (CLKI) with the same phase for channel I and channel Q
  - One master clock but with two phases (CLKI for channel I and CLKIB for channel Q)
- ISA: Internal Settling Adjustment on channel I and channel Q
- FiSDA: Fine Sampling Delay Adjustment on channel Q
- Adjustable Data Ready Output Delay on both channels
- Test mode: decimation mode (by 16), Built-In Test

A calibration phase is provided to set the two DC offsets of channel I and channel Q close to code 127.5 and calibrate the two gains to achieve a maximum difference of 0.5 LSB. The offset and gain error can also be set externally via the 3-wire serial interface.

The AD84AD004 operates in fully differential mode from the analog inputs up to the digital outputs. The AD84AD004 features a full-power input bandwidth of 1 GHz.

Figure 1. Simplified Block Diagram



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

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