HB56TW432D Series, HB56TW433D Series

4,194,304-word × 32-bit High Density Dynamic RAM Module

HITACHI

ADE-203-732A (Z)
Rev.1.0
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Description

The HB56TW432D is a 4M × 32 dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 8 pieces of 16-Mbit DRAM (HM51W16400) sealed in TSOP package. The HB56TW433D is a 4M × 32 dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 8 pieces of 16-Mbit DRAM (HM51W17400) sealed in TSOP package. An outline of the HB56TW432D, HB56TW433D is 72-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56TW432D, HB56TW433D make high density mounting possible without surface mount technology. The HB56TW432D, HB56TW433D provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 72-pin Zig Zag Dual tabs socket type
  - — Outline: 59.69 mm (Length) × 25.40 mm (Height) × 3.80 mm (Thickness)
  - — Lead pitch: 1.27 mm
- Single 3.3 V (±0.3 V) supply
- High speed
  - — Access time: t_{RAC} = 50/60/70 ns (max)
    t_{CAC} = 13/15/18 ns (max)
- Low power dissipation
  - — Active mode: 2.59/2.30/2.02 W (max) (HB56TW432D Series)
    2.88/2.59/2.30 W (max) (HB56TW433D Series)
  - — Standby mode (TTL): 57.6 mW (max)
    (CMOS): 2.88 mW (max) (L-version)
- Fast page mode capability

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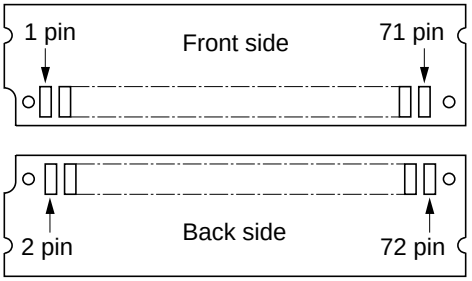
- Refresh period
  - 4096 refresh cycles: 64 ms (HB56TW432D Series)
    128 ms (L-version)
  - 2048 refresh cycles: 32 ms (HB56TW433D Series)
    128 ms (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
  - Self refresh (L-version)

Ordering Information

Type No.	Access time	Package	Contact pad
HB56TW432D-5	50 ns	72-pin small outline DIMM	Gold
HB56TW432D-6	60 ns		
HB56TW432D-7	70 ns		
HB56TW432D-5L	50 ns		
HB56TW432D-6L	60 ns		
HB56TW432D-7L	70 ns		
HB56TW433D-5	50 ns		
HB56TW433D-6	60 ns		
HB56TW433D-7	70 ns		
HB56TW433D-5L	50 ns		
HB56TW433D-6L	60 ns		
HB56TW433D-7L	70 ns		

Pin Arrangement



Pin Arrangement

Front side				Back side			
Pin No.	**Pin name**	**Pin No.**	**Pin name**	**Pin No.**	**Pin name**	**Pin No.**	**Pin name**
1	V_{SS}	37	DQ18	2	DQ0	38	DQ19
3	DQ1	39	V_{SS}	4	DQ2	40	$\overline{CE0}$
5	DQ3	41	$\overline{CE2}$	6	DQ4	42	$\overline{CE3}$
7	DQ5	43	$\overline{CE1}$	8	DQ6	44	$\overline{RE0}$
9	DQ7	45	NC	10	V_{CC}	46	NC
11	PD1	47	$\overline{WE}$	12	A0	48	NC
13	A1	49	DQ20	14	A2	50	DQ21
15	A3	51	DQ22	16	A4	52	DQ23
17	A5	53	DQ24	18	A6	54	DQ25
19	A10	55	NC	20	NC	56	DQ27
21	DQ9	57	DQ28	22	DQ10	58	DQ29
23	DQ11	59	DQ31	24	DQ12	60	DQ30
25	DQ13	61	V_{CC}	26	DQ14	62	DQ32
27	DQ15	63	DQ33	28	A7	64	DQ34
29	A11 (NC)*[1]	65	NC	30	V_{CC}	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	NC	69	PD5	34	$\overline{RE2}$	70	PD6
35	DQ16	71	PD7	36	NC	72	V_{SS}

Note: 1. A11: HB56TW432D, NC: HB56TW433D

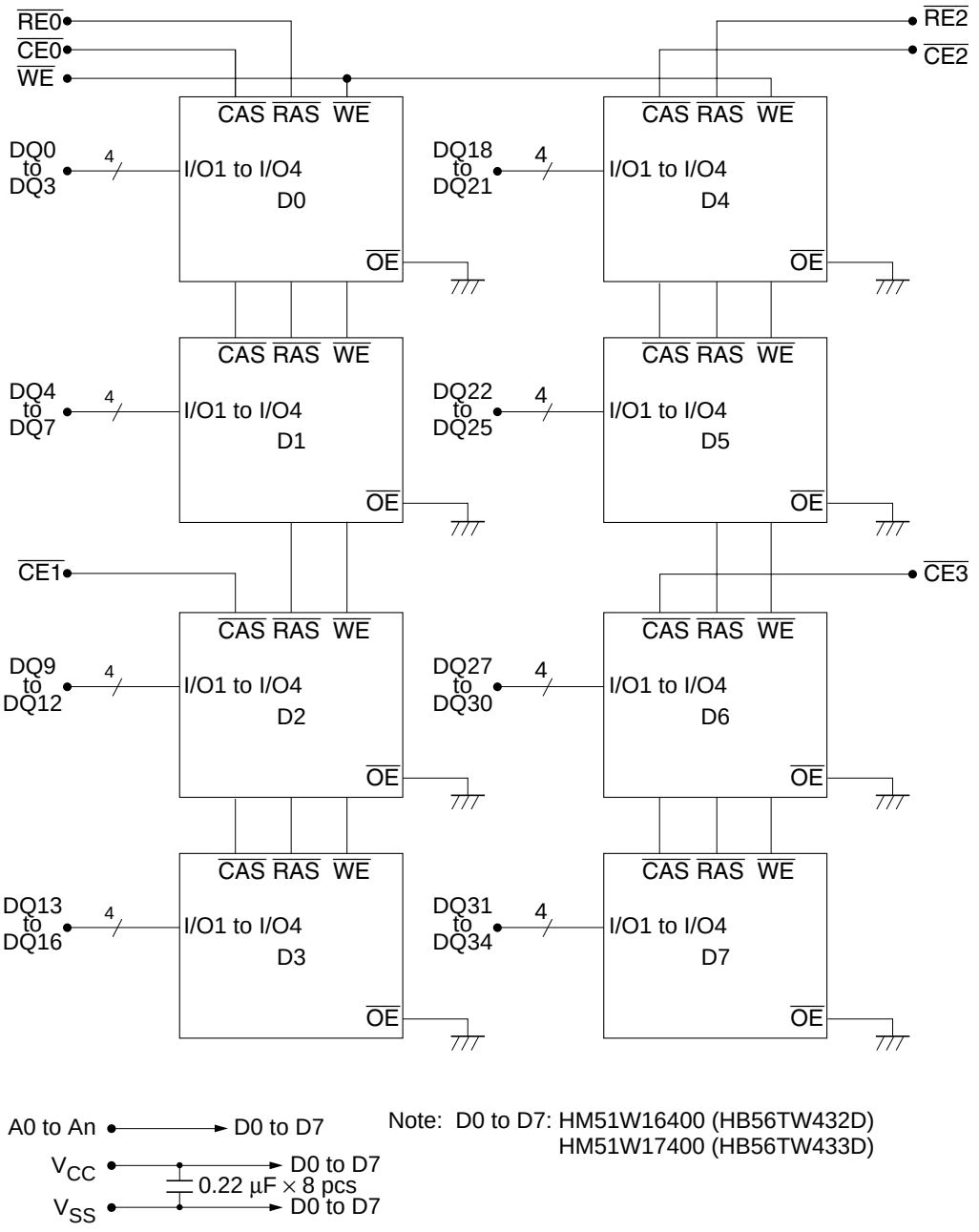
Pin Description

Pin name	Function
A0 to A11 (HB56TW432D)	Address inputs: — Row address: A0 to A11 — Column address: A0 to A9 — Refresh address: A0 to A11
A0 to A10 (HB56TW433D)	Address inputs: — Row address: A0 to A10 — Column address: A0 to A10 — Refresh address: A0 to A10
DQ0 to DQ7, DQ9 to DQ16, DQ18 to DQ25, DQ27 to DQ34	Data-in/Data-out
$\overline{RE0}$, $\overline{RE2}$	Row address strobe ($\overline{RAS}$)
$\overline{CE0}$ to $\overline{CE3}$	column address strobe ($\overline{CAS}$)
$\overline{WE}$	Read/Write enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD7	Presence detect
NC	No connection

Presence Detect Pin Arrangement

		Function		
Pin No.	**Pin name**	**50 ns**	**60 ns**	**70 ns**
11	PD1	NC	NC	NC
66	PD2	NC	NC	NC
67	PD3	V_{SS}	V_{SS}	V_{SS}
68	PD4	NC	NC	NC
69	PD5	V_{SS}	NC	V_{SS}
70	PD6	V_{SS}	NC	NC
71	PD7	NC	NC	NC
	PD7 (L-version)	V_{SS}	V_{SS}	V_{SS}

Block Diagram



Note: D0 to D7: HM51W16400 (HB56TW432D)
HM51W17400 (HB56TW433D)

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	8	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V) (HB56TW432D)

		50 ns		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	720	—	640	—	560	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	0.8	—	0.8	—	0.8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	720	—	640	—	560	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	720	—	640	—	560	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	640	—	560	—	480	mA	t_{PC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	2.4	—	2.4	—	2.4	mA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 31.3 µs t_{RAS} ≤ 0.3 µs	
Self refresh mode current (L-version)	I_{CC11}	—	1.6	—	1.6	—	1.6	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V Dout = High-Z	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V) (HB56TW433D)

		50 ns		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	800	—	720	—	640	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	0.8	—	0.8	—	0.8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	800	—	720	—	640	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	800	—	720	—	640	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	720	—	640	—	560	mA	t_{PC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	2.4	—	2.4	—	2.4	mA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 62.5 µs t_{RAS} ≤ 0.3 µs	
Self refresh mode current (L-version)	I_{CC11}	—	1.6	—	1.6	—	1.6	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V Dout = High-Z	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	68	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	76	pF	1
Input capacitance ($\overline{CAS}$)	C_{I3}	—	29	pF	1
Input capacitance ($\overline{RAS}$)	C_{I4}	—	43	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70˚C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) *[1], *[2], *[17]

Test Conditions

- Input rise and fall times: 5 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, and Refresh Cycles (Common parameters)

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	90	—	110	—	130	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10000	15	10000	18	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	10	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	37	20	45	20	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	15	—	18	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	50	—	60	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_{T}	3	50	3	50	3	50	ns	5
Refresh period (HB56TW432D: 4,096 cycles)	t_{REF}	—	64	—	64	—	64	ms	
Refresh period (HB56TW432D: 4,096 cycles) (L-version)	t_{REF}	—	128	—	128	—	128	ms	
Refresh period (HB56TW433D: 2,048 cycles)	t_{REF}	—	32	—	32	—	32	ms	
Refresh period (HB56TW433D: 2,048 cycles) (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	7, 8, 15
Access time from address	t_{AA}	—	25	—	30	—	35	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	25	—	30	—	35	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	11
$\overline{CAS}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	

Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	12
Write command hold time	t_{WCH}	8	—	10	—	15	—	ns	
Write command pulse width	t_{WP}	8	—	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	13
Data-in hold time	t_{DH}	8	—	10	—	15	—	ns	13

Refresh Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	8	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	5	—	ns	

Fast Page Mode Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode cycle time	t_{PC}	35	—	40	—	45	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	30	—	35	—	40	ns	7, 15
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	30	—	35	—	40	—	ns	

Self Refresh Mode (L-version)

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{RAS}$ pulse width (Self refresh)	t_{RASS}	100	—	100	—	100	—	µs	
$\overline{RAS}$ precharge time (Self refresh)	t_{RPS}	90	—	110	—	130	—	ns	
$\overline{CAS}$ hold time (Self refresh)	t_{CHS}	–50	—	–50	—	–50	—	ns	

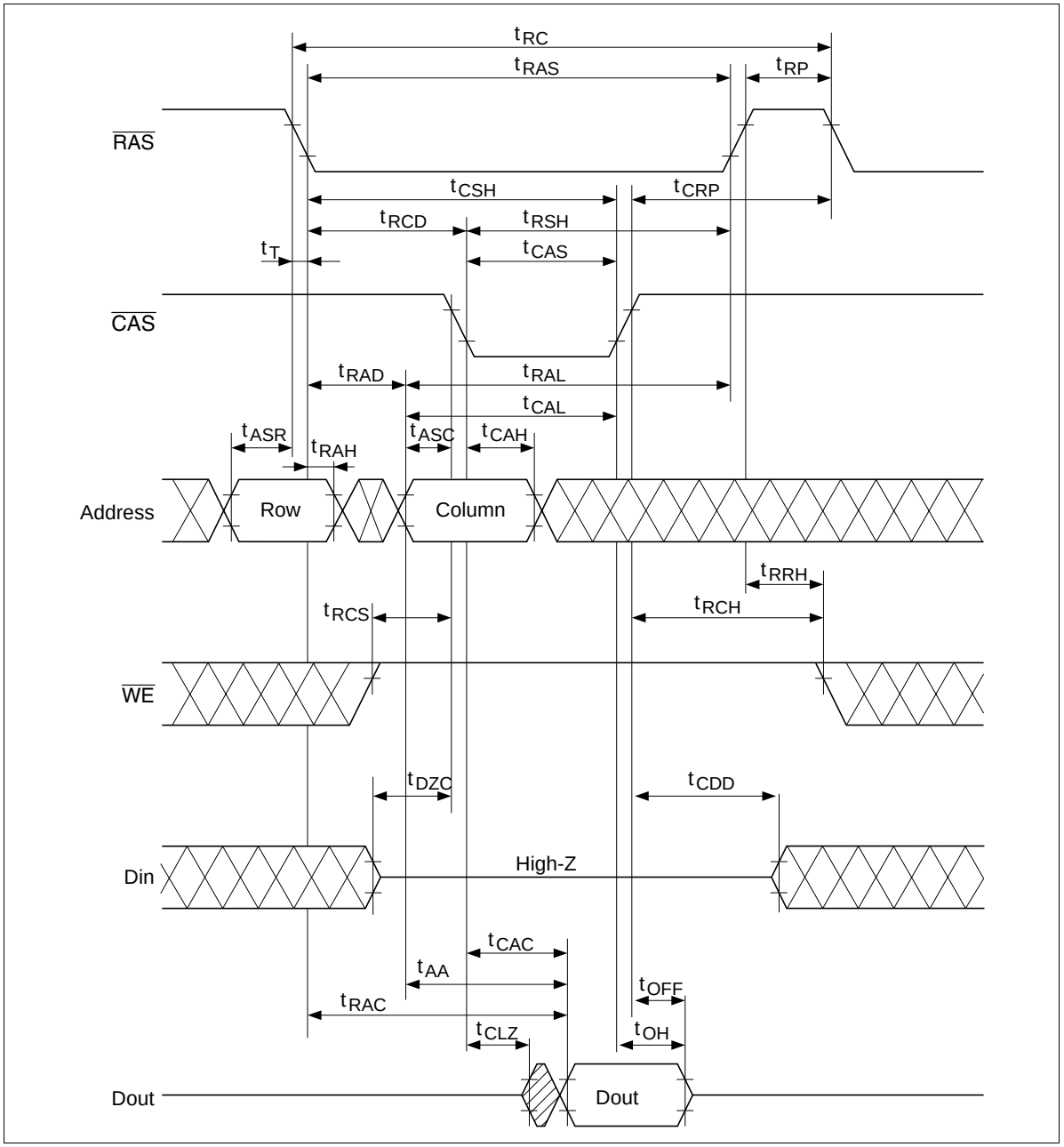
Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
11. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
12. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
13. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in Fast page mode cycles.
15. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
16. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
17. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
18. Please do not use t_{RASS} timing, 10 µs $\leq t_{RASS} \leq$ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq$ 100 µs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
19. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
20. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 2048 cycles (4096 cycles: HB56TW432D Series, 2048 cycles: HB56TW433D Series) of distributed CBR refresh with 15.6 µs interval should be executed within 64 or 32 ms (64 ms: HB56TW432D Series, 32 ms: HB56TW433D Series) immediately after exiting from and before entering into the self refresh mode.
21. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
22. XXX: H or L (H: V_{IH} (min) $\leq V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) $\leq V_{IN} \leq V_{IL}$ (max))

    ///////: Invalid Dout

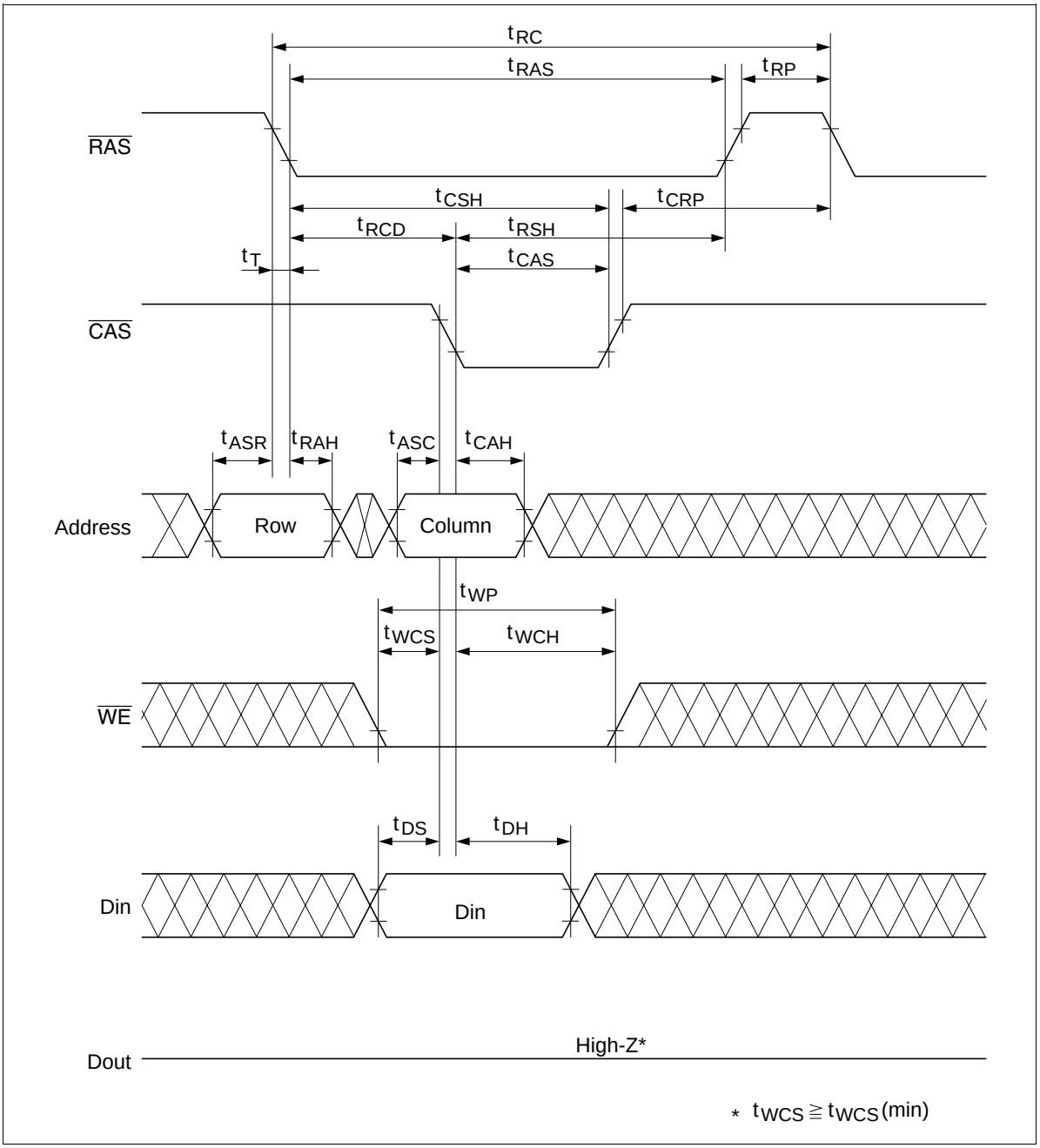
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[22]

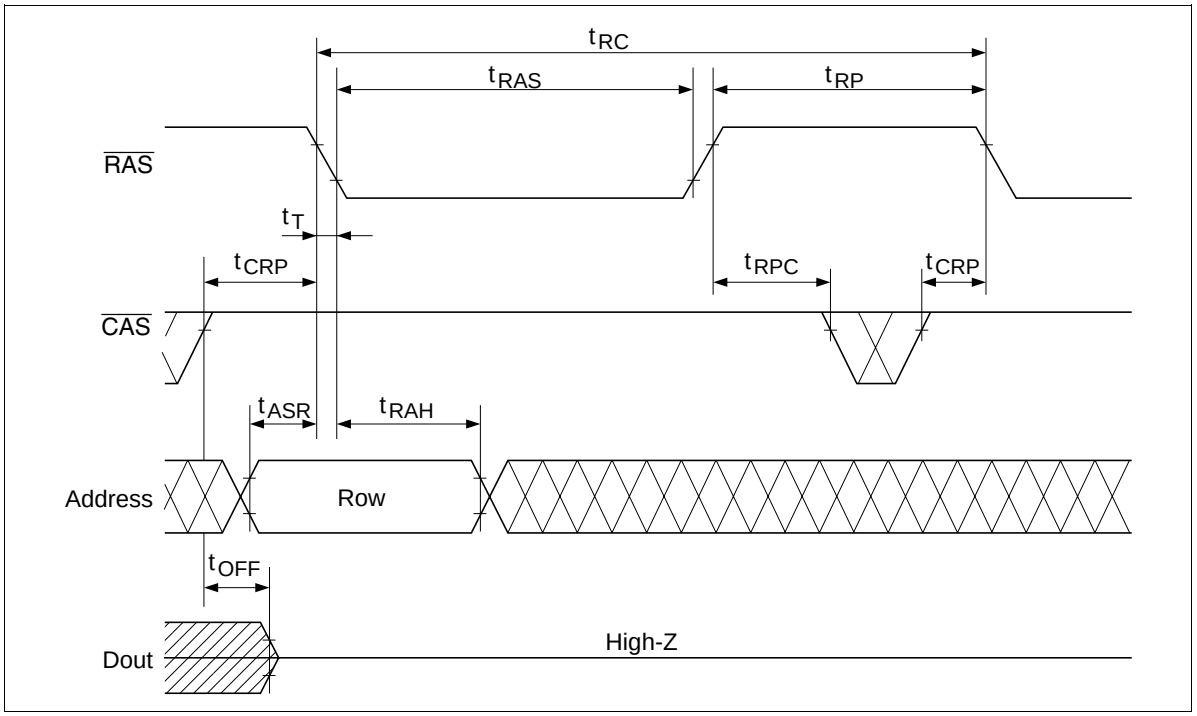
Read Cycle



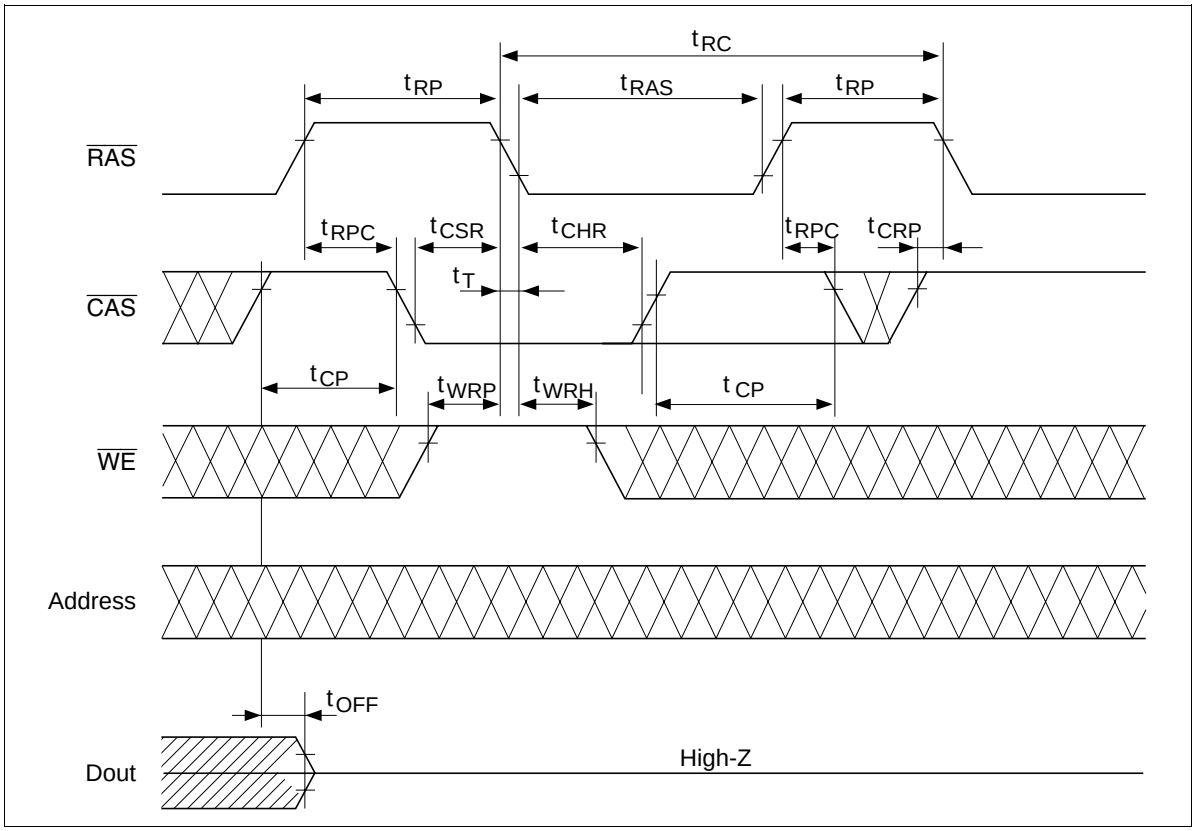
Early Write Cycle



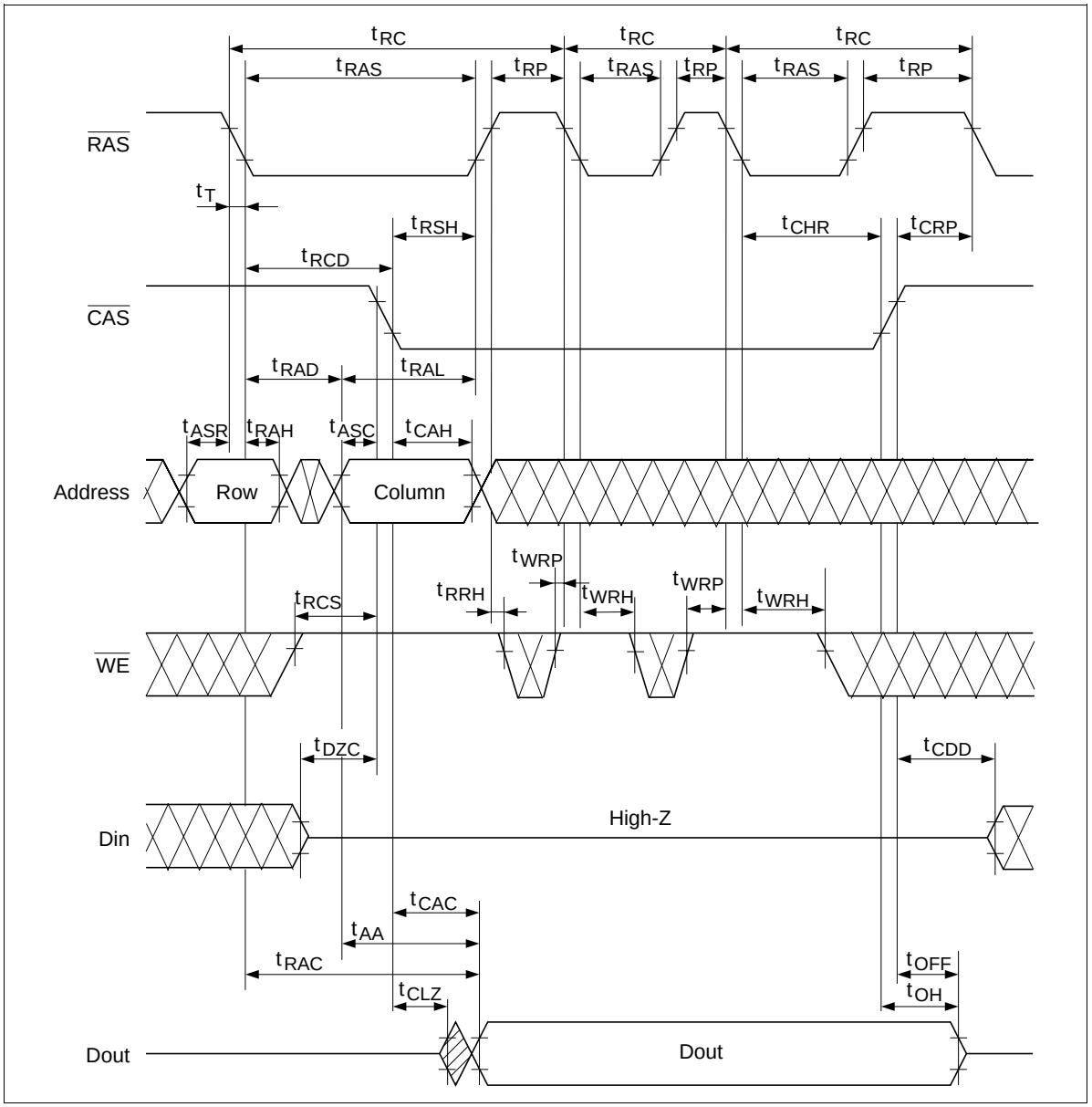
$\overline{\text{RAS}}$-Only Refresh Cycle



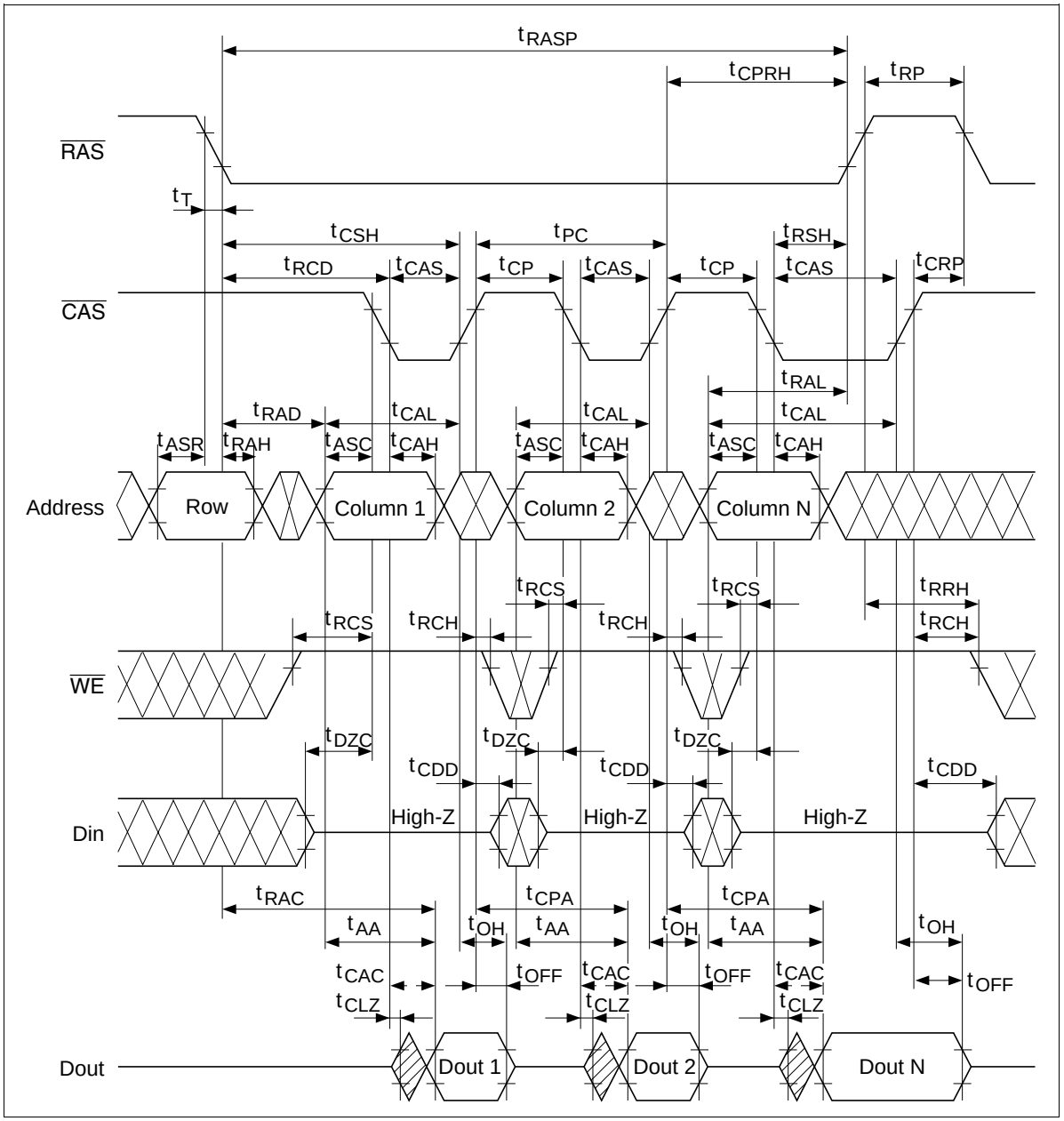
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



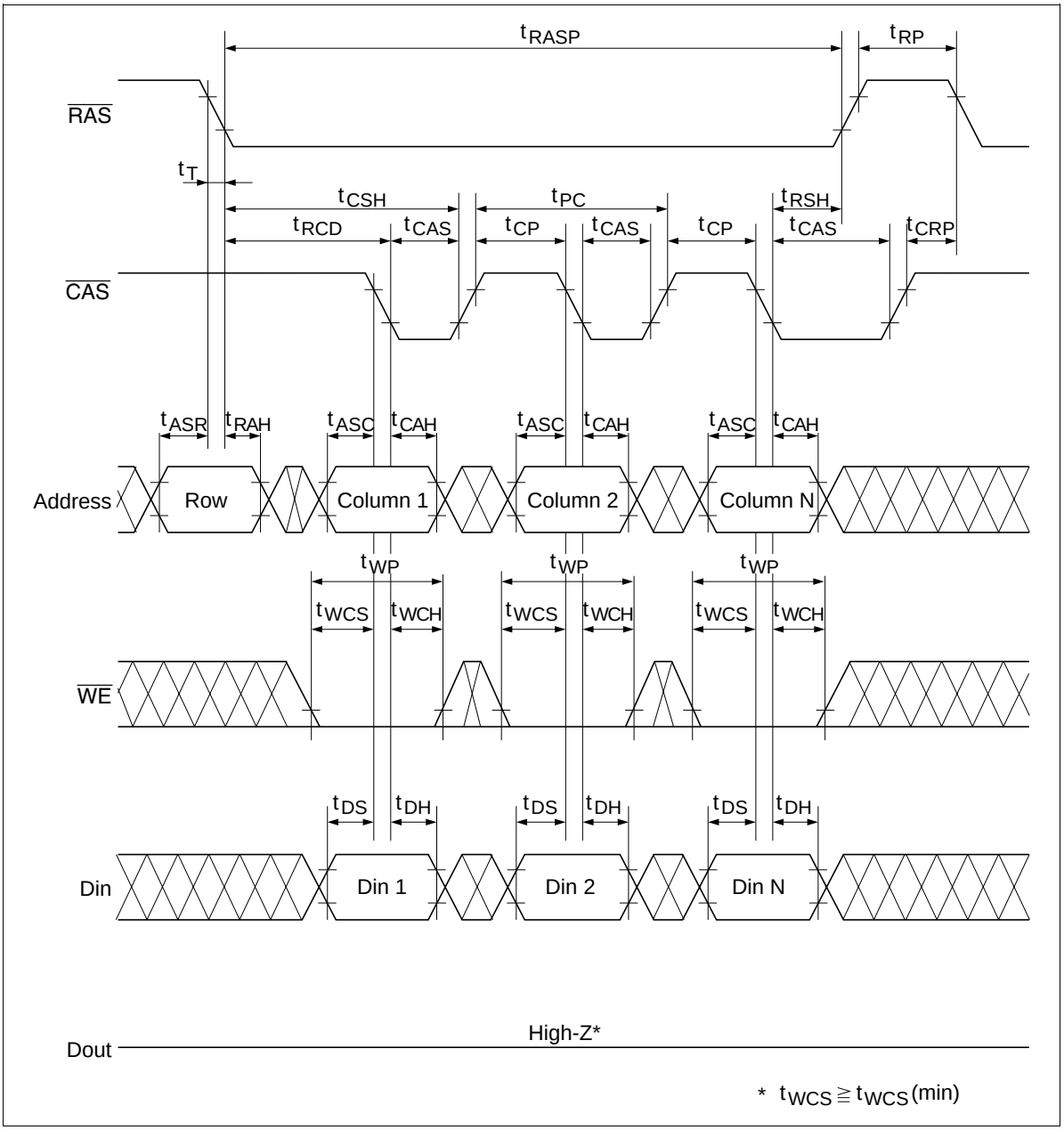
Hidden Refresh Cycle



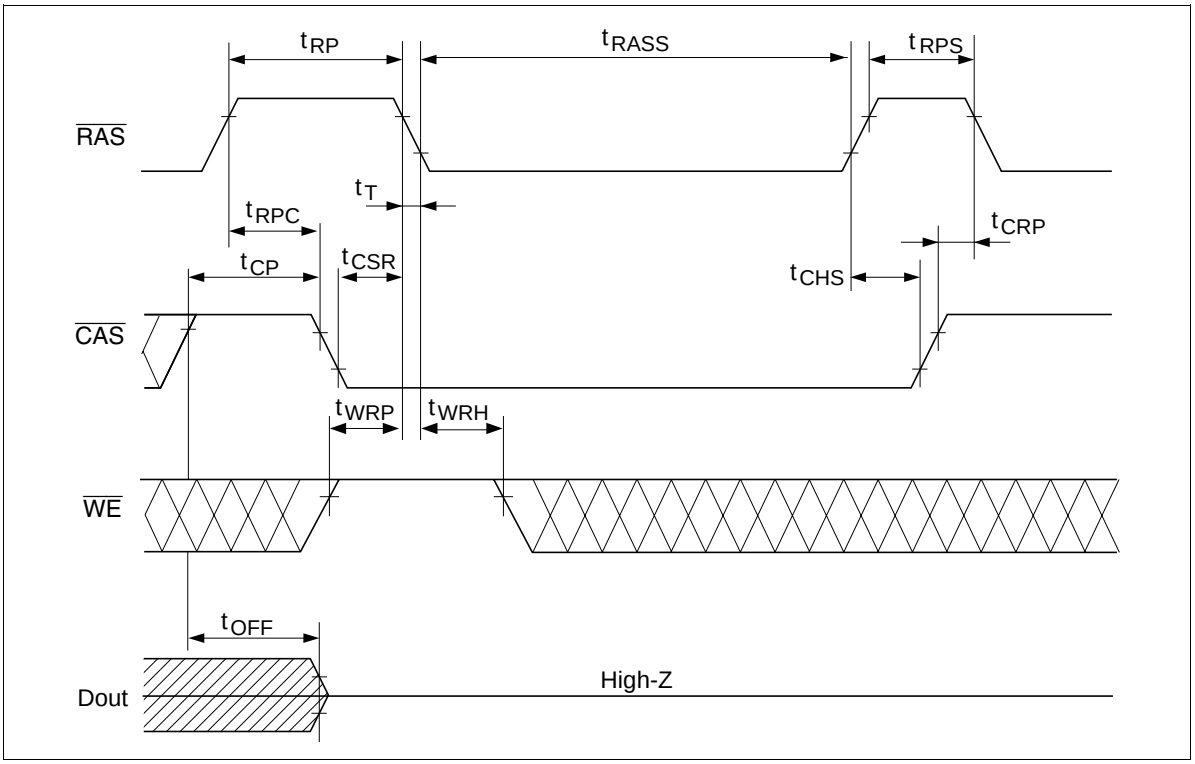
Fast Page Mode Read Cycle



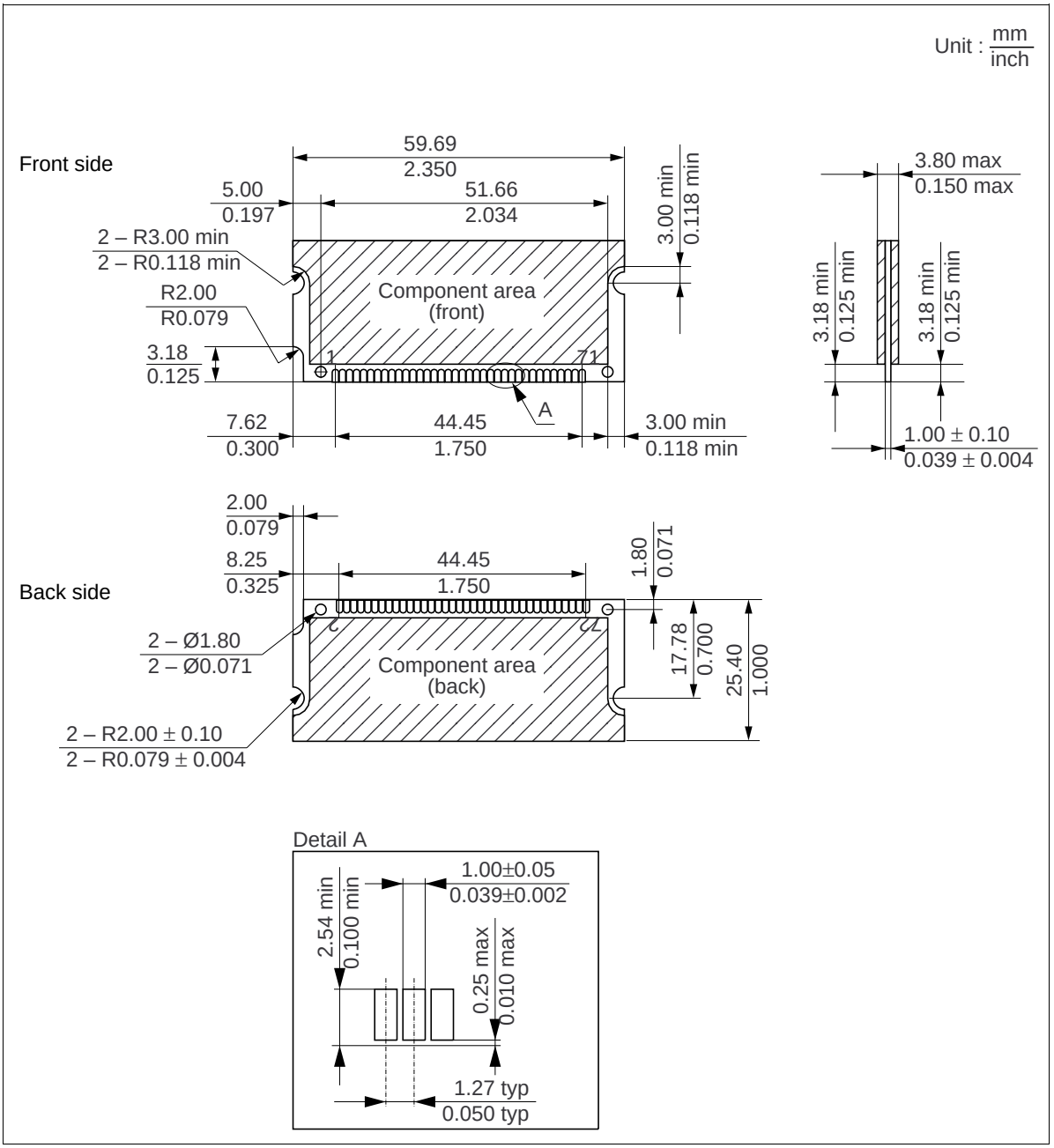
Fast Page Mode Early Write Cycle



Self Refresh Cycle (L-version)* [18, 19, 20, 21]



Physical Outline



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Revision Record

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1.0	Feb. 27, 1997	Initial issue		