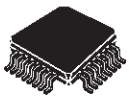
L5995

ACCURATE 4 BIT PROGRAMMABLE POWER SUPPLY CONTROLLER FOR MOBILE CPU

- PROGRAMMABLE OUTPUT FROM 1.3V TO 2.0V WITH 0.05V BINARY STEPS
- OUTPUT VOLTAGE RANGE EXTENDIBLE FROM 2V TO 3.5V
- ULTRA HIGH EFFICIENCY
- SEPARATE 5V BIAS SUPPLY AVAILABLE FOR HIGH EFFICIENCY PERFORMANCE
- EXCELLENT OUTPUT ACCURACY ±1% OVER LINE, LOAD AND TEMPERATURE VARIATIONS
- HIGH PRECISION INTERNAL REFERENCE DIGITALLY TRIMMED
- OPERATING SUPPLY VOLTAGE FROM 4.75V TO 25V
- VERY FAST LOAD TRANSIENT
- REMOTE SENSING INPUTS
- INTERNAL LINEAR REGULATOR 2.5V /150mA, ±2% PRECISION
- POWER MANAGEMENT
  - PROGRAMMABLE POWER-UP TIME
  - POWER GOOD OUTPUT, SKIP MODE
  - OUTPUT OVERVOLTAGE PROTECTION
  - OUTPUT UNDERVOLTAGE LOCKOUT
- OPERATING FREQUENCY UP TO 1MHz
- MEETS INTEL MOBILE PENTIUM II



TQFP32
(7mm x 7mm)

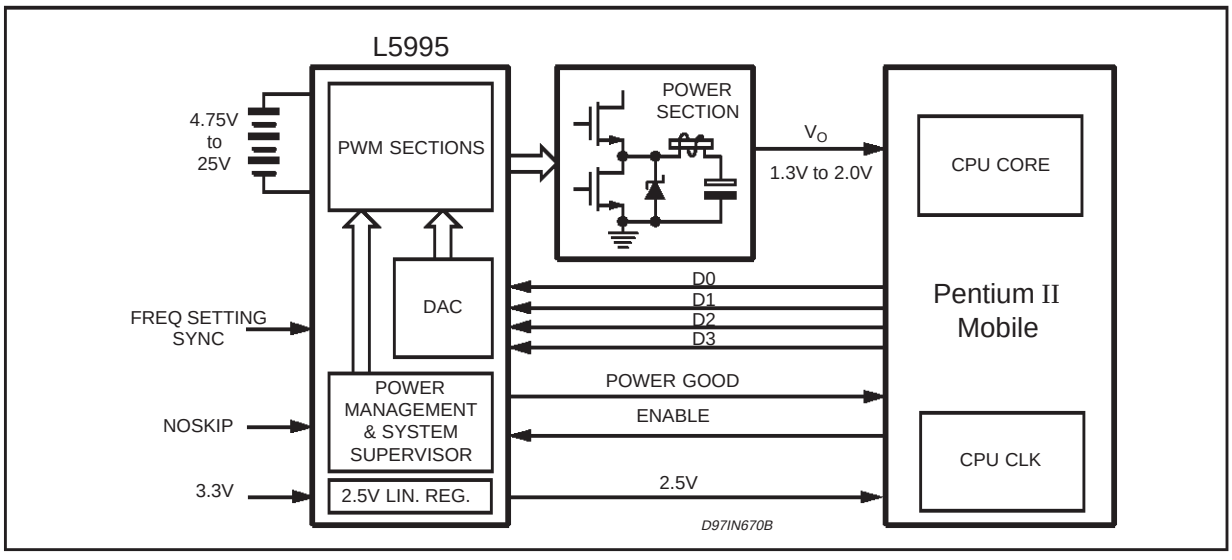
Application

- ADVANCED MICROPROCESSOR SUPPLIES
- POWER SUPPLY FOR PENTIUM II INTEL MOBILE

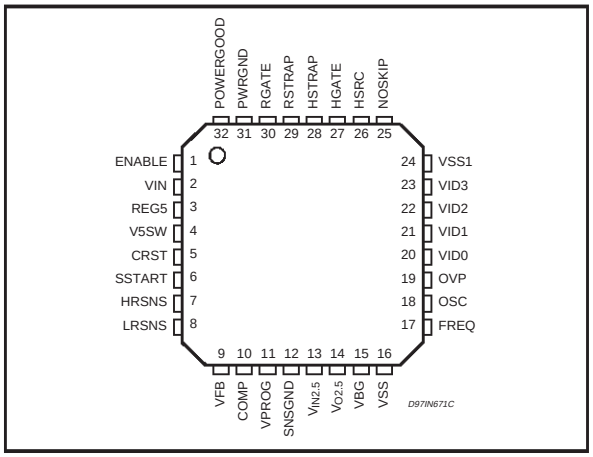
DESCRIPTION

The L5995 is a power supply controller that offers a complete power management for notebook CPUs of the next generation especially for mobile Pentium II. A high precise 4 bit digital to analog converter (DAC) allows to adjust the output voltage from 1.3V to 2.0V with 0.05V binary steps. The reference can be programmed with an auxiliary bit between 2.1V and 3.5V with 0.1V steps. The high precision internal reference, digitally trimmed, assures the selected output voltage to

TYPICAL APPLICATION CIRCUIT



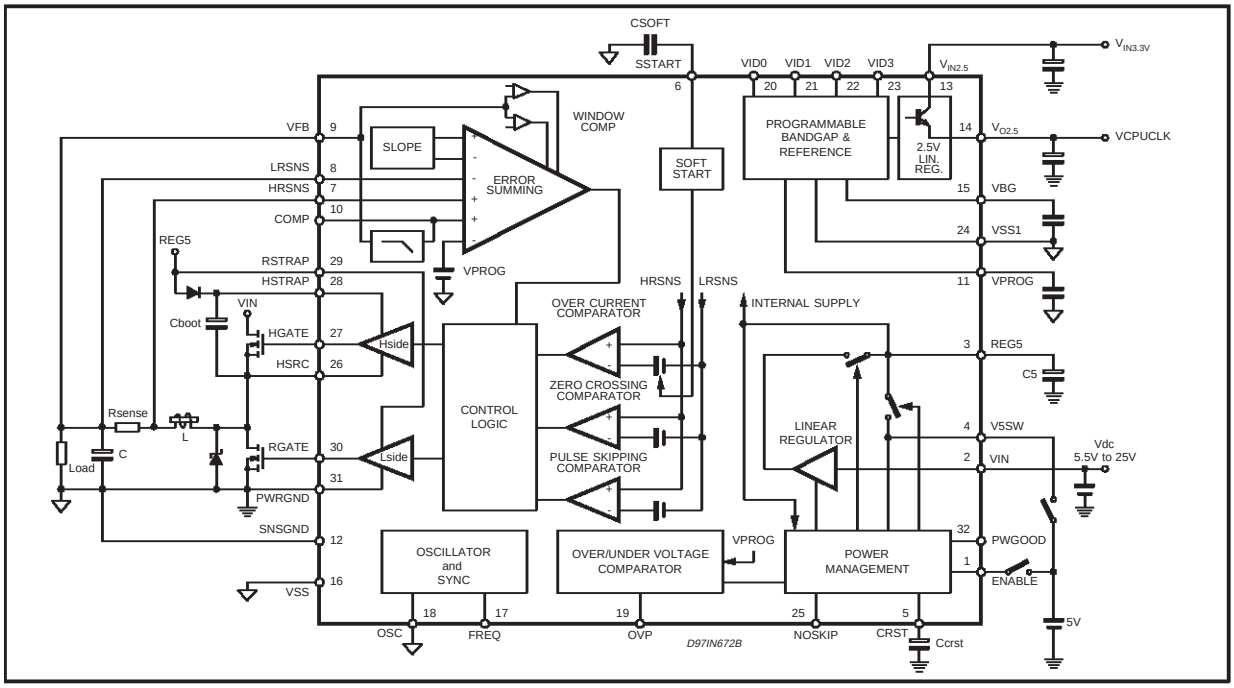
PIN CONNECTION



DESCRIPTION (Continued)

within +/-1% over temperature and battery voltage variations. Thanks to the remote sensing inputs and to the window comparator system, embedded in the error summing structure, the device provides excellent load transient performance. The high peak current gate drive affords to have fast switching to the external power mos, performing an high efficiency. A complete power management include on board a programmable power-up sequencing, power good signal, skip mode operation and undervoltege detection. The L5995 assures a fast protection against load overvoltage and load overcurrent. Linear regulator on-board is available with an output voltage of 2.5V (+/-2%) and a current capability of 150mA, useful for CPU CLOCK BUS.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	VIN to PWRGND	-0.5 to 27	V
	PWRGND to VSS	±0.5	V
	VREFS to PWRGND	5	V
	HSTRAP, HGATE to PWRGND	-0.5V to VIN+14V	
	RSTRAP, RGATE to PWRGND	-0.5V to 14V	
	EABLE, FREQ, OSC, COMP, VFB, HRSNS, LRSNS	5	V
	VID0-3, NOSKIP, V_{SS1}	7	V
T_j	Junction Temperature Range	-40 to 150	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{Th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 12V; T_i = 25°C, OSC = GND, unless otherwise specified)
● = specifications referred to T_J from 0 to 70°C.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
V_{IN}	Input Supply Voltage		●	4.75		25	V
I_{OP}	Operating Quiescent Current	RGATE = HGATE = OPEN ENABLE = REG5	●		650	800	µA
I_{SB}	Stand-By Current	ENABLE = GND VIN = 12V V_{IN} = 25V	●		 80 100	 150 180	 µA µA
INTERNAL REGULATOR (VREG5)							
V_{REG5}	Output Voltage	V_{IN} = 6V to 25V I_{LOAD} = 0 to 5mA, C_{REG5} = 4.7µF		4.9	5.0	5.1	V
I_{REG5}	Total Current Capability	CREG5 = 4.7µF V_{IN} = 5.5V $V_{IN} \geq$ 6V		 25		 60	 mA mA
	Switch-Over Threshold Voltage			4.3	4.5	4.7	V
	Current Capability (internal switch on)	V_{5SW} = 4.5 to 5.5V $V_{REG5} \geq$ 4.4V		25			mA
2.5V REFERENCE VOLTAGE							
$V_{O\ 2.5}$	Regulated Voltage	$V_{IN\ 2.5}$ = 3.3V $C_{VO\ 2.5}$ = 47µF $I_{O\ 2.5}$ = 10mA	●	2.45	2.5	2.55	V
	Regulation over Line and Load	6V < V_{IN} < 25V $V_{IN\ 2.5}$ = 3.3V $I_{O\ 2.5}$ = 0-150mA	●	2.425	2.5	2.575	V
$I_{VO\ 2.5\ MAX}$	Current Limit	$V_{IN\ 2.5}$ = 3.3V				500	mA
PROGRAMMABLE REFERENCE VOLTAGE AND VBG							
V_{PROG}	Accuracy	V_{ID0}, V_{ID1}, V_{ID2}, V_{ID3}, V_{SS1} see Table 1.	●	-0.5%	V_{PROG}	+0.5%	V
V_{FB}	Ouput Voltage Accuracy	Line and Load Regulation included, V_{ID0}, V_{ID1}, V_{ID2}, V_{ID3}, V_{SS1}, see Table 1.	●	-1%	V_{PROG}	+1%	V
V_{BG}	Band Gap reference	C_{VBG} = 220nF	●	1.240	1.246	1.252	V
POWER MANAGEMENT							
	Enable Voltage	HIGH LEVEL		2.4			V
	Disable Voltage	LOW LEVEL				0.8	V
	Power Good Delay	C_{RST} = 10nF 16 cycles		120	160	200	ms
	Shutdown Delay Time before Low side activation (Except Over-Voltage Fault)	C_{RST} = 10nF 16 cycles		120	160	200	ms
	CRST Timing Rate				16		ms/nF
	Power Good Saturation Voltage	I_{sink} = 400µA				0.4	V
	NOSKIP Mode (Active high)	High Level Low Level		 2.4		0.8	V V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
	Output UVLO Threshold	OVP = GND		60	70	80	%
	Output UVLO Lockout Time	Depending on C_{SS} value			775		ms/µF
PROTECTION FUNCTIONS							
V_8-V_7	Over-Current Threshold Voltage	V_{SSTART} = 3.1V	●	31	35	39	mV
	Pulse Skipping Mode Threshold Voltage	NOSKIP = HIGH		3	6	10	mV
	Zero Crossing Threshold			-2		+2	mV
	Under-Voltage Threshold			Vprog -13%	Vprog -10%	Vprog -7%	V
	Over-Voltage Threshold	OVP = GND		Vprog +7%	Vprog +10%	Vprog +13%	V
	Over-Voltage Propagation Time					1.5	µs
	Under-Voltage Propagation Time					1.5	µs
SOFT START							
	Soft start source current			3.2	4	4.8	µA
	Soft start clamp voltage				3.1		V
OSCILLATOR AND SYNC							
f_{osc}	Fixed frequency	OSC =0V; FREQ = REG5	●	225	250	275	KHz
		OSC = REG5 FREQ = REG5	●	180	200	220	KHz
$f_{SINK\ MIN}$	Minimum Synchronizzable external frequency	FREQ = REG5 OSC = EXTERNAL SIGNAL				120	KHz
	Sync pulse width	Rising edge mode		200			ns
	Sync pulse amplitude			3		5.5	V
fosc	Operating switching frequency	Rext connected between FREQ and GND, Osc connect to REG5 or GND Rext = 680kΩ Rext = 40kΩ	●			 100 1	 kHz MHz
HIGH AND LOW SIDE GATE DRIVERS							
I_{OH5}	Output high source peak current	HSTRAP = RSTRAP = REG5			550		mA
R_{H5}	Output high sink impedance	I_{test} = 100mA, HSTRAP = RSTRAP = REG5			3.5		Ω
I_{OH12}	Output high source peak current	HSTRAP = RSTRAP = 12V			2		A
R_{H12}	Output high sink impedance	I_{test} = 100mA, HSTRAP - RSTRAP = 12V			2		Ω
I_{OL5}	Output low peak current	HSTRAP = RSTRAP = 5V			500		mA
R_{L5}	Output low impedance	Itest = 100mA, HSTRAP = RSTRAP = 5V			3		Ω
I_{OL12}	Output low peak current	HSTRAP = RSTRAP = 12V			2		A
R_{L12}	Output low Impedance	I_{test} = 100mA, HSTRAP = RSTRAP = 12V			2		Ω
T_{CC}	Dead Time	GATE low to high		60			ns

FUNCTIONAL PIN DESCRIPTION

ENABLE(pin1): Enable input. A high level (>2.4V) enables the device, a low level (<0.8V) shuts it down. As ENABLE drops below 0.8V, the drivers are turned off and all internal functions are disabled except REG5. In this condition the stand by current is less than 80µA at VIN = 12V.

VIN(pin2): Device supply voltage. Input voltage range at this pin is 4.75V to 25V and the operating current requirement at 12V is 650µA.

REG5(pin3): 5V Regulator supply. Used also to supply the bootstrap capacitor. A minimum 2.2µF ceramic capacitor connected to PWRGND is required.

V5SW(pin4): 5V supply line. Connecting to 5V bus(4.75V to 5.5V) the device is no longer powered by VIN but by this pin and the internal linear regulator is disconnected increasing the efficiency.

CRST(pin5): Control start up. An external capacitor connected to this pin defines the delay between the output voltage Vo has reached 90% of VPROG and POWERGOOD leading edge signal will start to go high. This delay could be calculated using the follows formula: Tst(ms)=16*C(µF).

SSTART(pin6): Soft Start. The soft-start time is programmed by an external capacitor connected between this pin and SGND. The internal current generator forces 4µA through the capacitor implementing the soft start function.

HRSNS(pin7): Error summing current sense non inverting input.

LRSNS(pin8): Error summing current sense inverting input.

VFB(pin9): Regulator voltage feedback input. Connect close to the CPU input supply pin realise an accurate voltage regulation. VFB internally is connected to the window comparator that is used to increase the performance during the load transient.

COMP(pin10): Regulator stability compensation pin. The compensation is realised internally and normally it is not necessary to connect any external components to this pin .

VPROG(pin11): Reference voltage test pin. This pin provides the DAC output and should be decoupled to ground using a 0.22µF ceramic capacitor. No load has to be connected.

SNSGND(pin12): Remote ground sense. This pin is internally connected to the low power circuitry and for a precise output voltage regulation can be connected to the output capacitor negative terminal.

$V_{IN2.5}$(pin13): 2.5V linear supply voltage. Is available on-chip a linear regulator useful for the 2.5V bus. A max input voltage of 3.3V is recommended at Iomax (150mA).

$V_{O2.5}$(pin14): 2.5V linear regulator output. The linear regulator is realised with an internal NPN transistor with +/-2% output accuracy. A minimum of 47µF capacitor connected versus PWRGND is required.

VBG(pin15): Band-gap reference voltage. A min 220nF ceramic capacitor is required to assure the band gap stability and noise immunity.

VSS(pin16): Signal ground. This pin could be connected to the PWRGND pin.

FREQ(pin17): Connecting an external resistor versus ground is possible to select the switching frequency between 100kHz and 1MHz. Using an Rext=680k the fsw is 100kHz, using an Rext = 40k the fsw is 1MHz. In this condition is recommended to connect the OSC pin to REG5 or to VSS.

OSC(pin18): Connecting to REG5 is able to set the switching frequency at 250kHz, connecting to VSS is able to set the switching frequency at 300kHz. An external pulsed signal, with an amplitude higher than 2.4V, could synchronise the device. In all these conditions pin FREQ has to be connected to REG5.

OVP(pin19): Over voltage protection pin. If connected ti GND the device works in normal operation activating OVP and UVLO output controls. If connected to REG5 the OVP and UVLO controls are disabled. If OVP = GND and ENABLE = GND or the NO-CPU condition is set the high side is maintained off and the low side is on. If OVP = REG5 and ENABLE = GND or the NO-CPU condition is set the high side and the low side are maintained off.

VID0-3(pin20-23): Voltage Identification code input. These open collector compatible inputs are used to program the output voltage as specified in Table 1. Every pin has an internal pull up. If all four pins are high or floating, the output voltage and the 2.5V regulator are suspended and the POWERGOOD is low.

VSS1(pin24): See Table 1.

NOSKIP(pin25): Pulse skipping mode control. A high level (>2.4V) disables pulse skipping in low load condition, a low level (>0.8V) enables it.

HSRC(pin26): High side N-Channel switch source connection. This pin provides the return path for the high side driver.

HGATE(pin27): Gate driver output, high side N-Channel switch. The driver internal impedance is about 4Ω at VIN=12V.

HSTRAP(pin28): Bootstrap capacitor pin. This pin provide to supply the high side driver sinking the current by the bootstrap capacitor.

RSTRAP(pin29): Synchronous rectifier gate driver supply voltage. This pin could be connected to REG5 to reduce the switching losses due to the external mosfets gate capacitance. This is useful to maintain an high efficiency at light load.

RGATE(pin30): Gate driver output, low side N-Channel switch. The driver internal impedance is about 3Ω at VIN=12V.

PWRGND(pin31): Power ground. This pin has to be connected closely to the low side mosfet source in order to reduce the noise injected into the IC.

POWER GOOD(pin32): Open drain power good output. This pin is pulled low if the output voltage is not within ±10% and the 2.5V output is lower than 2.175V (-13%). The pin is pulled low also if REG5, VPROG and VBG have not reached the expected values. This test could be useful in an assembling fault condition

Table 1. Output voltage.

				OUTPUT VOLTAGE (V_{FB})	
VID3 (PIN 23)	**VID2 (PIN 22)**	**VID1 (PIN 21)**	**VID0 (PIN 20)**	**V_{SS1} = GND**	**V_{SS1} = REG5**
1	1	1	1	NO CPU	NO CPU
1	1	1	0	1.30	2.1
1	1	0	1	1.35	2.2
1	1	0	0	1.40	2.3
1	0	1	1	1.45	2.4
1	0	1	0	1.50	2.5
1	0	0	1	1.55	2.6
1	0	0	0	1.60	2.7
0	1	1	1	1.65	2.8
0	1	1	0	1.70	2.9
0	1	0	1	1.75	3.0
0	1	0	0	1.80	3.1
0	0	1	1	1.85	3.2
0	0	1	0	1.90	3.3
0	0	0	1	1.95	3.4
0	0	0	0	2.00	3.5

Figure 1. Application Circuit

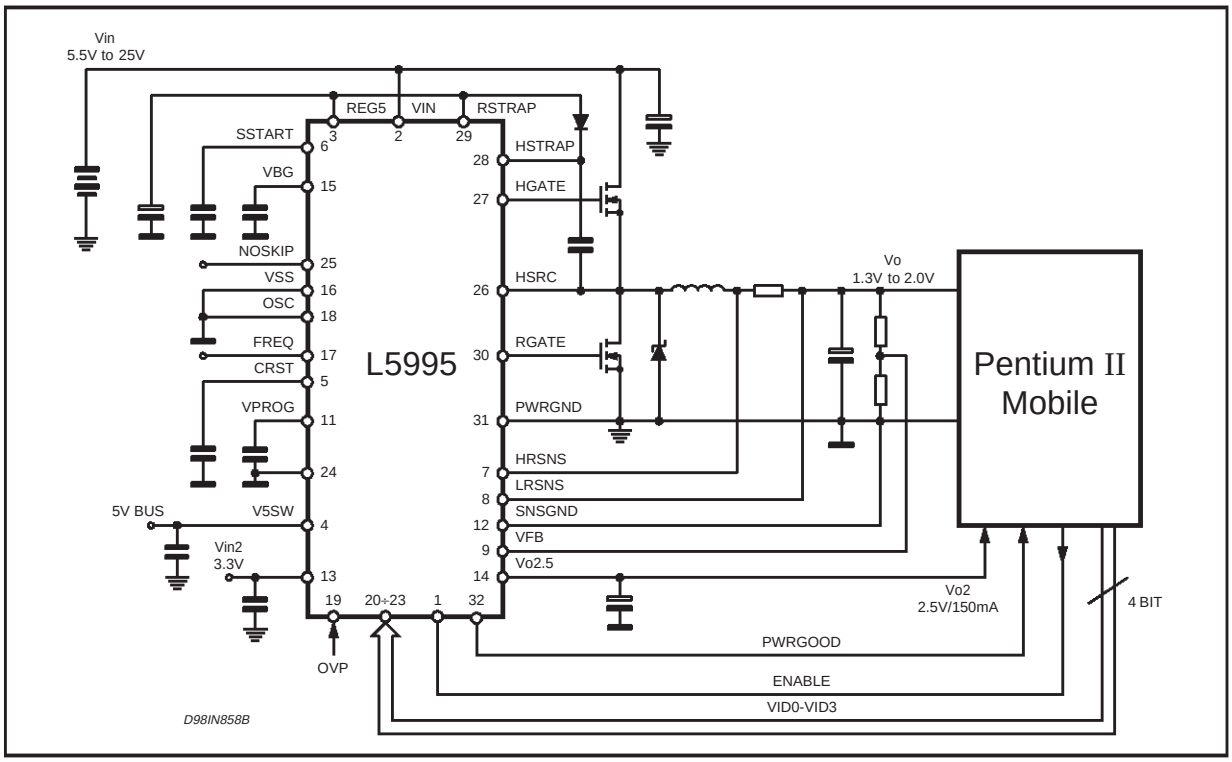


Figure 2. Application Circuit (Supply by 5V bus)

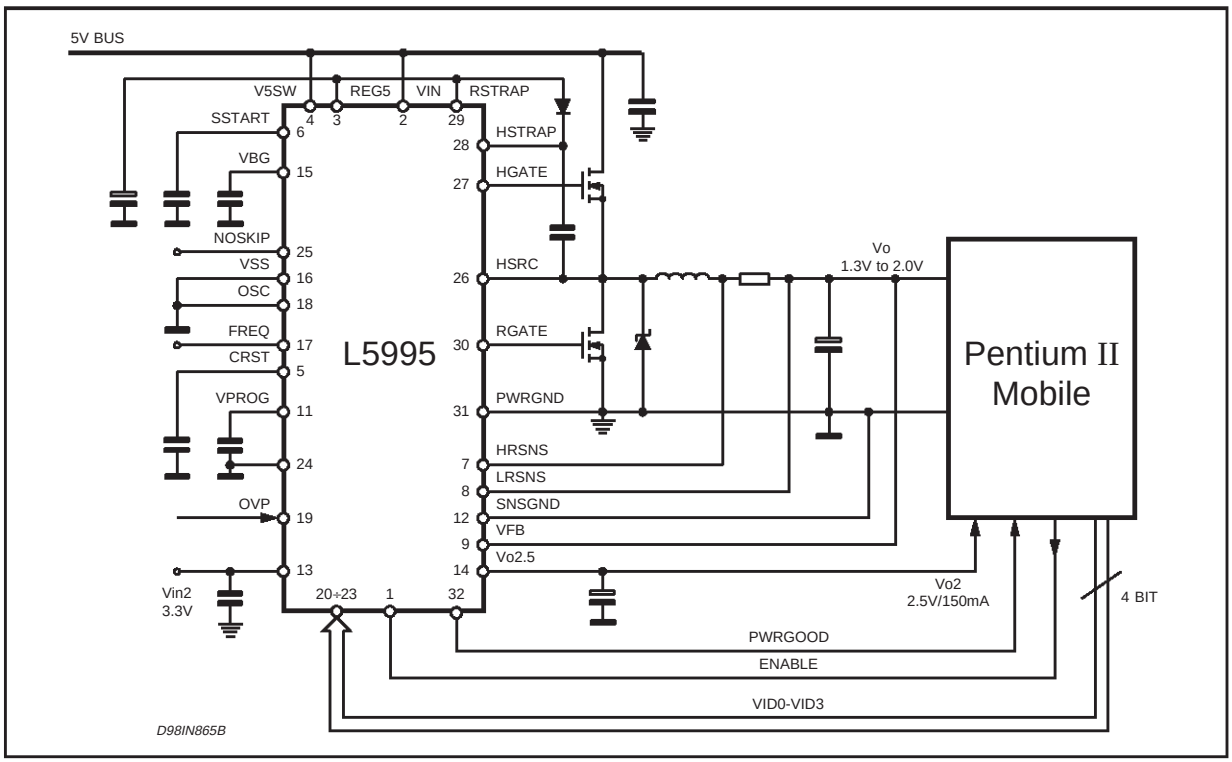


Figure 3. Start up, enable and disable signals.

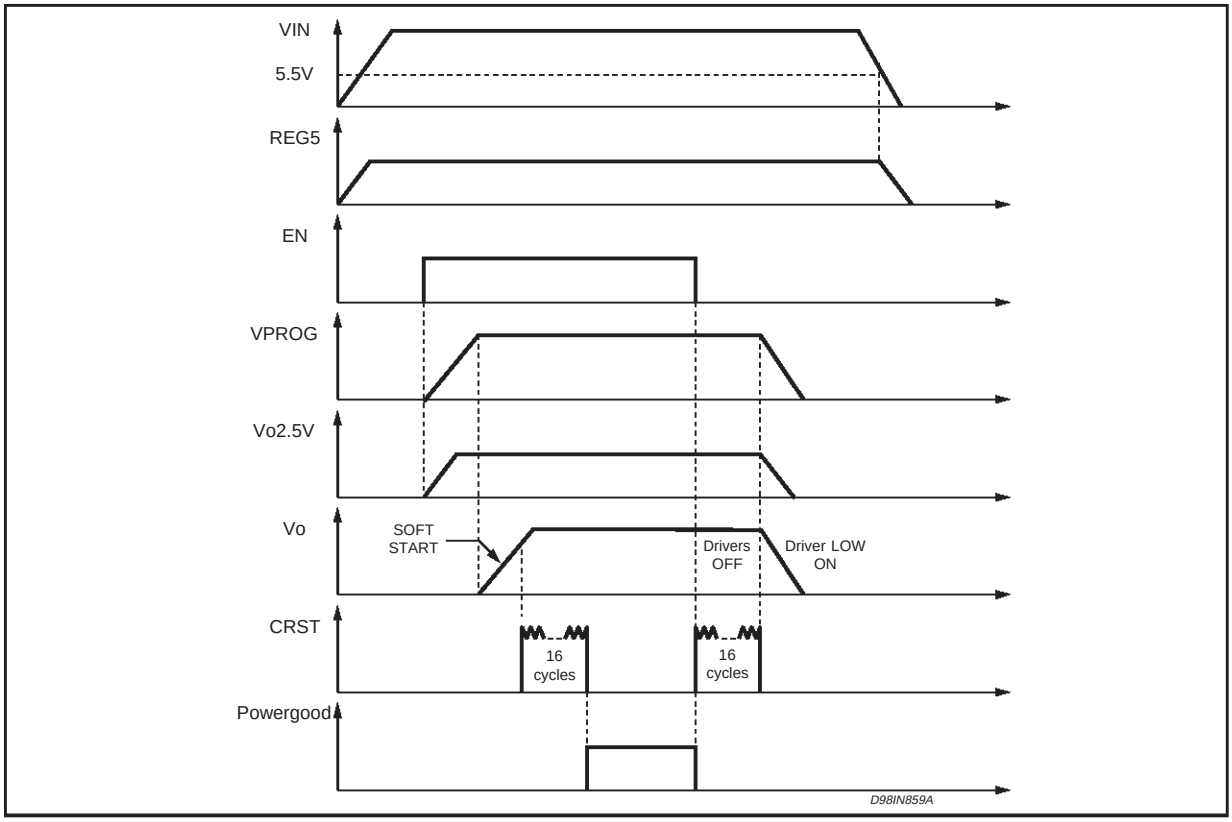
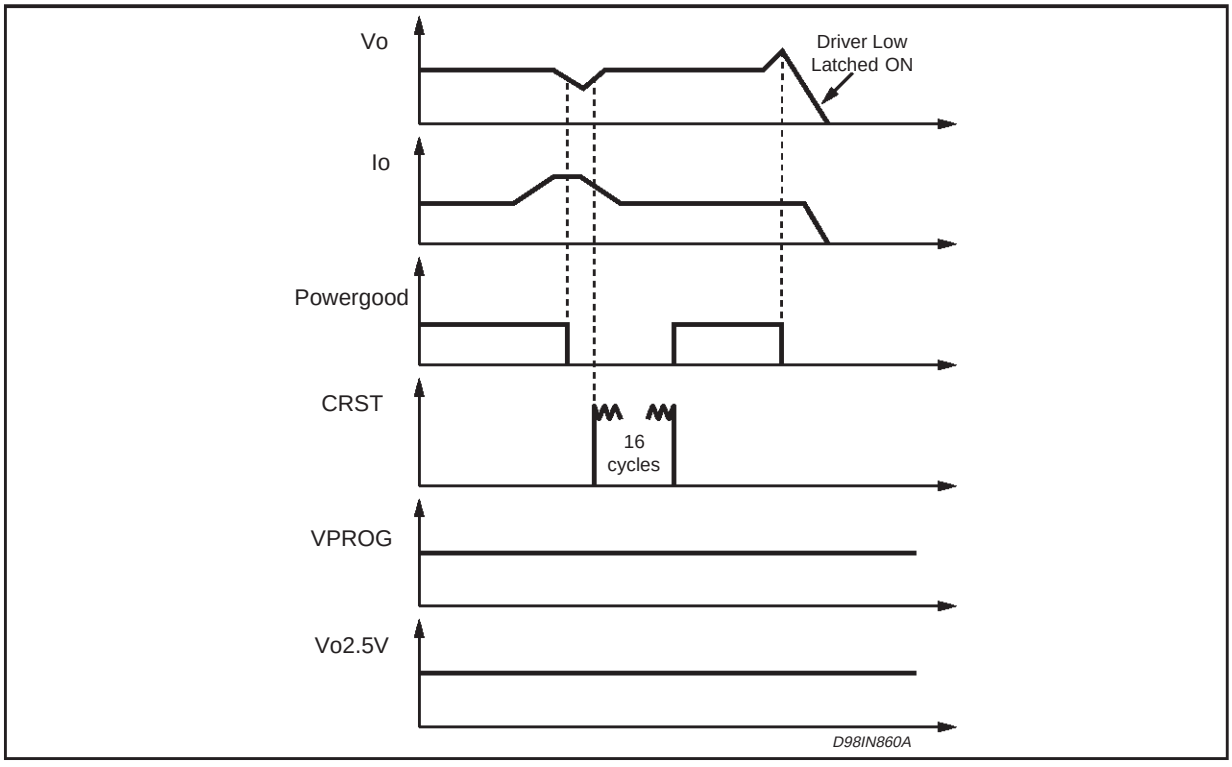
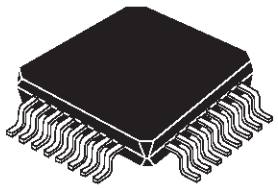


Figure 4. Overcurrent and overvoltage protection.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.60			0.220	
e		0.80			0.031	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.60			0.220	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



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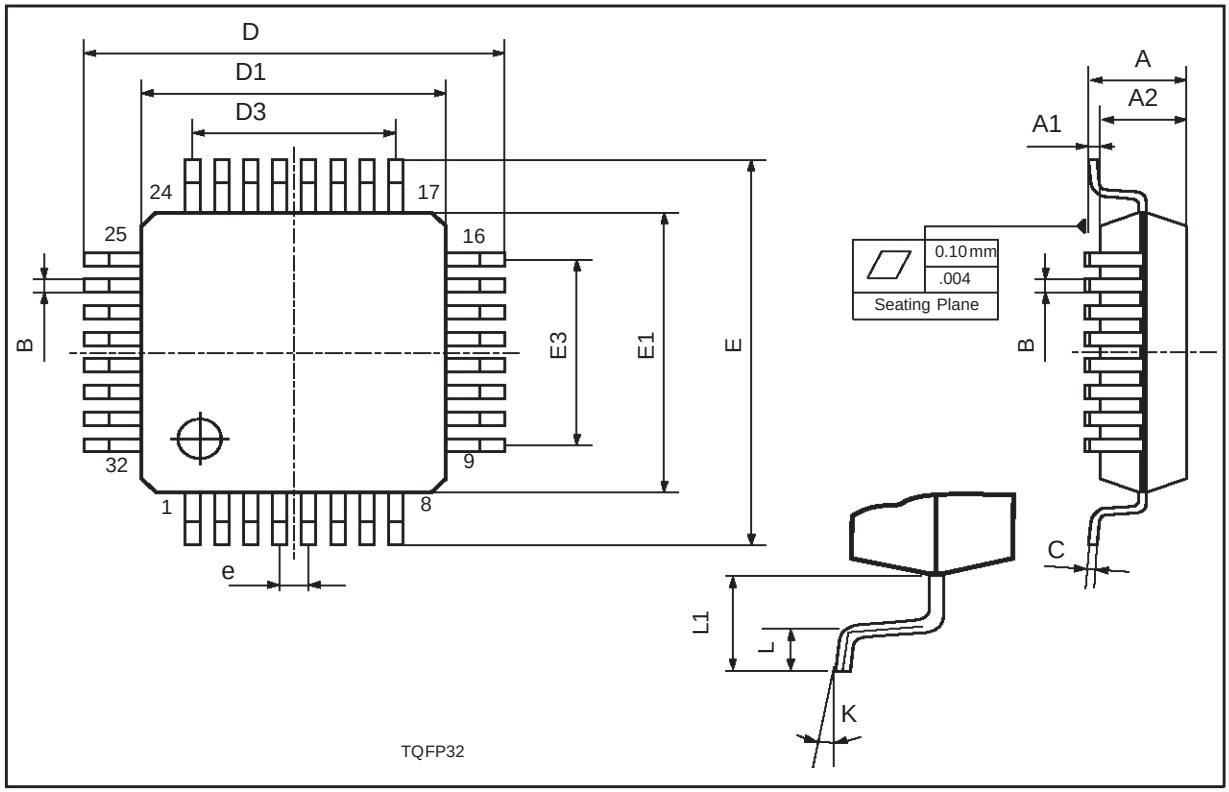

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