HM62P1321 Series

32768-word × 32-bit Synchronous Fast Static RAM with Burst Counter and Pipelined Data Output

HITACHI

ADE-203-753 (Z)
Preliminary
Rev.0.0
Mar. 6, 1997

Features

- 3.3 V core power supply
- 2.5 V I/O power supply
- Fast clock access time: 8.0 ns (max)
- Clock cycle times: 15 ns (min)
- Address data pipeline capability
- Internal input registers (Address, Data, Control)
- Internal data output registers
- Internal self-timed write cycle
- $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ and $\overline{\text{ADV}}$ burst control pins (Supports interleaving)
- Asynchronous output enable controlled three-state outputs
- Individual byte write control and global write
- Power down state via ZZ
- Common data inputs and data outputs
- High board density 100-lead LQFP package

Ordering Information

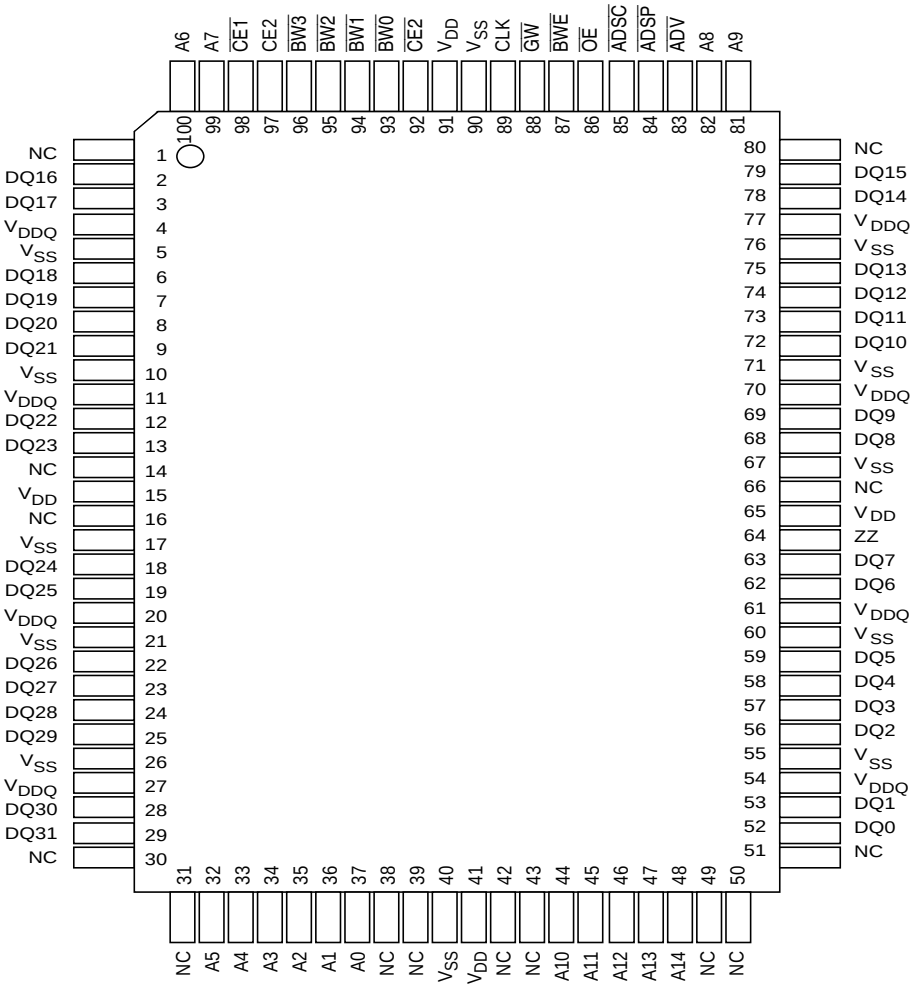
Type No.	Access time	CPU clock rate	Package
HM62P1321FP-15	8 ns	66 MHz	LQFP 100-pin (FP-100H)

Preliminary:The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

Hitachi semiconductor

Pin Arrangement

HM62P1321FP Series

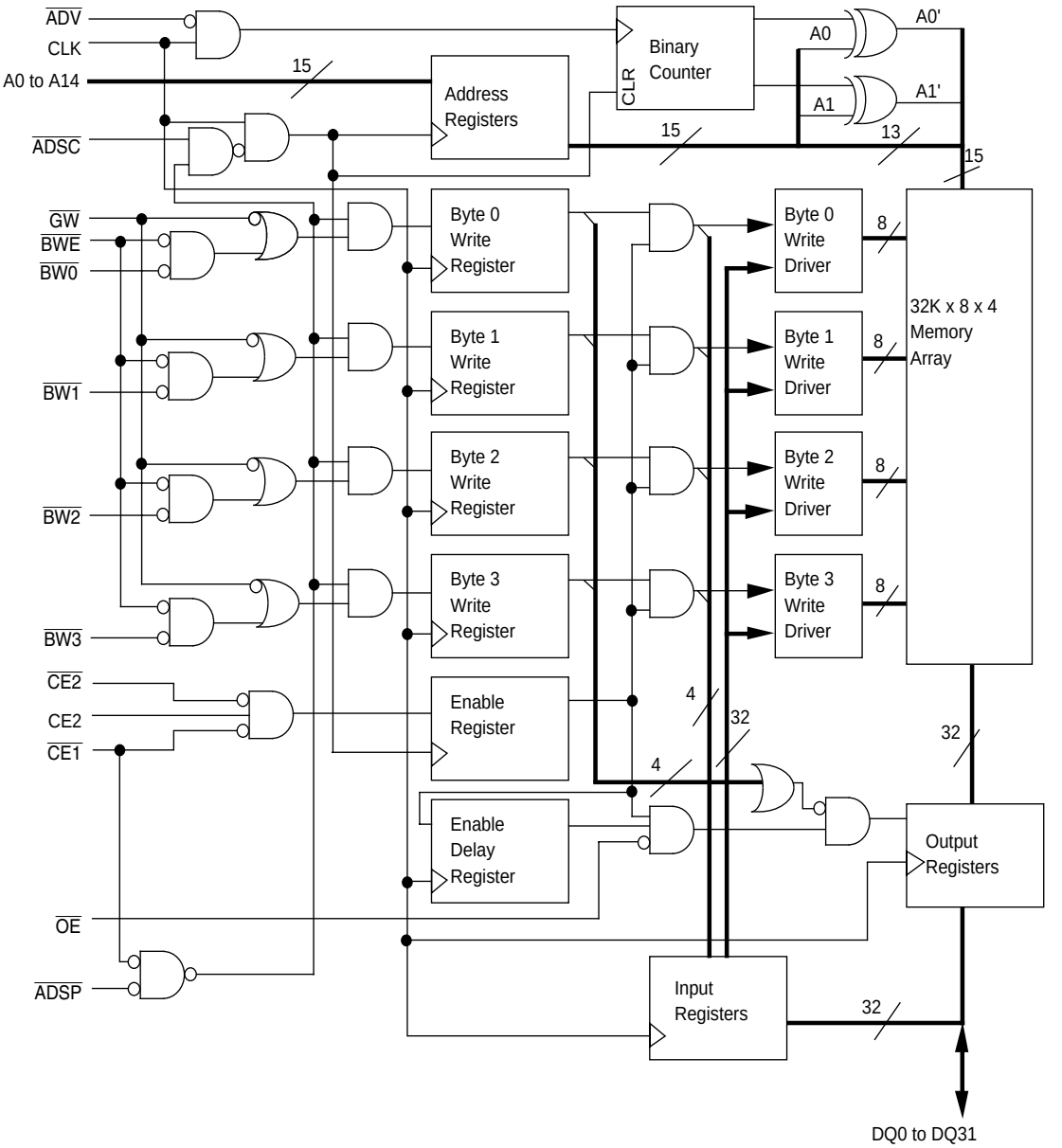


(Top view)

Pin Description (See Detailed Pin Description)

Pin name	Type	Function
A0 to A14	Input	Address inputs
$\overline{BW0}$, $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$	Input	Byte write enables $\overline{BW0}$ controls DQ0 to DQ7 $\overline{BW1}$ controls DQ8 to DQ15 $\overline{BW2}$ controls DQ16 to DQ23 $\overline{BW3}$ controls DQ24 to DQ31
$\overline{GW}$	Input	Global write
$\overline{BWE}$	Input	Byte write enable
CLK	Input	Clock
$\overline{CE1}$	Input	Enable
$\overline{CE2}$, CE2	Input	Chip enable
$\overline{OE}$	Input	Output enable
$\overline{ADV}$	Input	Address advance
$\overline{ADSP}$	Input	Address status processor
$\overline{ADSC}$	Input	Address status controller
NC	—	No connection
DQ0 to DQ31	Input/Output	
V_{DD}	Supply	Power supply
V_{DDQ}	I/O Supply	I/O power supply
V_{SS}	Supply	Ground
ZZ	Input	Power down (Snooze)

Block Diagram



Note: The functional block diagram illustrates simplified device operation.
See truth table, detailed pin descriptions and timing diagrams for detailed information.

Synchronous Truth Table

Operation	Address	$\overline{CE1}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{Write}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	×	×	×	L	×	×	×	L-H	High-Z
Deselected cycle, power-down	None	L	×	L	L	×	×	×	×	L-H	High-Z
Deselected cycle, power-down	None	L	H	×	L	×	×	×	×	L-H	High-Z
Deselected cycle, power-down	None	L	×	L	H	L	×	×	×	L-H	High-Z
Deselected cycle, power-down	None	L	H	×	H	L	×	×	×	L-H	High-Z
READ cycle, begin burst	External	L	L	H	L	×	×	×	L	L-H	Q
READ cycle, begin burst	External	L	L	H	L	×	×	×	H	L-H	High-Z
WRITE cycle, begin burst	External	L	L	H	H	L	×	L	×	L-H	D
READ cycle, begin burst	External	L	L	H	H	L	×	H	L	L-H	Q
READ cycle, begin burst	External	L	L	H	H	L	×	H	H	L-H	High-Z
READ cycle, continue burst	Next	×	×	×	H	H	L	H	L	L-H	Q
READ cycle, continue burst	Next	×	×	×	H	H	L	H	H	L-H	High-Z
READ cycle, continue burst	Next	H	×	×	×	H	L	H	L	L-H	Q
READ cycle, continue burst	Next	H	×	×	×	H	L	H	H	L-H	High-Z
WRITE cycle, continue burst	Next	×	×	×	H	H	L	L	×	L-H	D
WRITE cycle, continue burst	Next	H	×	×	×	H	L	L	×	L-H	D
READ cycle, suspend burst	Current	×	×	×	H	H	H	H	L	L-H	Q
READ cycle, suspend burst	Current	×	×	×	H	H	H	H	H	L-H	High-Z
READ cycle, suspend burst	Current	H	×	×	×	H	H	H	L	L-H	Q
READ cycle, suspend burst	Current	H	×	×	×	H	H	H	H	L-H	High-Z
WRITE cycle, suspend burst	Current	×	×	×	H	H	H	L	×	L-H	D
WRITE cycle, suspend burst	Current	H	×	×	×	H	H	L	×	L-H	D

Notes: 1. H means logic HIGH, L means logic LOW. × means H or L. $\overline{Write}$ = L means any one or more byte write enable signals ($\overline{BW0}$, $\overline{BW1}$, $\overline{BW2}$ or $\overline{BW3}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{Write}$ = H means all byte write enable signals and $\overline{GW}$ are HIGH.

2. $\overline{BW0}$ enables write to Byte0 (DQ0 to DQ7). $\overline{BW1}$ enables write to Byte1 (DQ8 to DQ15). $\overline{BW2}$ enables write to Byte2 (DQ16 to DQ23). $\overline{BW3}$ enables write to Byte3 (DQ24 to DQ31).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and hold HIGH throughout the input data hold time.
6. $\overline{ADSP}$ = LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

Asynchronous Truth Table

Operation	ZZ	$\overline{OE}$	I/O status
Read	L	L	Data out
Read	L	H	High-Z
Write	L	×	High-Z, Data in
Deselect	L	×	High-Z
Power down (Snooze)	H	×	HIgh-Z

Note: H means logic HIGH. L means logic LOW. × means H or L.

Partial Truth Table for Writes

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$
Read	H	H	×	×	×	×
Read	H	×	H	H	H	H
Write byte 0	H	L	L	H	H	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	×	×	×	×	×

Note: H means logic HIGH. L means logic LOW. × means H or L.

Interleave Sequence Table

Parameter	A14 to A2	Sequence 1 (A1, A0)	Sequence 2 (A1, A0)	Sequence 3 (A1, A0)	Sequence 4 (A1, A0)
External address	A14 to A2	0 0	0 1	1 0	1 1
1st internal address	A14 to A2	0 1	0 0	1 1	1 0
2nd internal address	A14 to A2	1 0	1 1	0 0	0 1
3rd internal address	A14 to A2	1 1	1 0	0 1	0 0

Note: Each Sequence wraps around to its initial state upon completion.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Core Supply voltage	V_{DD}	–0.5 to +4.6	V
I/O supply voltage	V_{DDQ}	–0.5 to V_{DD}	V
Voltage on any pins relative to V_{SS} (Except V_{DD})	V_T	–0.5 to V_{DD} +0.5	V
Power dissipation	P_T	1.2	W
Operating temperature	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Core Supply voltage (Operating voltage range)	V_{DD}	3.135	3.465	V	
I/O Supply voltage (Operating voltage range)	V_{DDQ}	2.375	2.900	V	
Supply voltage to V_{SS}	V_{SS}	0.0	0.0	V	
Input high voltage	V_{IH}	1.7	V_{DDQ} +0.3	V	1
Input low voltage	V_{IL}	–0.3	0.7	V	2

Notes: 1. V_{DDQ} + 1.9 V for overshoot pulse width ≤ t_{CYC} min/2.
2. –1.9 V for undershoot pulse width ≤ t_{CYC} min/2.

DC Characteristics (Ta = 0 to +70°C, V_{DD} = 3.3 V ±5 %, V_{DDQ} = 2.375 V to 2.9V, unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input leakage current	I_{LI}	–2	2	µA	All inputs Vin = V_{SS} to V_{DDQ}
Output leakage current	I_{LO}	–2	2	µA	$\overline{OE}$ = V_{IH}, Vout = V_{SS} to V_{DDQ}
Supply current	I_{DD}	—	140	mA	Device selected Iout = 0 mA, all inputs = V_{IH} or V_{IL}, Cycle time = t_{CYC} min. V_{DD} = Max
Standby current	I_{SB}	—	30	mA	Device deselected Iout = 0 mA, all inputs = fixed and all inputs ≥ V_{DDQ} – 0.2 V or ≤ 0.2 V, Cycle time = t_{CYC} min.
	I_{SB1}	—	5	mA	Device deselected, Output disabled all inputs = fixed and all inputs ≥ V_{DDQ} – 0.2 V or ≤ 0.2 V, V_{DD} = Max, Cycle time = ∞ (Frequency = 0 MHz)
	I_{SBzz}	—	5	mA	ZZ ≥ V_{DDQ} – 0.2 V
Output low voltage	V_{OL}	—	0.4	V	I_{OL} = 1 mA
Output high voltage	V_{OH}	2.0	—	V	I_{OH} = –1 mA

Capacitance (Ta = 25°C, f = 1.0 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input capacitance	Cin	2	4	5	pF	1
Input/output capacitance	$C_{I/O}$	4	7	8	pF	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{DD} = 3.3 V ±5 %, V_{DDQ} = 2.375 V to 2.9V, unless otherwise noted.)

Test Conditions

- Input timing measurement reference level: V_{DDQ} / 2
- Input pulse levels: 0 V to V_{DDQ}
- Input rise and fall edge rate: 1.5ns (20 % to 80 %)
- Output timing reference level: V_{DDQ} / 2
- Output load: See figure A unless otherwise noted

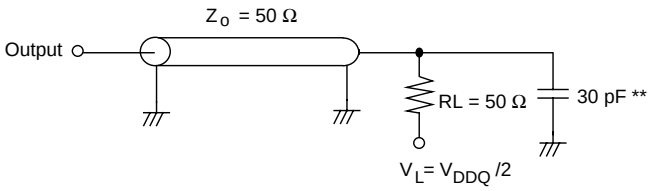


Figure A

**(including the capacitance of tester and jig)

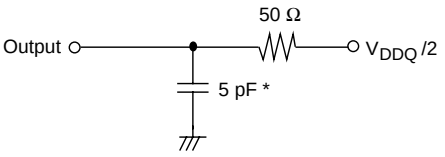


Figure B

*(including SCOPE and jig)

Parameter	Symbol		HM62P1321-15		Unit	Notes
	Standard	Alternate	Min	Max		
Cycle time	t_{KHKH}	t_{CYC}	15	—	ns	
Clock access time	t_{KHQV}	t_{ACK}	—	8.0	ns	
Output enable to output valid	t_{GLQV}	t_{OE}	—	5.0	ns	4
Clock high to output active	t_{KHQX1}	t_{CLZ}	1.5	—	ns	
Clock high to output change	t_{KHQX2}	t_{COH}	2.0	—	ns	
Output enable to output active	t_{GLQZ}	t_{OLZ}	0	—	ns	
Output disable to Q High-Z	t_{GHQZ}	t_{OHZ}	—	6.0	ns	1
Clock high to Q High-Z	t_{KHQZ}	t_{CHZ}	—	6.0	ns	1
Clock high pulse width	t_{KHKL}	t_{CH}	5.0	—	ns	
Clock low pulse width	t_{KLKH}	t_{CL}	5.0	—	ns	
Setup Times:			2.5	—	ns	2, 3
Address	t_{AVKH}	t_{SA}				
Address Status	t_{ADSVKH}	t_{SADS}				
Input Data	t_{DVKH}	t_{SD}				
Write	t_{WVKH}	t_{SW}				
Address Advance	t_{ADVVK}	t_{SADV}				
Chip Enable	t_{EVKH}	t_{SCE}				
Hold Times:			0.5	—	ns	2, 3
Address	t_{KHAX}	t_{HA}				
Address Status	t_{KHADSX}	t_{HADS}				
Input Data	t_{KHDX}	t_{HD}				
Write	t_{KHWX}	t_{HW}				
Address Advance	t_{KHADVX}	t_{HADV}				
Chip Enable	t_{KHEX}	t_{HCE}				
ZZ standby		t_{zzs}	6.0	—	ns	5, 6
ZZ Recovery		t_{zzrec}	6.0	—	ns	5

Notes: 1. Transition is measured ± 200mV from steady-state voltage with load of FigureB. This parameter is sampled.

2. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.

3. This is a synchronous device. All address must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other Synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.

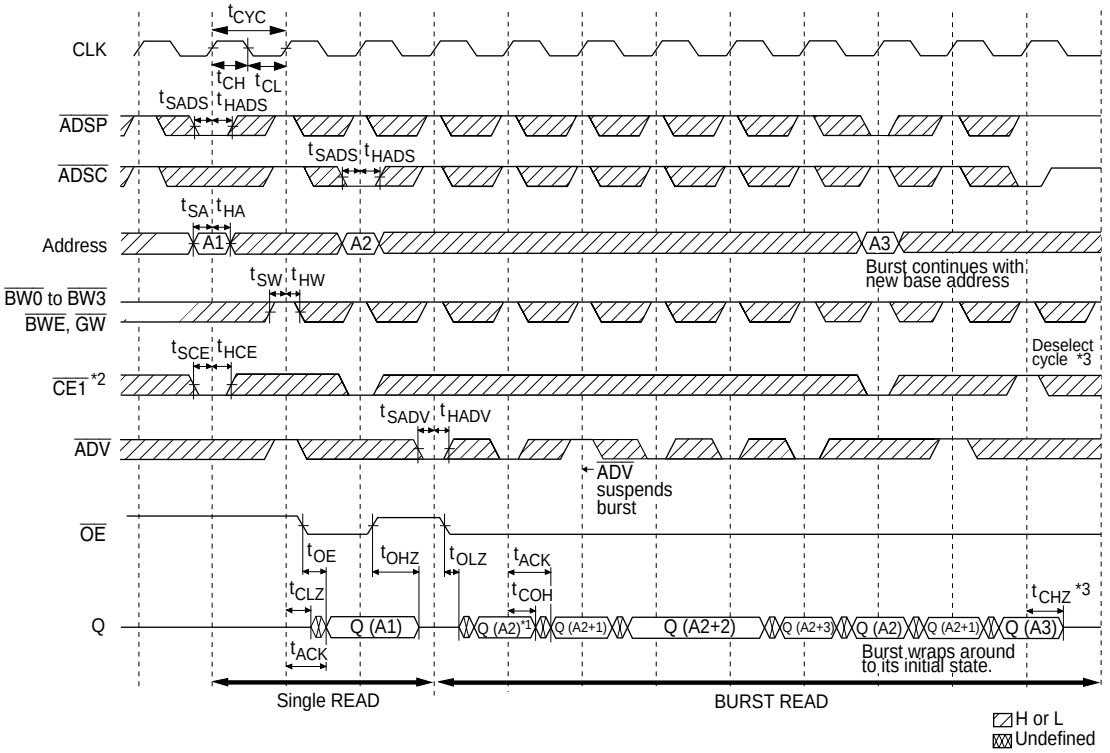
4. $\overline{OE}$ is a " H or L " when a byte write enable is sampled LOW.

5. During the cycle when transition of ZZ from high to low or from low to high occurs, $\overline{ADSP}$,$\overline{ADSC}$,$\overline{BWE}$,$\overline{GW}$ $\overline{Bwi}$ must be high at its rising edge of CLK.

6. Data-output is not guaranteed during the cycle when transition of ZZ from low to high occurs.

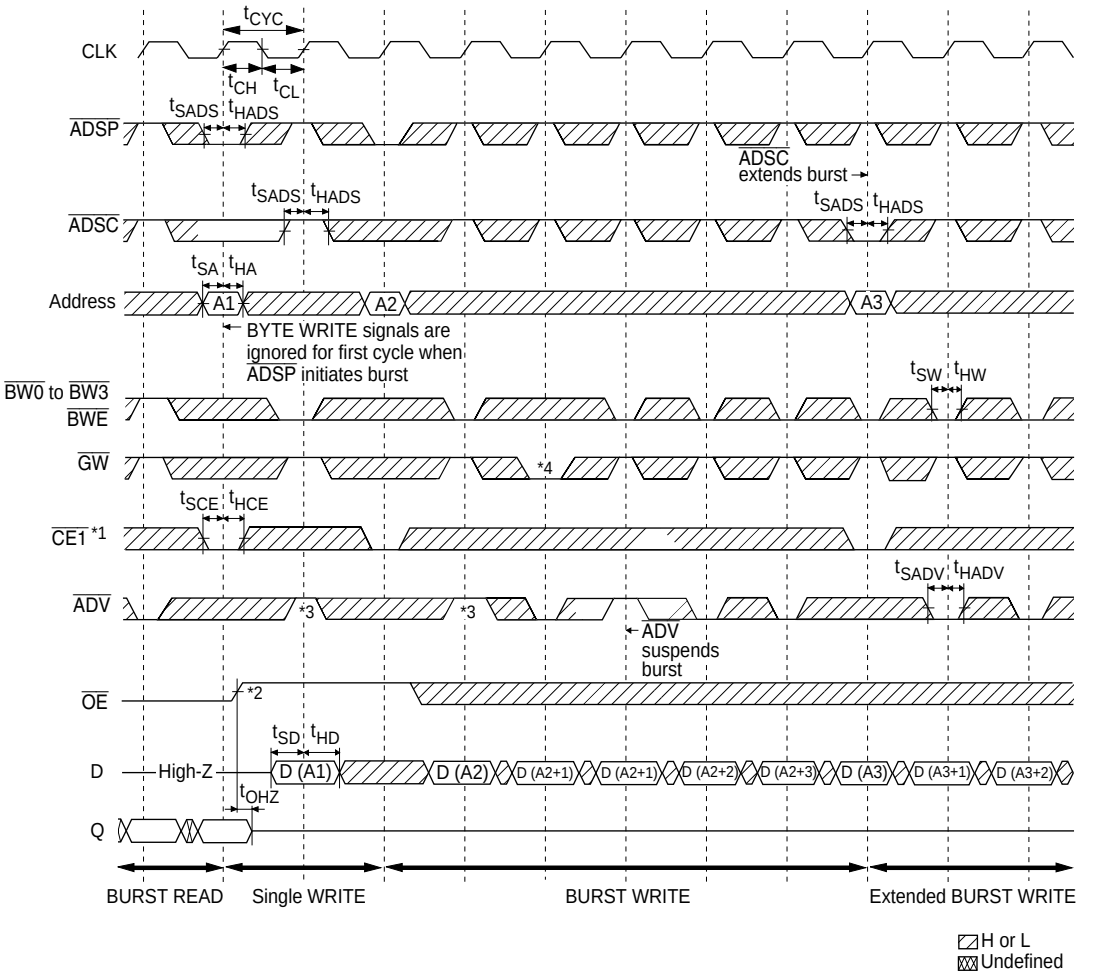
Timing Waveforms

Example of Read Timing



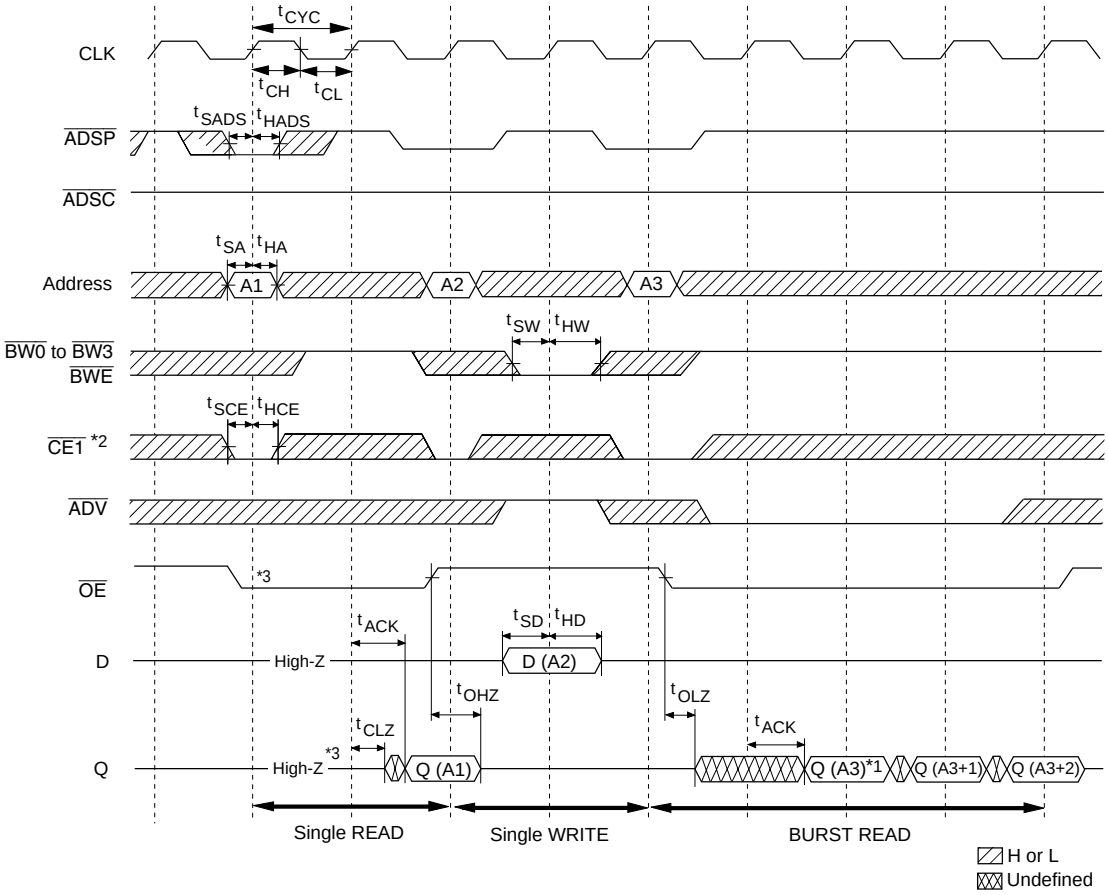
Notes: 1. Q (A2) refers to output from address A2. Q (A2 + 1) refers to output from next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Outputs are disabled within one clock cycle after deselect.
4. ZZ is LOW

Example of Write Timing



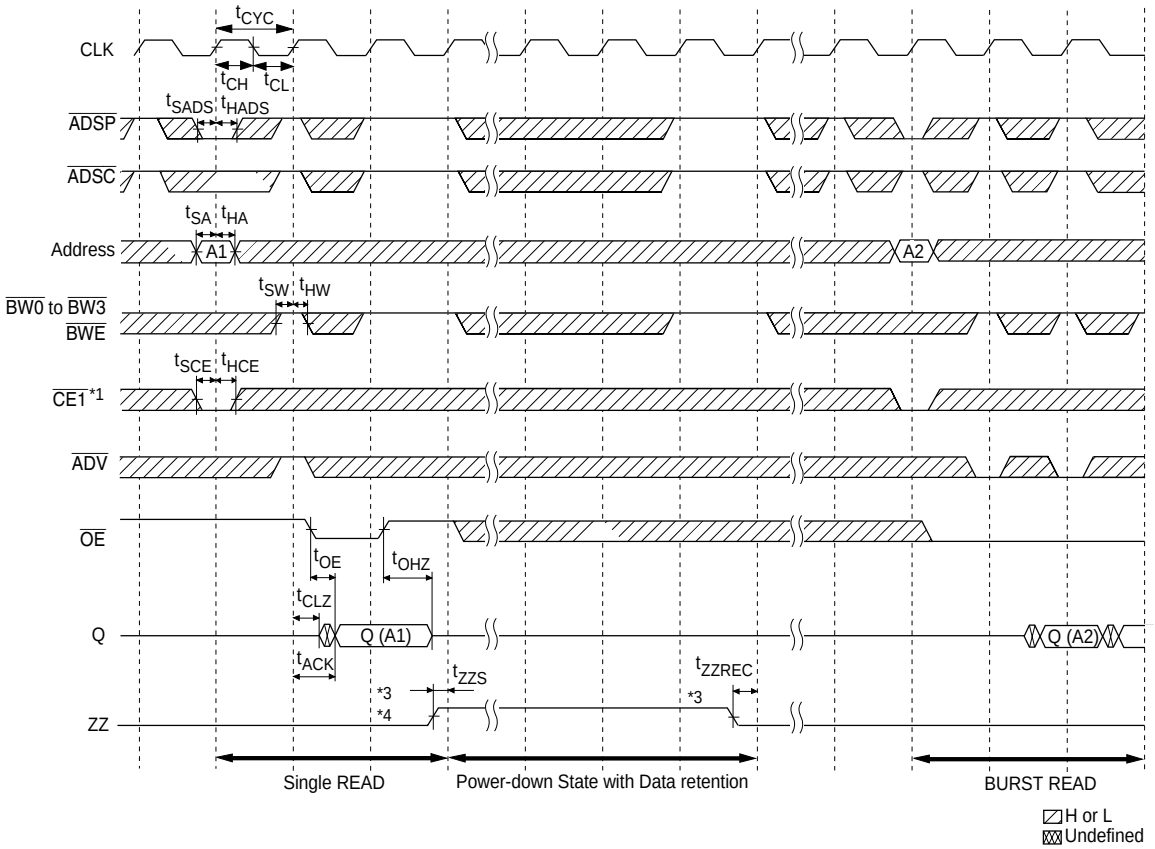
Notes: 1. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.
4. Full width WRITE can be initiated by $\overline{GW}$ is LOW or $\overline{GW}$ is HIGH and $\overline{BWE}$, $\overline{BW0}$ to $\overline{BW3}$ are LOW.
5. ZZ is LOW.

Example of Read/Write Timing



Notes: 1. Q (A3) refers to output from address A3. Q (A3 + 1) refers to output from next internal burst address following A3.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.
4. $\overline{GW}$ is HIGH. ZZ is LOW.

Example of Power-down State Timing



Notes: 1. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
2. $\overline{GW}$ is HIGH.
3. During the cycle when transition of ZZ from high to low or from low to high occurs, $\overline{ADSP}$, $\overline{ADSC}$, $\overline{BWE}$, $\overline{GW}$ and $\overline{BWi}$ must be high at its rising edge of CLK.
4. Data-output is not guaranteed during the cycle when transition of ZZ from low to high occurs.

Detailed Pin Description

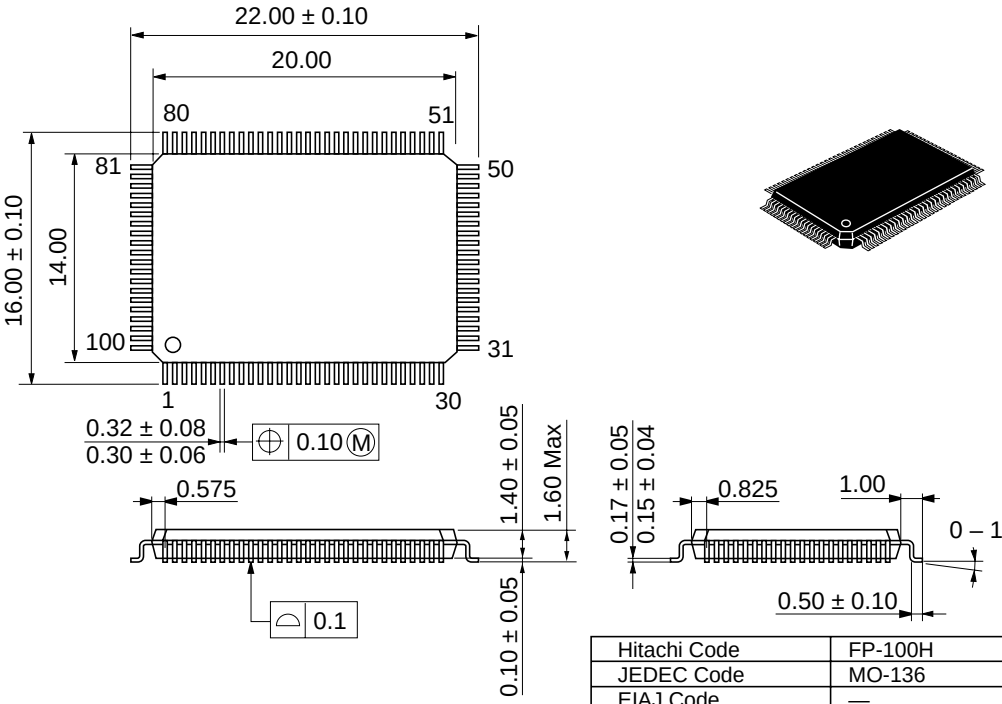
LQFP pin number(s)	Symbol	Type	Description
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0 to A14	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW0}$, $\overline{BW1}$ $\overline{BW2}$, $\overline{BW3}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0 to DQ7. $\overline{BW1}$ controls DQ8 to DQ15. $\overline{BW2}$ controls DQ16 to DQ23. $\overline{BW3}$ controls DQ24 to DQ31. Data I/O are tri-stated if any of these four inputs are LOW.
88	$\overline{GW}$	Input	Synchronous Global Write: This active LOW input allows a full 32 bit Write to occur independent of the $\overline{BWE}$ and $\overline{BWi}$ lines and must meet the setup and hold times around the rising edge of CLK. System must connect pin to V_{DD} when not used.
87	$\overline{BWE}$	Input	Synchronous Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK. System must connect pin to V_{SS} when not used.
89	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE1}$	Input	Synchronous Chip Enables: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is load.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input sampled only when a new external address is load. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait status to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a write cycle is desired (to ensure use of correct address).

Detailed Pin Description (cont)

LQFP pin number(s)	Symbol	Type	Description
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE1}$ is HIGH. Power-down state is entered if $\overline{CE2}$ is HIGH or CE2 is LOW.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enabled are inactive.
1, 14, 16, 30, 31, 38, 39, 42, 43,49, 50, 51, 64, 66, 80	NC	—	No Connect: These signals are internally not connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ0 to DQ31	Input/ Output	SRAM Data I/O: Byte 0 is DQ0 to DQ7; Byte 1 is DQ8 to DQ15; Byte 2 is DQ16 to DQ23; Byte 3 is DQ24 to DQ31. Input data must meet setup and hold times around the rising edge of CLK.
15, 41, 65, 91	V_{DD}	Supply	Power Supply: +3.3 V ±5 %
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply: +2.375V to V_{DD}
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND
64	ZZ	Input	Asynchronous Power down (Snooze):This active HIGH input enables SRAM to enter a Power down (Snooze) state with data retention. During Snooze state, data retention is guranteed. At this time, internal state of the SRAM must be initiated with $\overline{ADSP}$ or $\overline{ADSC}$ using a new external address. Must be connected to V_{SS} in systems that do not use ZZ feature.

Package Dimensions

HM62P1321FP Series (FP-100H) Unit: mm



Hitachi Code	FP-100H
JEDEC Code	MO-136
EIAJ Code	—
Weight	0.95 g

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