
HM62W4100H Series

1048576-word \times 4-bit High Speed CMOS Static RAM

HITACHI

ADE-203-774 (Z)
Preliminary
Rev. 0.0
Apr. 28, 1997

Description

The HM62W4100H is an asynchronous high speed static RAM organized as 1-Mword \times 4-bit. It has realized high speed access time (10/12/15 ns) with employing 0.35 μ m CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed and high density memory, such as cache and buffer memory in system. The HM62W4100H is packaged in 400-mil 32-pin SOJ for high density surface mounting.

Features

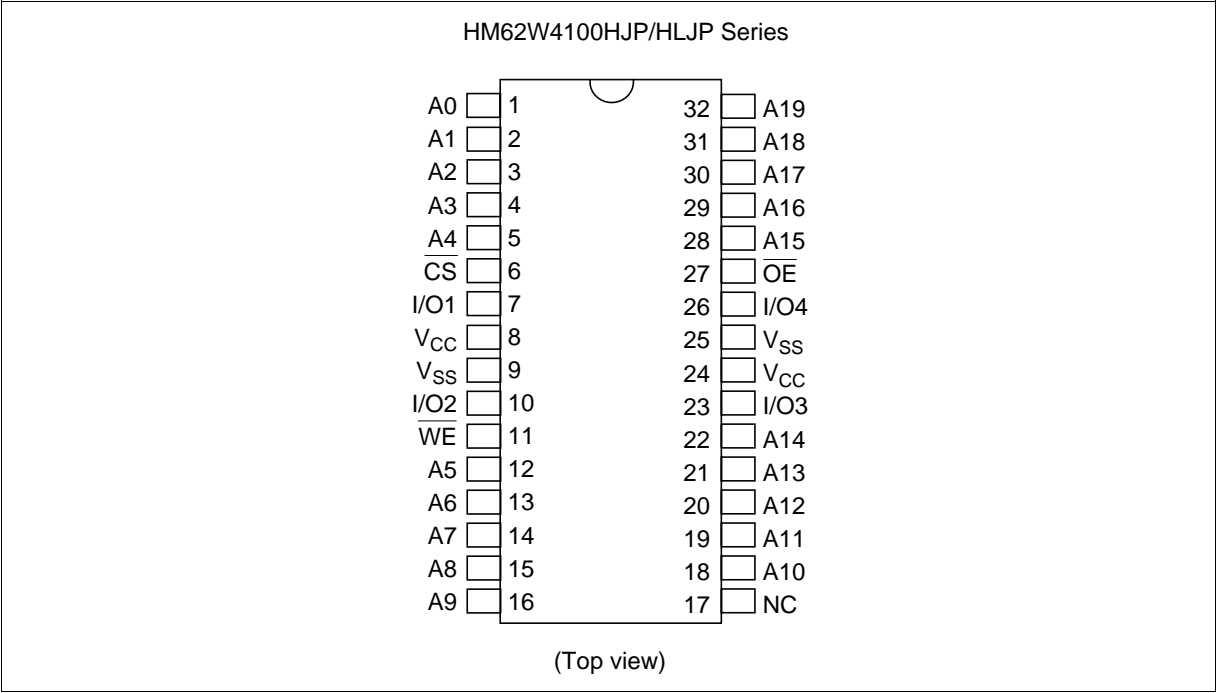
- Single supply : 3.3 V \pm 0.3 V
- Access time 10 ns/12 ns/15 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- 400-mil 32-pin SOJ package
- Center V_{CC} and V_{SS} type pinout

Ordering Information

Type No.	Access time	Package
HM62W4100HJP-10	10 ns	400-mil 32-pin plastic SOJ (CP-32DB)
HM62W4100HJP-12	12 ns	
HM62W4100HJP-15	15 ns	
HM62W4100HLJP-10	10 ns	
HM62W4100HLJP-12	12 ns	
HM62W4100HLJP-15	15 ns	

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

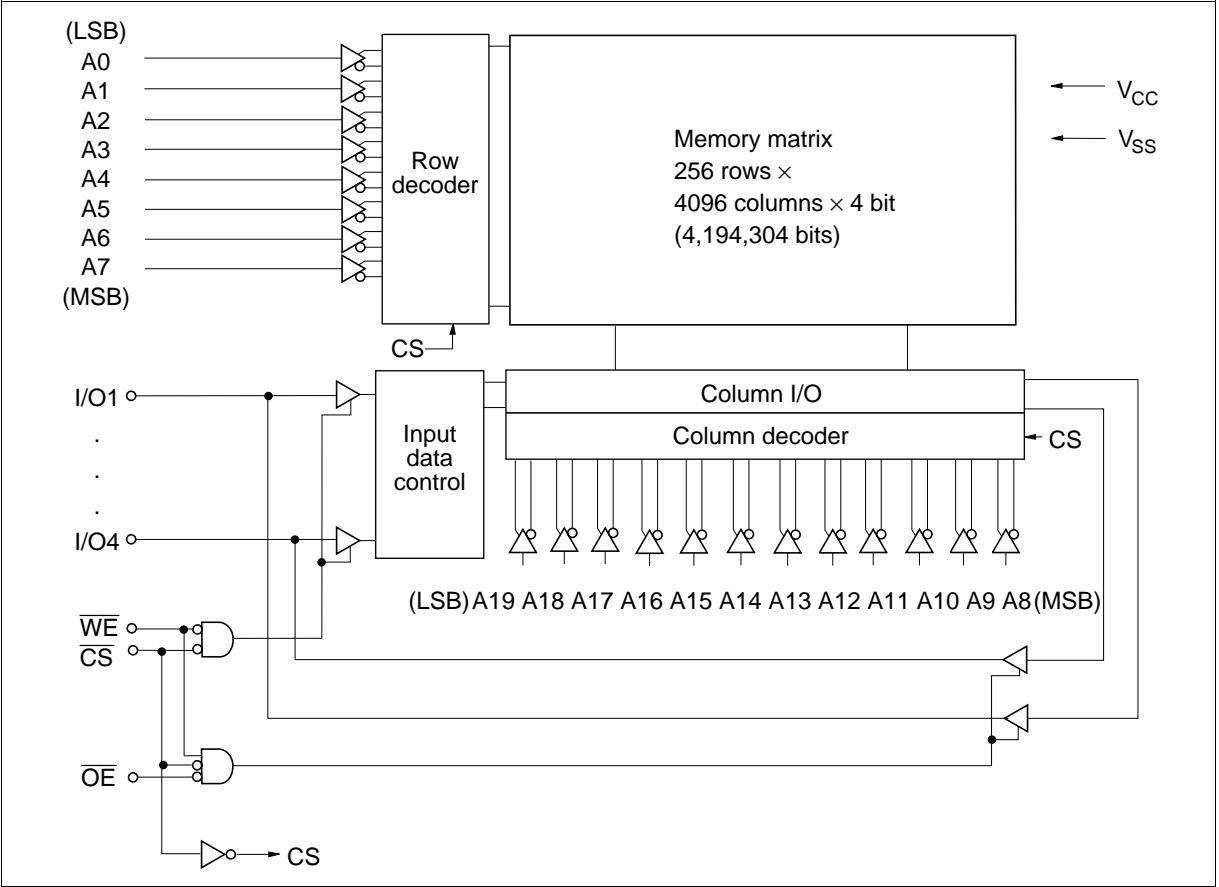
Pin Arrangement



Pin Description

Pin name	Function
A0 to A19	Address input
I/O1 to I/O4	Data input/output
\overline{CS}	Chip select
\overline{OE}	Output enable
\overline{WE}	Write enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Function Table

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} current	I/O	Ref. cycle
H	×	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	Output disable	I_{CC}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	-0.5*1 to $V_{CC}+0.5$	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to +85	°C

Notes: 1. V_T min = -2.5 V for pulse width (under shoot) \leq 10 ns

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}^{*2}	3.0	3.3	3.6	V
	V_{SS}^{*3}	0	0	0	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3*1	—	0.8	V

- Notes: 1. V_{IL} min = -2.0 V for pulse width (under shoot) \leq 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0V)

Parameter		Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current		I _{LI}	—	—	2	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current		I _{LO}	—	—	2	μA	V _{in} = V _{SS} to V _{CC}
Operation power supply current	10 ns cycle	I _{CC}	—	—	240	mA	$\overline{CS} = V_{IL}$, I _{out} = 0 mA Other inputs = V _{IH} /V _{IL}
	12 ns cycle	I _{CC}	—	—	200		
	15 ns cycle	I _{CC}	—	—	190		
Standby power supply current	10 ns cycle	I _{SB}	—	—	100	mA	$\overline{CS} = V_{IH}$, Other inputs = V _{IH} /V _{IL}
	12 ns cycle	I _{SB}	—	—	100		
	15 ns cycle	I _{SB}	—	—	100		
		I _{SB1}	—	—	10	mA	V _{CC} ≥ \overline{CS} ≥ V _{CC} - 0.2 V, (1) 0 V ≤ V _{in} ≤ 0.2 V or (2) V _{CC} ≥ V _{in} ≥ V _{CC} - 0.2 V
			—* ²	—* ²	0.5* ²		
Output voltage		V _{OL}	—	—	0.4	V	I _{OL} = 8 mA
		V _{OH}	2.4	—	—	V	I _{OH} = -4 mA

Notes: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹		C _{in}	—	—	6	pF	V _{in} = 0 V
Input/output capacitance* ¹		C _{I/O}	—	—	8	pF	V _{I/O} = 0 V

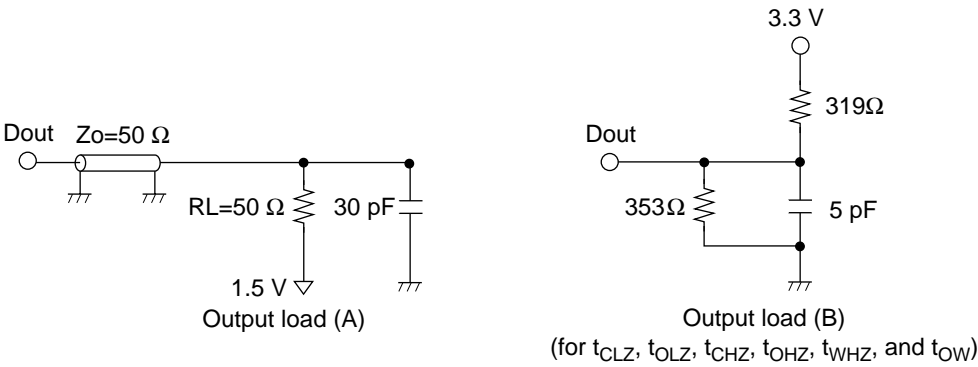
Note: 1. This parameter is sampled and not 100% tested.

HM62W4100H Series

AC Characteristics (Ta = 0 to +70°C, VCC = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5V
- Output load: See figures (Including scope and jig)



Read Cycle

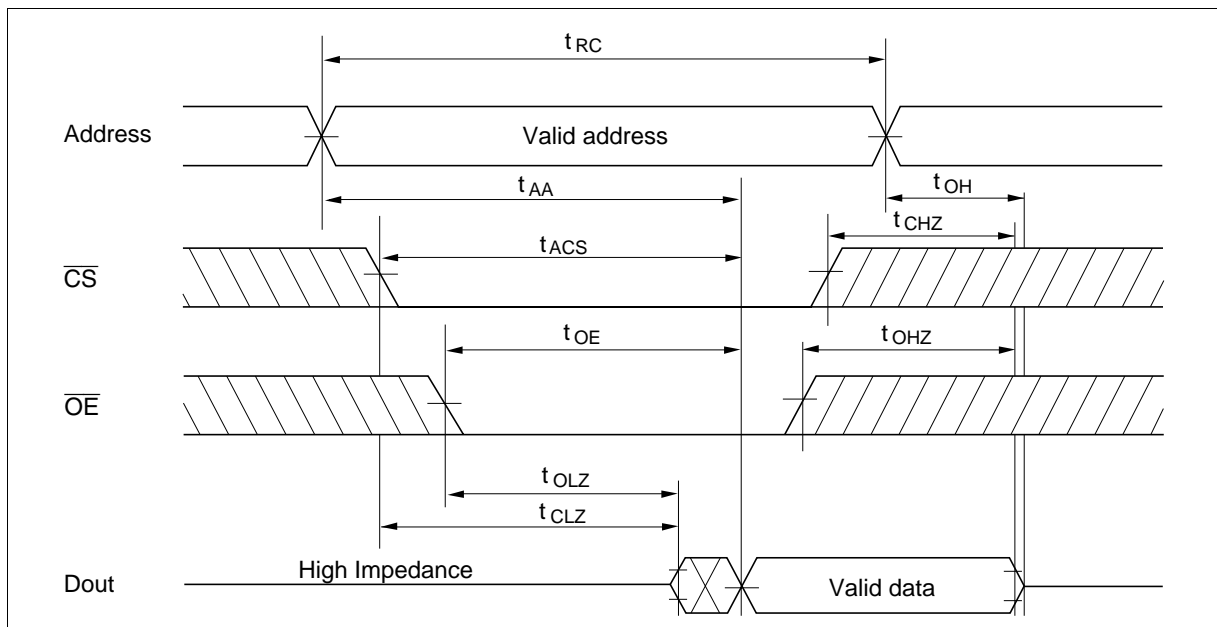
HM62W4100H									
Parameter	Symbol	-10		-12		-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	—	12	—	15	—	ns	
Address access time	t_{AA}	—	10	—	12	—	15	ns	
Chip select access time	t_{ACS}	—	10	—	12	—	15	ns	
Output enable to output valid	t_{OE}	—	5	—	6	—	8	ns	
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	5	—	6	—	8	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	—	6	—	8	ns	1

Write Cycle

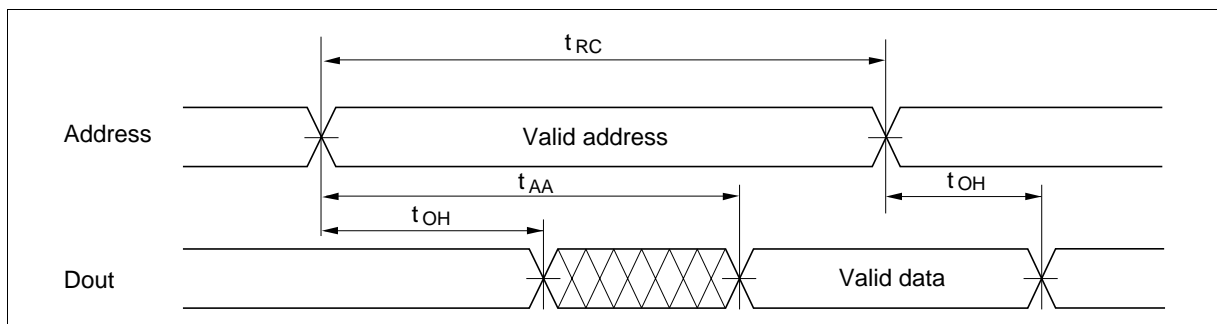
		HM62W4100H							
		-10		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	10	—	12	—	15	—	ns	
Address valid to end of write	t _{AW}	6	—	8	—	10	—	ns	
Chip select to end of write	t _{CW}	6	—	8	—	10	—	ns	9
Write pulse width	t _{WP}	6	—	8	—	10	—	ns	8
Address setup time	t _{AS}	0	—	0	—	0	—	ns	6
Write recovery time	t _{WR}	0	—	0	—	0	—	ns	7
Data to write time overlap	t _{DW}	5	—	6	—	8	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns	
Write disable to output in low-Z	t _{OW}	3	—	3	—	3	—	ns	1
Output disable to output in high-Z	t _{OHZ}	—	5	—	6	—	8	ns	1
Write enable to output in high-Z	t _{WHZ}	—	5	—	6	—	8	ns	1

- Note:
1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
 2. Address should be valid prior to or coincident with \overline{CS} transition low.
 3. \overline{WE} and/or \overline{CS} must be high during address transition time.
 4. If \overline{CS} and \overline{OE} are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
 5. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, output remains a high impedance state.
 6. t_{AS} is measured from the latest address transition to the later of \overline{CS} or \overline{WE} going low.
 7. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the first address transition.
 8. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low. A write ends at the earliest transition among \overline{CS} going high and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 9. t_{CW} is measured from the later of \overline{CS} going low to the the end of write.

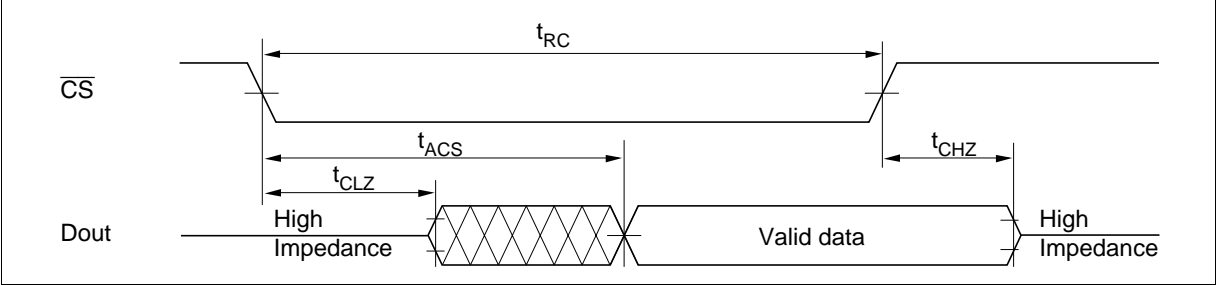
Read Timing Waveform (1) ($\overline{\text{WE}} = V_{\text{IH}}$)



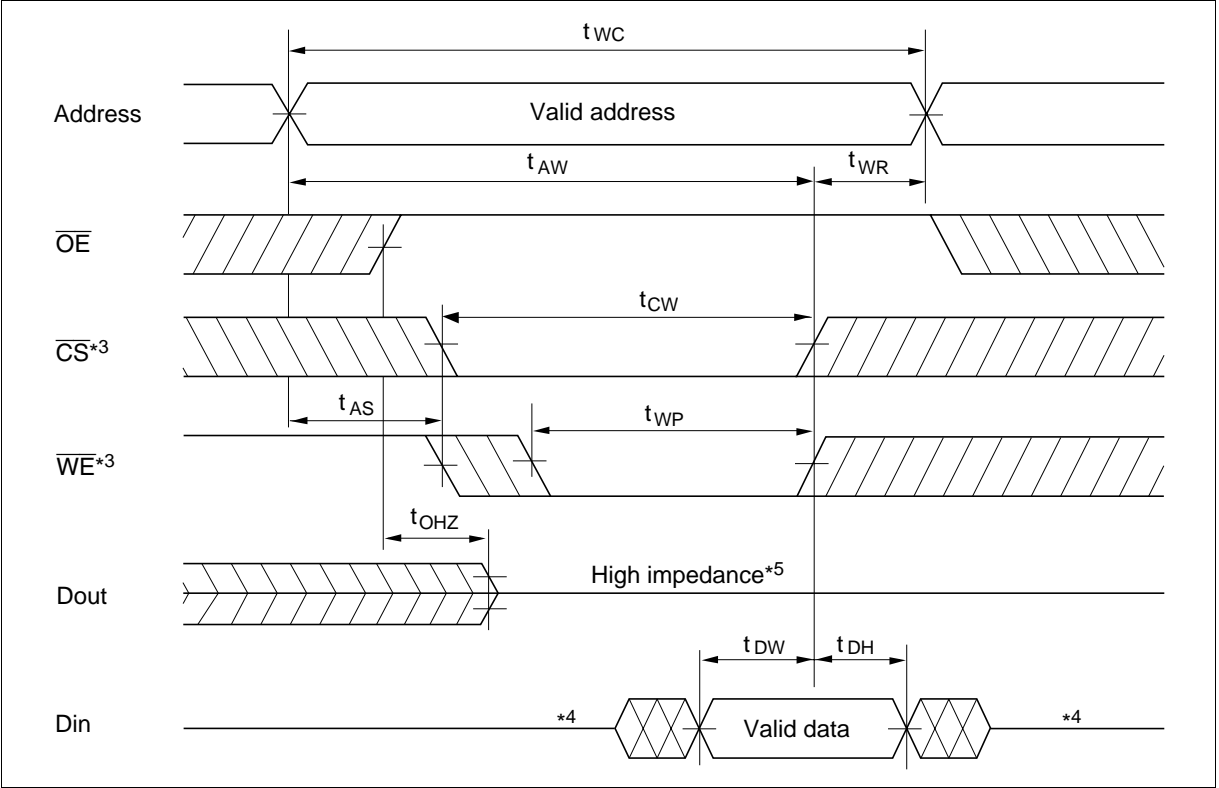
Read Timing Waveform (2) ($\overline{\text{WE}} = V_{\text{IH}}$, $\overline{\text{CS}} = V_{\text{IL}}$, $\overline{\text{OE}} = V_{\text{IL}}$)



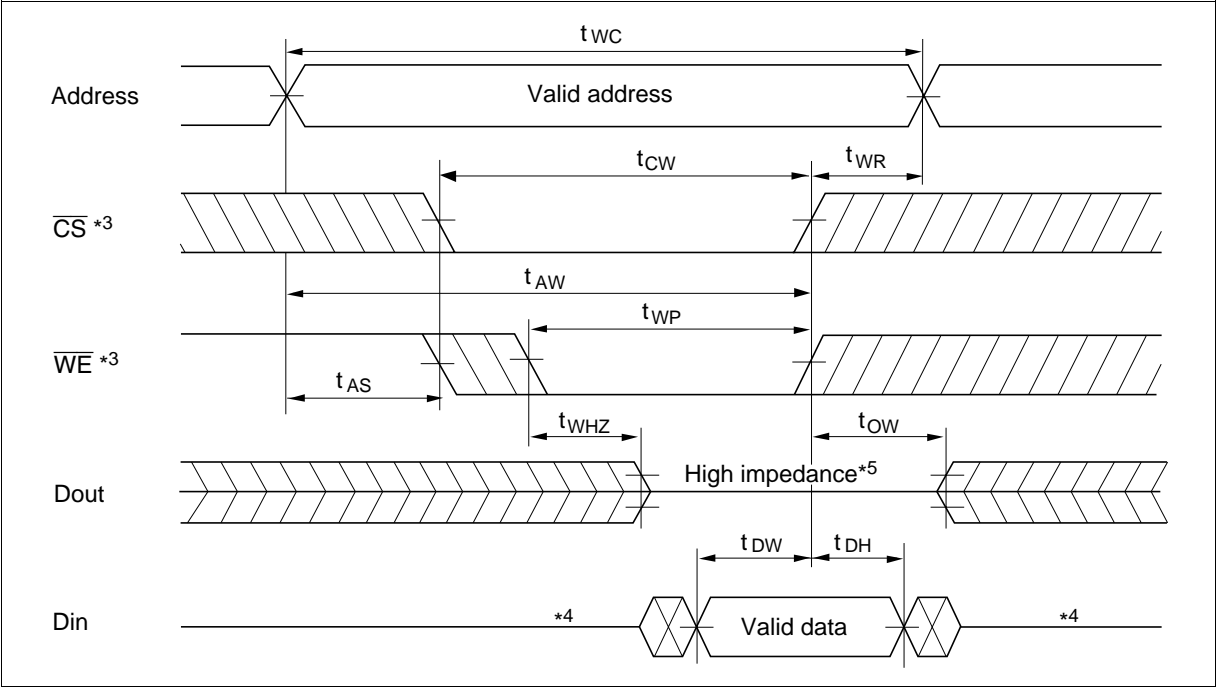
Read Timing Waveform (3) ($\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$)*2



Write Timing Waveform (1) (\overline{WE} Controlled)



Write Timing Waveform (2) (\overline{CS} Controlled)



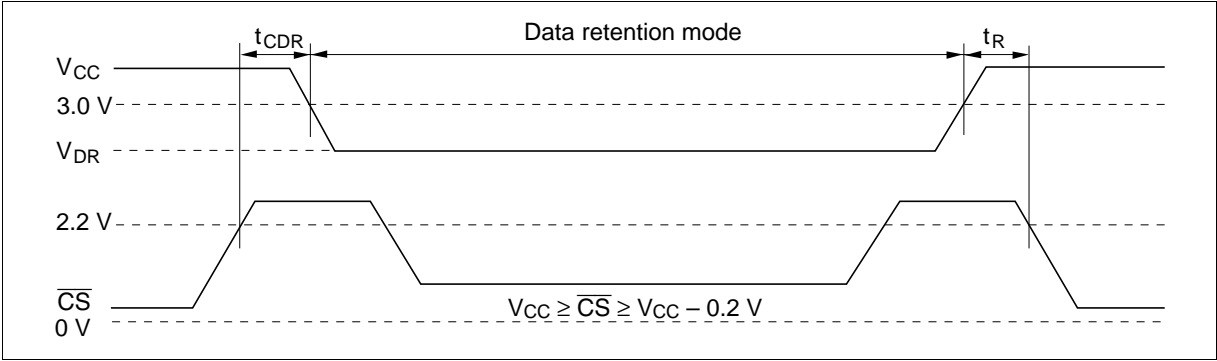
Low V_{CC} Data Retention Characteristics (Ta = 0 to 70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
V _{CC} for data retention	V _{DR}	2.0	—	—	V	V _{CC} ≥ \overline{CS} ≥ V _{CC} - 0.2 V (1) 0 V ≤ Vin ≤ 0.2 V or (2) V _{CC} ≥ Vin ≥ V _{CC} - 0.2 V
Data retention current	I _{CCDR}	—	2	300	μA	V _{CC} = 3 V, V _{CC} ≥ \overline{CS} ≥ V _{CC} - 0.2 V (1) 0 V ≤ Vin ≤ 0.2 V or (2) V _{CC} ≥ Vin ≥ V _{CC} - 0.2 V
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	5	—	—	ms	

Note: 1. Typical values are at V_{CC} = 3.0 V, Ta = 25°C, and not guaranteed.

Low V_{CC} Data Retention Timing Waveform

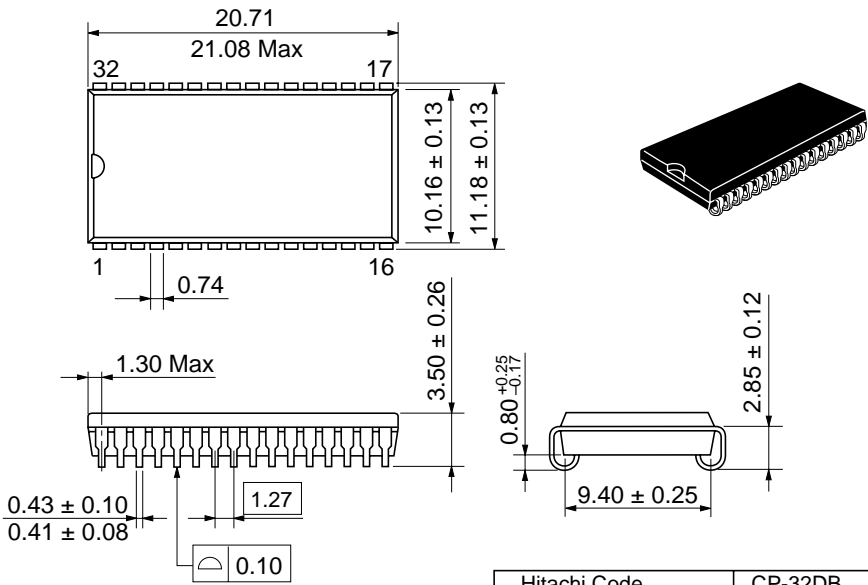


HM62W4100H Series

Package Dimensions

HM62W4100HJP/HLJP Series (CP-32DB)

Unit: mm



Hitachi Code	CP-32DB
JEDEC Code	MO-061-AB
EIAJ Code	SC-638
Weight	1.2 g

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HM62W4100H Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Apr. 28, 1997	Initial issue		
