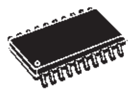
TS612

DUAL WIDE BAND OPERATIONAL AMPLIFIER WITH HIGH OUTPUT CURRENT

- LOW NOISE : **$3nV/\sqrt{Hz}$, $1.2pA/\sqrt{Hz}$**
- HIGH OUTPUT CURRENT : **200mA min.**
- VERY LOW HARMONIC AND INTERMODULATION DISTORTION
- HIGH SLEW RATE : **40V/µs**
- SPECIFIED FOR 25Ω LOAD
- POWER DOWN FUNCTION

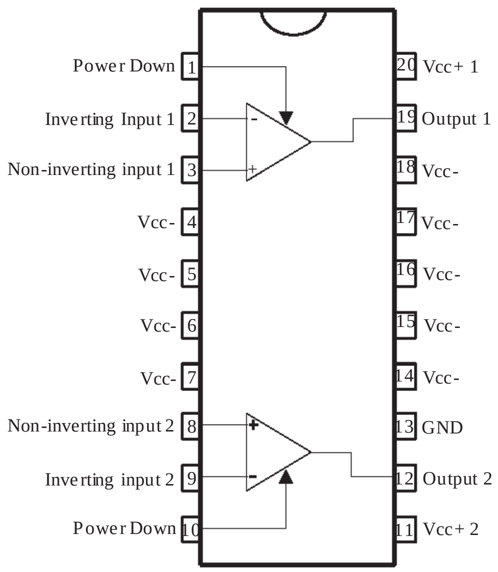


D
SO20
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package D
TS612ID	-40, +85°C	•

PIN CONNECTIONS (top view)



DESCRIPTION

The TS612 is a dual operational amplifier featuring a high output current (200mA min.), large gain-bandwidth product (130MHz) and capable of driving a 25Ω load with a 160mA output current at ±6V power supply.
This device is particularly intended for applications where multiple carriers must be amplified simultaneously with very low intermodulation products.
The TS612 is housed in a SO20 batwing package for a very low thermal resistance.
The TS612 is fitted out with Power Down function in order to decrease the consumption.

APPLICATIONS

UPSTREAM line driver for Assymetric Digital Subscriber Line (ADSL) (NT).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage - note 1	±7	V
V_{id}	Differential Input Voltage - note 2	±2	V
V_i	Input Voltage - note 3	±6	V
T_{oper}	Operating Free Air Temperature Range TS612ID	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thjc}	Thermal Resistance Junction to Case	25	°C/W
	Output Short Circuit Duration	see note 4	

Note :
1. All voltages values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC} +0.3V.
4. An output current limitation protects the circuit from transient currents. Short-circuits can cause excessive heating. Destructive dissipation can result from short circuit on amplifiers.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±2.5 to ±6	V
V_{icm}	Common Mode Input Voltage	(V_{CC})+2 to $(V_{CC}+)$-1	V

V_{CC}+1 and V_{CC}+2 are both V_{CC}+ supply pins and they are internally connected together.
V_{CC}^- (pin18) is not internally connected with the other V_{CC}^- pins and must be externally connected to V_{CC}^-.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 6V$, $T_{amb} = 25^oC$ (unless otherwise specified)

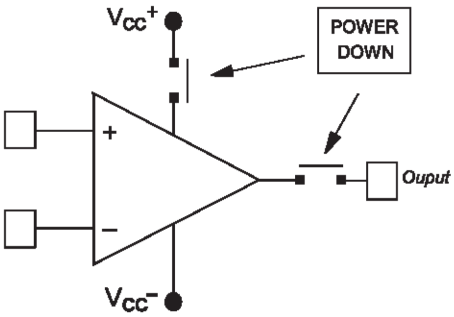
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage	$T_{amb} = 25^oC$ $T_{min.} < T_{amb} < T_{max.}$	-6	-1	6 10	mV
ΔV_{io}	Differential Input Offset Voltage	$T_{amb} = 25^oC$ $T_{min.} < T_{amb} < T_{max.}$			6	mV
I_{io}	Input Offset Current	$T_{amb} = 25^oC$ $T_{min.} < T_{amb} < T_{max.}$		0.2	3 5	µA
I_{ib}	Input Bias Current	$T_{amb} = 25^oC$ $T_{min.} < T_{amb} < T_{max.}$		5	15 30	µA
I_{CC}	Total Supply Current per Operator	No load, $V_{out} = 0$		14		MA
V_{OH}	High Level Output Voltage R_L connected to GND	Iout = 160mA R_L =25Ω	4	4.5		V
V_{OL}	Low Level Output Voltage R_L connected to GND	Iout = 160mA R_L =25Ω		-4.5	-4	V
A_{VD}	Large Signal Voltage Gain	Vout = 7Vpeak R_L = 25Ω $T_{amb} = 25^oC$ $T_{min.} < T_{amb} < T_{max.}$	 6500 5000	 11000		V/V
GBP	Gain Bandwidth Product	A_{VCL} = +11, f = 20MHz, R_L = 100Ω	80	130		MHz
CMR	Common Mode Rejection Ratio	V_{ic} = 2V to 2V $T_{min.} < T_{amb} < T_{max.}$	90 70	108		dB
SVR	Supply Voltage Rejection Ratio	V_{ic} = ±6V to ±4V $T_{min.} < T_{amb} < T_{max.}$	70 50	88		dB
I_{os}	Output Short Circuit Current			±320		mA
I_{sink}	Output Sink Current	V_{ic} = ±6V, $T_{amb} = 25^oC$ $T_{min.} < T_{amb} < T_{max.}$	+200 +180			mA
I_{source}	Output Source Current	V_{ic} = ±6V, $T_{amb} = 25^oC$ $T_{min.} < T_{amb} < T_{max.}$			-200 -180	mA
SR	Slew Rate	A_{VCL} = +7, R_L = 50Ω	23	40		V/µs
ΦM14	Phase Margine at A_{VCL} = 14dB	R_L = 25Ω//15pF		60		deg
ΦM6	Phase Margine at A_{VCL} = 6dB	RL = 25Ω//15pF		40		deg
en	Equivalent Input Noise Voltage	f = 100kHz		3		$nV/\sqrt{Hz}$
in	Equivalent Input Noise Current	f = 100kHz		1.2		$pA/\sqrt{Hz}$
THD	Total Harmonic Distorsion	V_{out} = 4Vpp, f = 100kHz A_{VCL} = -10 R_L = 25Ω//15pF		-69		dB
HD2	2nd Harmonic Distorsion	V_{out} = 4Vpp, f = 100kHz A_{VCL} = -10 R_L = 25Ω//15pF		-70		dBc
HD3	3rd Harmonic Distorsion	V_{out} = 4Vpp, f = 100kHz A_{VCL} = -10 R_L = 25Ω//15pF		-80		dBc
IM2	2nd Order Intermodulation Product	F1 = 80kHz, F2 = 70kHz Load = 25Ω//15pF V_{out} = 8Vpp, A_{VCL} = -10		-77		dBc
IM3	3rd Order Intermodulation Product	F1 = 80kHz, F2 = 70kHz Load = 25Ω//15pF V_{out} = 8Vpp, A_{VCL} = -10		-77		dBc
HD2	2nd Harmonic Distorsion	V_{out} = 4Vpp, f = 1MHz A_{VCL} = +2 R_L = 25Ω//15pF		-74		dBc
HD3	3rd Harmonic Distorsion	V_{out} = 4Vpp, f = 1MHz A_{VCL} = +2 R_L = 25Ω//15pF		-79		dBc

POWER DOWN MODE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{pdw}	Pin 1/10 Threshold Voltage for Power Down Mode Low level High level	 2	 0 3.3	 0.8	V
$I_{CC\ pdw}$	Supply Consumption per Operator			75	µA
R_{pdw}	Power Down Mode Output Resistance		1.4		mΩ
C_{pdw}	Power Down Mode Output Capacitance		33		pF

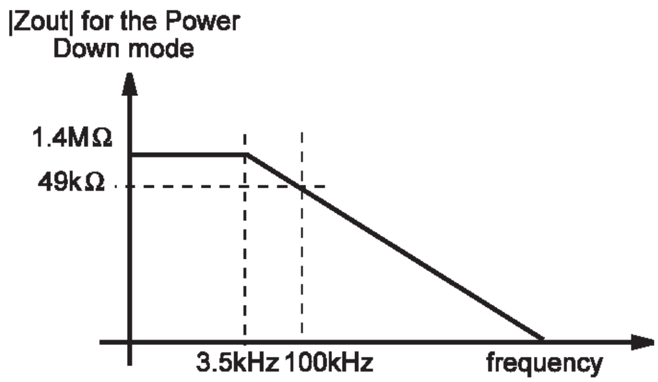
LOGIC INPUT		STATUS	
Power Down 1	**Power Down 2**	**Op-Amp 1**	**Op-Amp 2**
0	0	Enable	Enable
0	1	Enable	Power Down
1	0	Power Down	Enable
1	1	Power Down	Power Down

POWER MODE POSITION



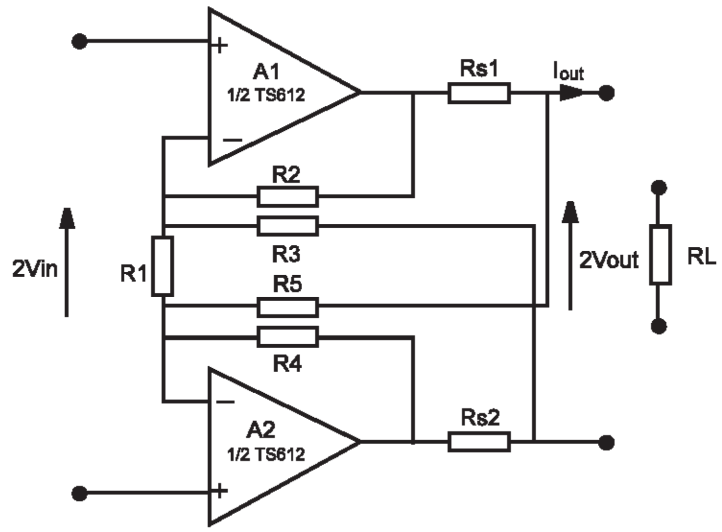
POWER DOWN MODE OUTPUT IMPEDANCE

For the Power-Down mode the driver output is on ”high impedance” state. It is really the case for the static mode.
For the dynamic mode the impedance decreases due to a capacitive effect of the collector-substrat and base-collector junction, then the impedance behaviour is capacitive and resistive (as shown on the following diagram) with R_{out} = 1.4MΩ and C_{out} = 33pF.

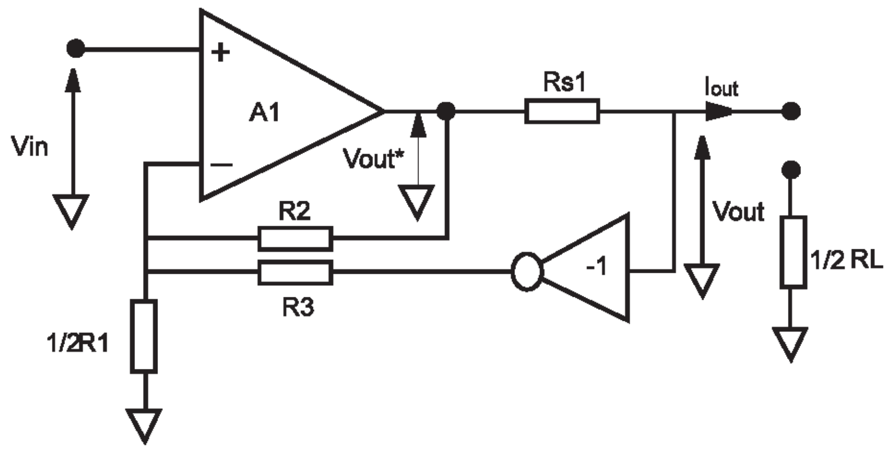


TYPICAL APPLICATION

Differential Line Driver with Active Impedance Matching



Equivalent circuit for one line



$V_{out} = (G.V_{in}) - (R_{out}.I_{out})$

with $R_{out} = R_s 1/(1\text{-}R2/3)$

$G = (1+2R2/R1+R2/R3)/(1-R2/R3)$ the gain for the unloaded device

$GL = G/2$

the gain for the loaded device

The aim of the active impedance matching :

By using a classical impedance matching (or passive impedance matching), a $V_{out}{}^{*}=2V_{out}$ output line amplitude. With the active impedance matching it is possible to hold a V_s line amplitude with a $V_{out}{}^{*}$ smaller than $2V_{out}$.

The advantage of this concept is to have a larger line amplitude without saturation of the output amplifier while keeping a good impedance matching.

Components calculation :

$R_{out} = {}_{1/2}RL$

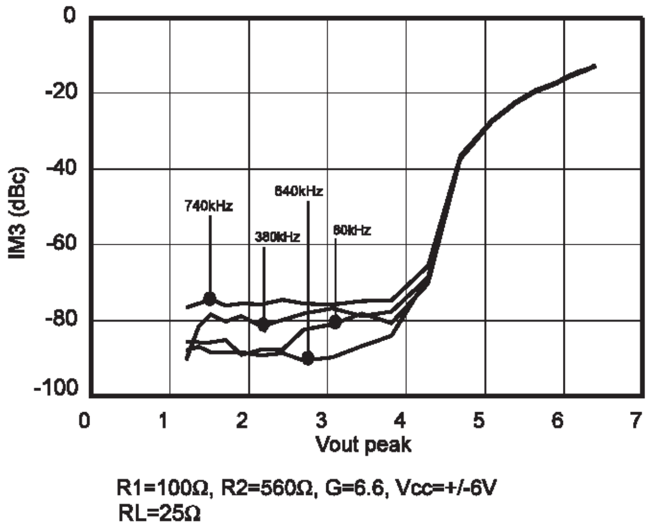
$G = 2GL$ with GL and $((V_{out}{}^{*}max-V_{out}max)/V_{out}max)$ fixed by the user

TS612 INTERMODULATION DISTORTION

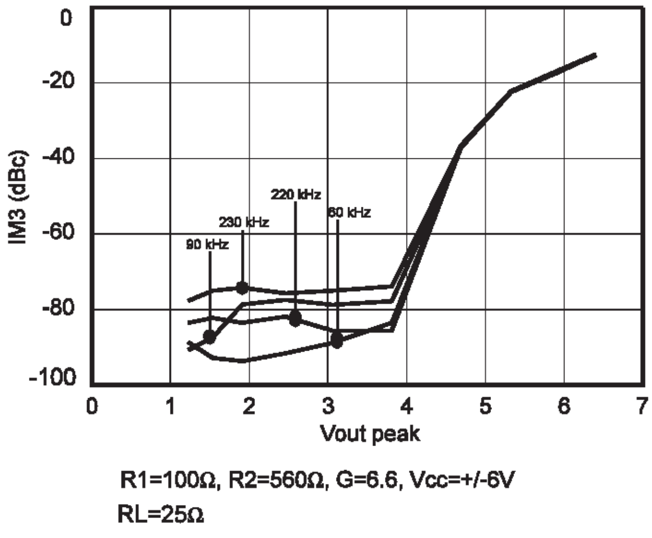
The curves shown below are the measurements results of a single operator wired as an adder with a gain of 20dB.
The operational amplifier is supplied by a symmetric ±6V and is loaded with 25Ω.
Two synthesizers (Rhode & Schwartz SME) generate two frequencies (tones) (70 & 80kHz ; 180 & 280kHz).

An HP3585 spectrum analyzer measures the spurious level at different frequencies.
The curves are traced for different output levels (the value in the X ax is the value of each tone).
The output levels of the two tones are the same.
The generators and spectrum analyzer are phase locked to enhance measurement precision.

THIRD ORDER INTERMODULATION
F1 = 180kHz ; F2 = 280kHz

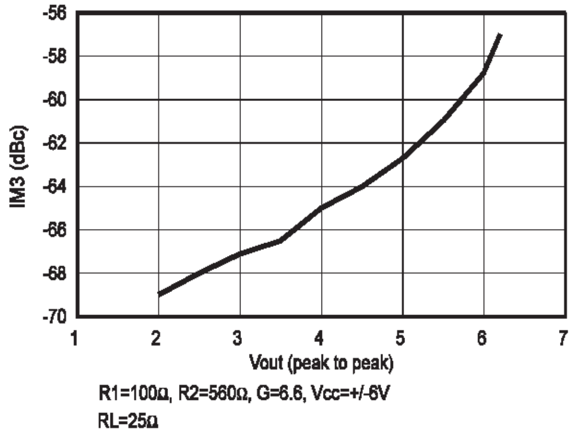


THIRD ORDER INTERMODULATION
F1 = 70kHz ; F2 = 80kHz



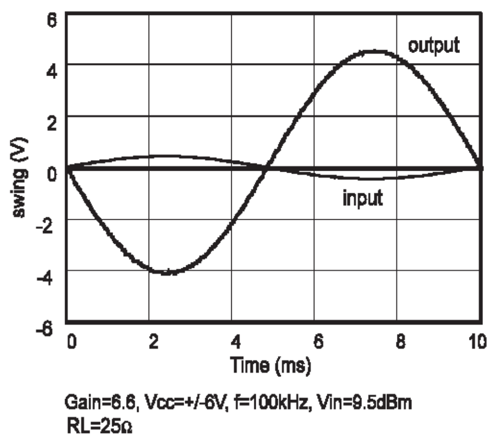
SECOND ORDER INTERMODULATION

F1 = 180kHz ; F2 = 280kHz, spurious measurement @ 100kHz

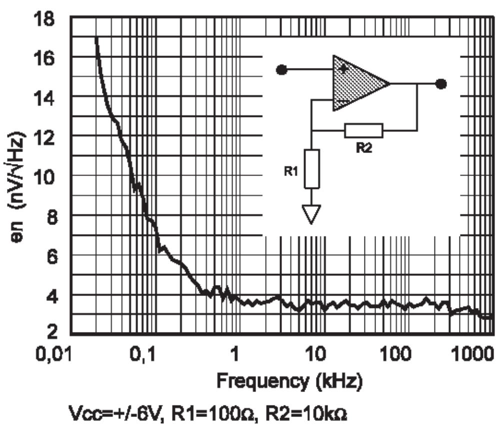


MAXIMUM OUTPUT SWING

The TS612 drives a 25Ω load @ 100kHz and is supplied with ±6V

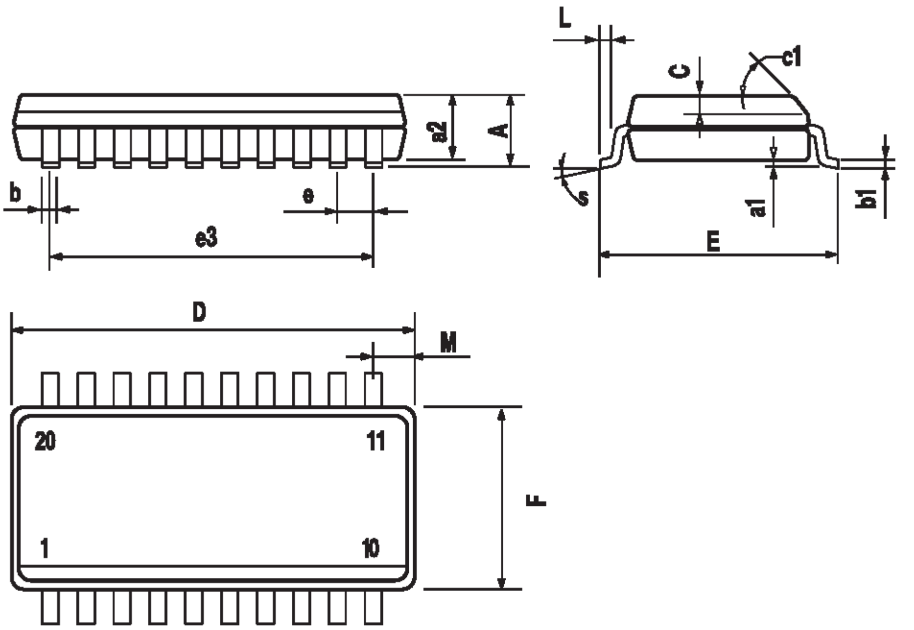


INPUT EQUIVALENT NOISE



PACKAGE MECHANICAL DATA

20 PINS - PLASTIC MICROPACKAGE (SO)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45^{o} (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8^{o} (Max.)					

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a trademark of STMicroelectronics

© 1999 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco
The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

© http://www.st.com