

DATA SHEET

74HC3G06; 74HCT3G06 Inverter with open-drain outputs

Product specification

2003 May 15

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Balanced propagation delays
- Very small 8 pins package.

DESCRIPTION

The 74HC3G06/74HCT3G06 is a high-speed Si-gate CMOS device. Specified in compliance with JEDEC standard no. 7A.

The 74HC3G06/74HCT3G06 provides three inverting buffers.

The outputs of the 74HC3G06; 74HCT3G06 devices are open drains and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH-level.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f \leq 6.0\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC3G	HCT3G	
t_{pZL}	propagation delay nA to nY	$C_L = 50\text{ pF}$; $V_{CC} = 4.5\text{ V}$	9	9	ns
t_{PLZ}	propagation delay nA to nY	$C_L = 50\text{ pF}$; $V_{CC} = 4.5\text{ V}$	11	12	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	4	4	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. For 74HC3G06 the condition is $V_I = \text{GND}$ to V_{CC} .

For 74HCT3G06 the condition is $V_I = \text{GND}$ to $V_{CC} - 1.5\text{ V}$.

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

FUNCTION TABLE

See note 1.

INPUT		OUTPUT	
nA		nY	
L		Z	
H		L	

Note

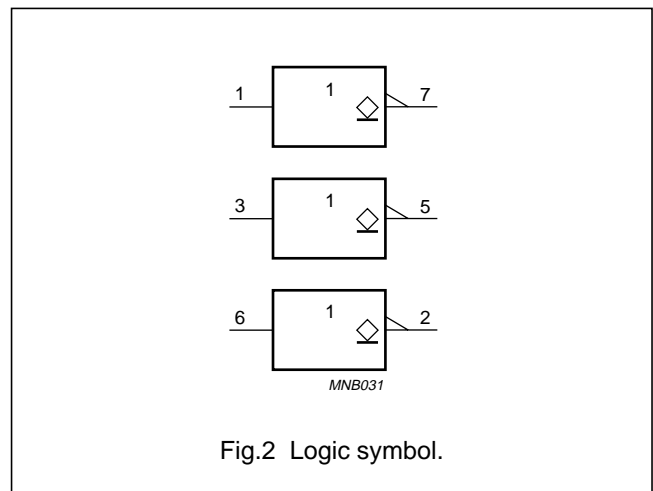
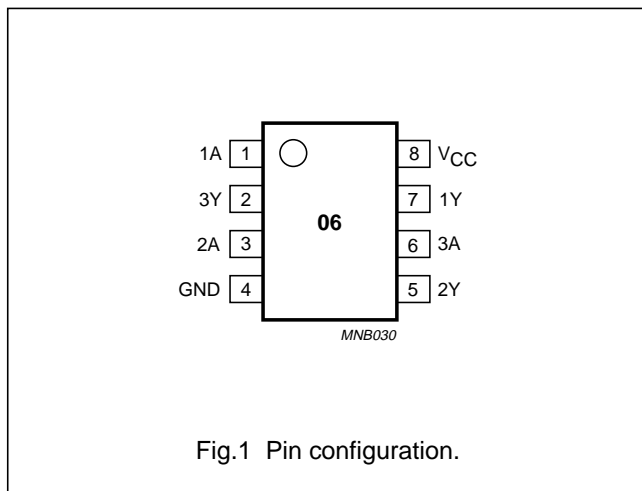
- 1. H = HIGH voltage level;
- L = LOW voltage level;
- Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC3G06DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	H06
74HCT3G06DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	T06

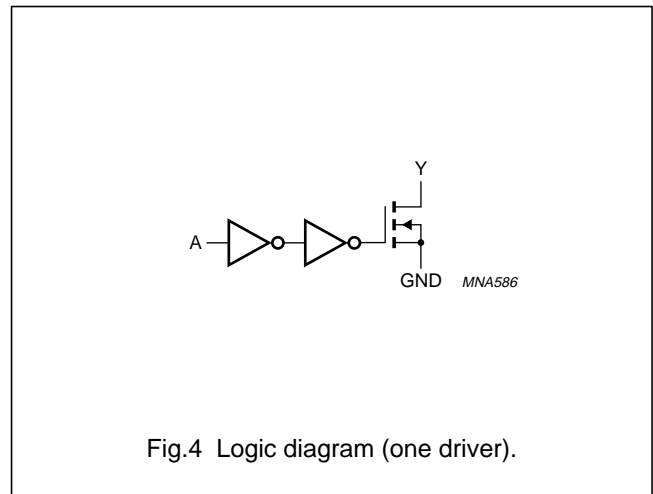
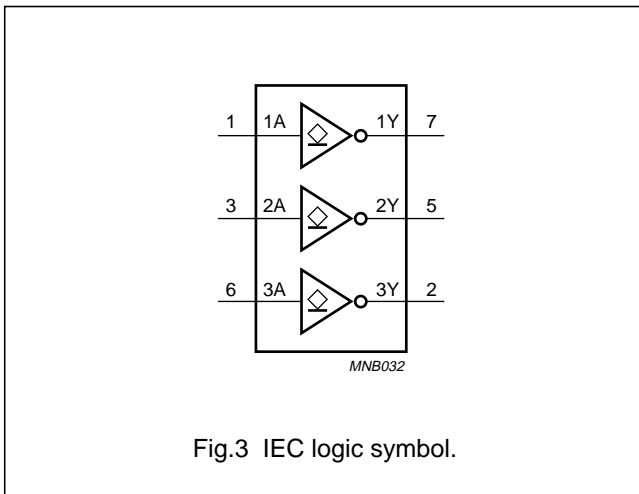
PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	3Y	data output
3	2A	data input
4	GND	ground (0 V)
5	2Y	data output
6	3A	data input
7	1Y	data output
8	V _{CC}	supply voltage



Inverter with open-drain outputs

74HC3G06; 74HCT3G06



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC3G06			74HCT3G06			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	–	6.0	0	–	5.5	V
V _O	output voltage		0	–	V _{CC}	0	–	V _{CC}	V
T _{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t _r , t _f	input rise and fall times	V _{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V _{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V _{CC} = 6.0 V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		–0.5	+7.0	V
I _{IK}	input diode current	V _I < –0.5 V or V _I > V _{CC} + 0.5 V; note 1	–	±20	mA
I _{OK}	output diode current	V _O < –0.5 V; note 1	–	–20	mA
V _O	output voltage	active mode; note 1	–0.5	V _{CC} + 0.5	V
		high-impedance mode; note 1	–0.5	7.0	V
I _O	output sink current	–0.5 V < V _O < 7.0 V; note 1	–	–25	mA
I _{CC} , I _{GND}	V _{CC} or GND current	note 1	–	50	mA
T _{stg}	storage temperature		–65	+150	°C
P _D	power dissipation	T _{amb} = –40 to +125 °C; note 2	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of P_D derates linearly with 8 mW/K.

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

DC CHARACTERISTICS

Type 74HC3G06

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
V _{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V _{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	2.0	–	0	0.1	V
		I _O = 20 µA	4.5	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.33	V
		I _O = 20 µA	6.0	–	0	0.1	V
		I _O = 5.2 mA	6.0	–	0.16	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±1.0	µA
I _{oz}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	–	–	±5.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	10	µA
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	2.0	–	–	0.1	V
		I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.4	V
		I _O = 20 µA	6.0	–	–	0.1	V
		I _O = 5.2 mA	6.0	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±1.0	µA
I _{oz}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	–	–	±10	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	20	µA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

Type 74HCT3G06

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 μA	4.5	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	μA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±5.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	10	μA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	–	375	μA
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 μA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	μA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	20	μA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	–	410	μA

Note1. All typical values are measured at T_{amb} = 25 °C.

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

AC CHARACTERISTICS

Type 74HC3G06

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
t _{PZL}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	22	95	ns
			4.5	–	9	18	ns
			6.0	–	8	16	ns
t _{PLZ}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	24	95	ns
			4.5	–	11	20	ns
			6.0	–	10	19	ns
t _{THL}	output transition time	see Figs 5 and 6	2.0	–	18	95	ns
			4.5	–	6	19	ns
			6.0	–	5	16	ns
T_{amb} = -40 to +125 °C							
t _{PZL}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	–	125	ns
			4.5	–	–	25	ns
			6.0	–	–	20	ns
t _{PLZ}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	–	125	ns
			4.5	–	–	27	ns
			6.0	–	–	23	ns
t _{THL}	output transition time	see Figs 5 and 6	2.0	–	–	125	ns
			4.5	–	–	25	ns
			6.0	–	–	20	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

Type 74HCT3G06

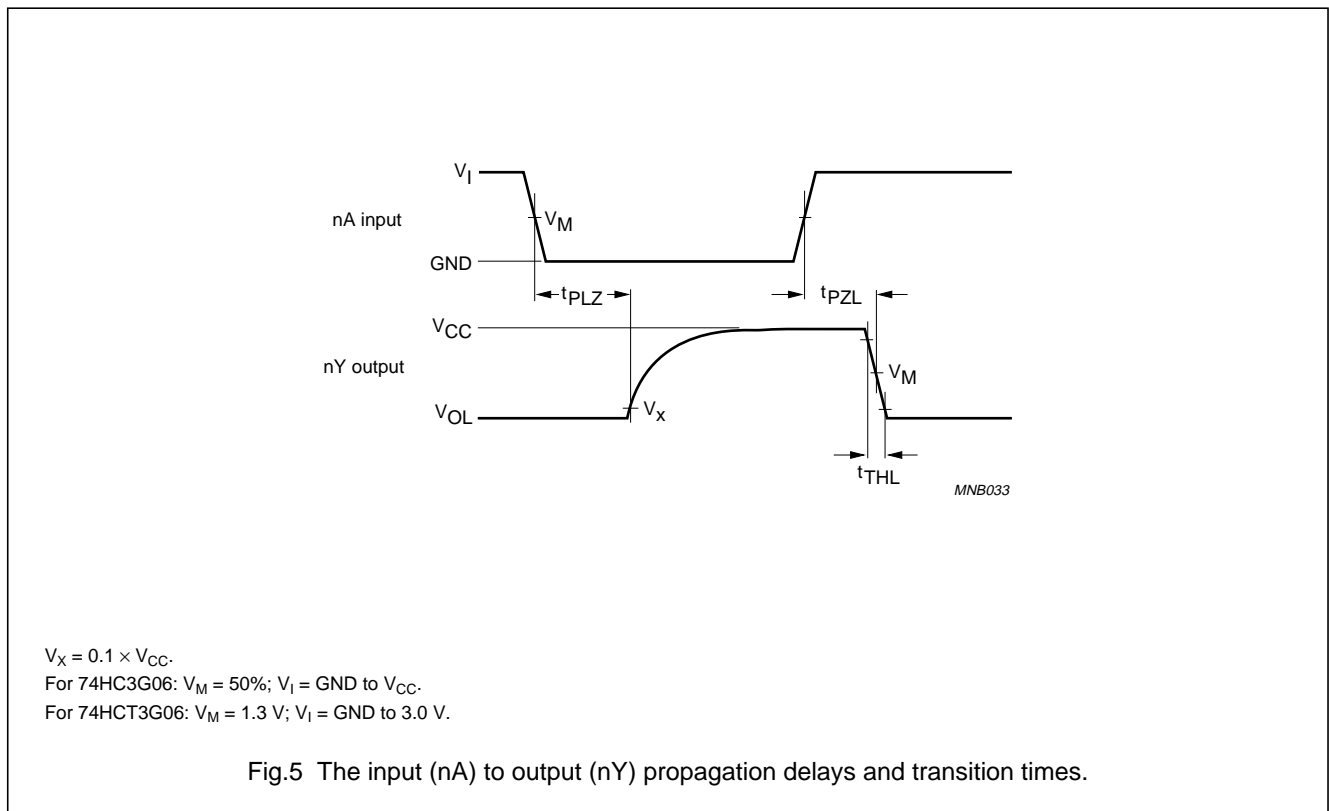
GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
t _{PZL}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	9	24	ns
t _{PLZ}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	12	27	ns
t _{THL}	output transition time	see Figs 5 and 6	2.0	–	6	19	ns
T_{amb} = -40 to +125 °C							
t _{PZL}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	–	29	ns
t _{PLZ}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	–	32	ns
t _{THL}	output transition time	see Figs 5 and 6	2.0	–	–	22	ns

Note

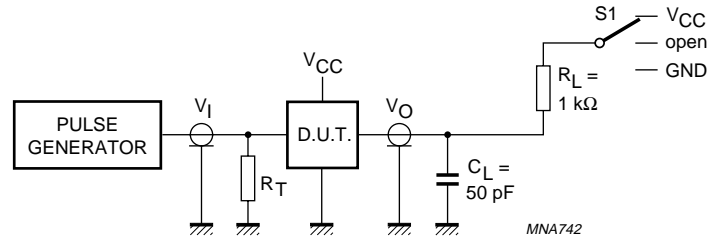
1. All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS



Inverter with open-drain outputs

74HC3G06; 74HCT3G06



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

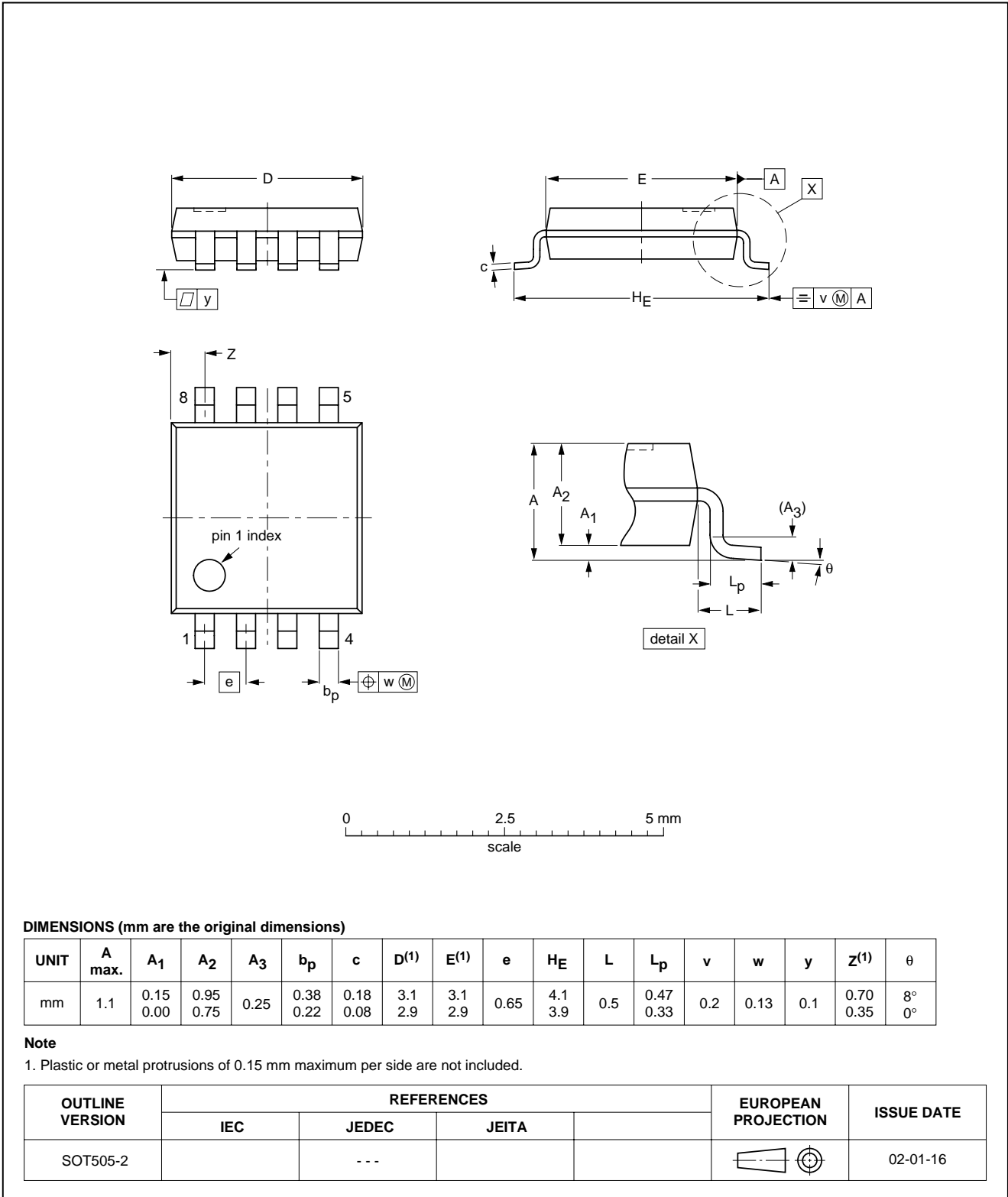
Fig.6 Load circuitry for switching times.

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

PACKAGE OUTLINE

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



Inverter with open-drain outputs

74HC3G06; 74HCT3G06

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all the BGA packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE ⁽¹⁾	SOLDERING METHOD	
	WAVE	REFLOW ⁽²⁾
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ⁽³⁾	suitable
PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ⁽⁶⁾	suitable

Notes

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

NOTES

Inverter with open-drain outputs

74HC3G06; 74HCT3G06

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

© Koninklijke Philips Electronics N.V. 2003

SCA75

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

613508/01/pp16

Date of release: 2003 May 15

Document order number: 9397 750 11187

Let's make things better.

**Philips
Semiconductors**



PHILIPS