

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT595

8-bit serial-in/serial or parallel-out  
shift register with output latches;  
3-state

Product specification  
Supersedes data of September 1993  
File under Integrated Circuits, IC06

1998 Jun 04

## 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

## 74HC/HCT595

### FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typ) shift out frequency
- Output capability:
  - parallel outputs; bus driver
  - serial output; standard
- I<sub>CC</sub> category: MSI.

### APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register.

### DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The “595” is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH<sub>CP</sub> input. The data in each register is transferred to the storage register on a positive-going transition of the ST<sub>CP</sub> input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D<sub>S</sub>) and a serial standard output (Q<sub>7</sub>') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns.

| SYMBOL                             | PARAMETER                                                   | CONDITIONS                                    | TYP. |     | UNIT |
|------------------------------------|-------------------------------------------------------------|-----------------------------------------------|------|-----|------|
|                                    |                                                             |                                               | HC   | HCT |      |
| t <sub>PHL</sub> /t <sub>PLH</sub> | propagation delay<br>SH <sub>CP</sub> to Q <sub>7</sub> '   | C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V | 16   | 21  | ns   |
|                                    | ST <sub>CP</sub> to Q <sub>n</sub>                          |                                               | 17   | 20  | ns   |
|                                    | MR to Q <sub>7</sub> '                                      |                                               | 14   | 19  | ns   |
| f <sub>max</sub>                   | maximum clock frequency SH <sub>CP</sub> , ST <sub>CP</sub> |                                               | 100  | 57  | MHz  |
| C <sub>I</sub>                     | input capacitance                                           |                                               | 3.5  | 3.5 | pF   |
| C <sub>PD</sub>                    | power dissipation capacitance per package                   | notes 1 and 2                                 | 115  | 130 | pF   |

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>; for HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

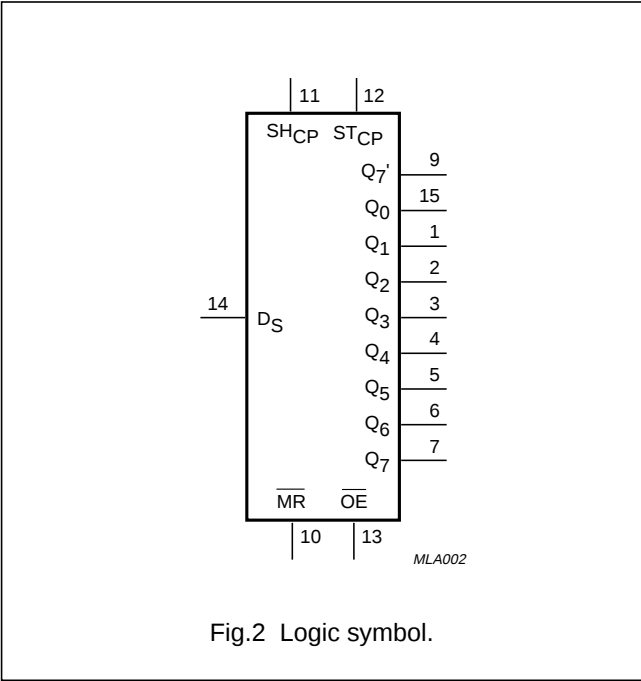
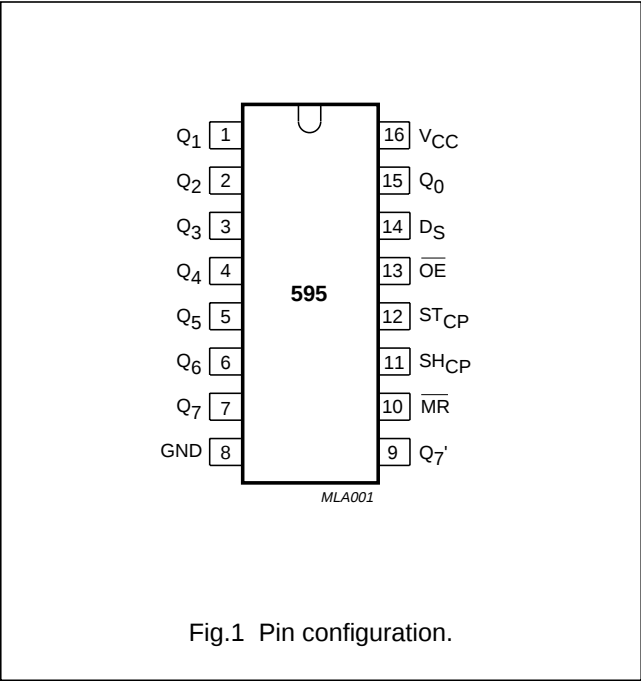
74HC/HCT595

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |                                                                        |          |
|-------------|---------|------------------------------------------------------------------------|----------|
|             | NAME    | DESCRIPTION                                                            | VERSION  |
| 74HC595N    | DIP16   | plastic dual in-line package; 16 leads (300 mil); long body            | SOT38-1  |
| 74HC595D    | SO16    | plastic small outline package; 16 leads; body width 3.9 mm             | SOT109-1 |
| 74HC595DB   | SSOP16  | plastic shrink small outline package; 16 leads; body width 5.3 mm      | SOT338-1 |
| 74HC595PW   | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT595N   | DIP16   | plastic dual in-line package; 16 leads (300 mil); long body            | SOT38-1  |
| 74HCT595D   | SO16    | plastic small outline package; 16 leads; body width 3.9 mm             | SOT109-1 |

PINNING

| SYMBOL                           | PIN        | DESCRIPTION                  |
|----------------------------------|------------|------------------------------|
| Q <sub>0</sub> to Q <sub>7</sub> | 15, 1 to 7 | parallel data output         |
| GND                              | 8          | ground (0 V)                 |
| Q <sub>7</sub> '                 | 9          | serial data output           |
| MR                               | 10         | master reset (active LOW)    |
| SH <sub>CP</sub>                 | 11         | shift register clock input   |
| ST <sub>CP</sub>                 | 12         | storage register clock input |
| OE                               | 13         | output enable (active LOW)   |
| D <sub>S</sub>                   | 14         | serial data input            |
| V <sub>CC</sub>                  | 16         | positive supply voltage      |



8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

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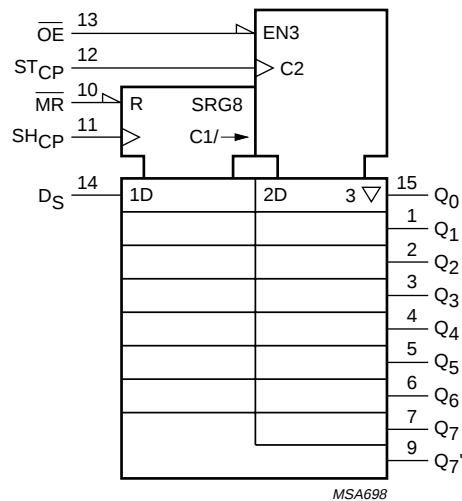


Fig.3 IEC logic symbol.

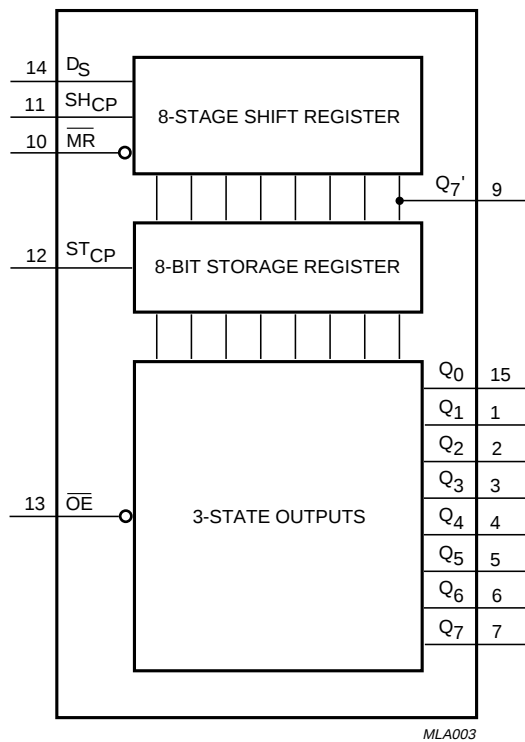


Fig.4 Functional diagram.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

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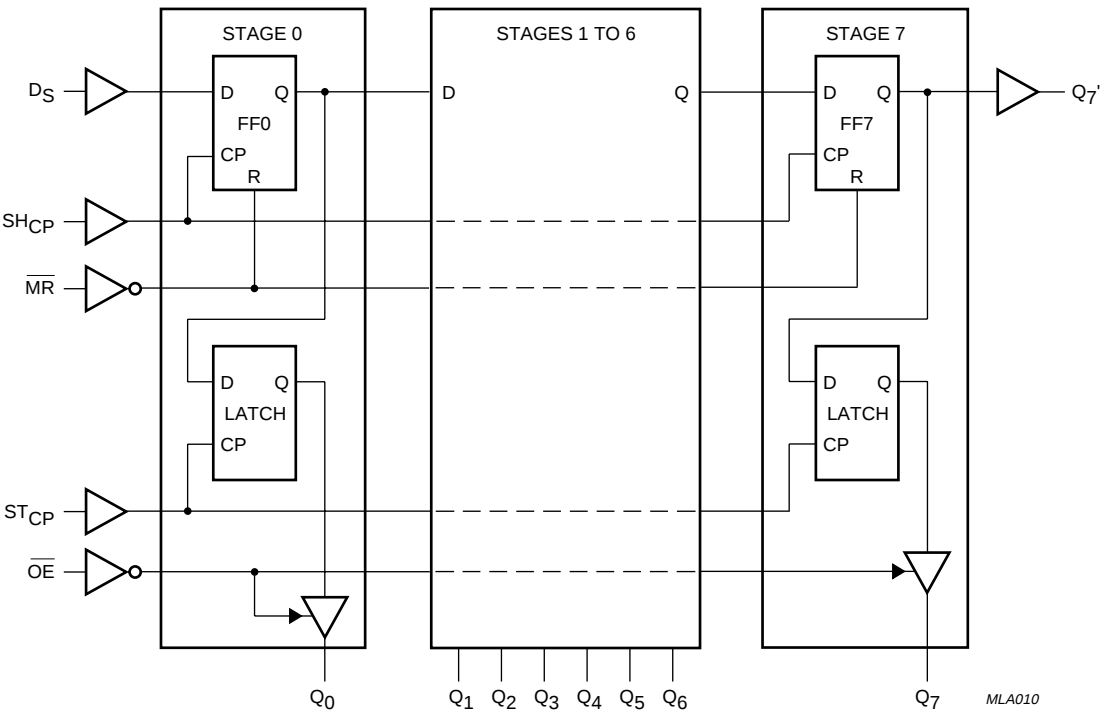


Fig.5 Logic diagram.

# 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

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FUNCTION TABLE

| INPUTS           |                  |                 |                 |                | OUTPUTS          |                  | FUNCTION                                                                                                                                                                                                                |
|------------------|------------------|-----------------|-----------------|----------------|------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SH <sub>CP</sub> | ST <sub>CP</sub> | $\overline{OE}$ | $\overline{MR}$ | D <sub>S</sub> | Q <sub>7</sub> ' | Q <sub>N</sub>   |                                                                                                                                                                                                                         |
| X                | X                | L               | L               | X              | L                | NC               | a LOW level on $\overline{MR}$ only affects the shift registers                                                                                                                                                         |
| X                | ↑                | L               | L               | X              | L                | L                | empty shift register loaded into storage register                                                                                                                                                                       |
| X                | X                | H               | L               | X              | L                | Z                | shift register clear. Parallel outputs in high-impedance OFF-state                                                                                                                                                      |
| ↑                | X                | L               | H               | H              | Q <sub>6</sub> ' | NC               | logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q <sub>6</sub> ') appears on the serial output (Q <sub>7</sub> ') |
| X                | ↑                | L               | H               | X              | NC               | Q <sub>N</sub> ' | contents of shift register stages (internal Q <sub>N</sub> ') are transferred to the storage register and parallel output stages                                                                                        |
| ↑                | ↑                | L               | H               | X              | Q <sub>6</sub> ' | Q <sub>N</sub> ' | contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.                                                              |

**Notes**

1. H = HIGH voltage level; L = LOW voltage level  
 ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition  
 Z = high-impedance OFF-state; NC = no change  
 X = don't care.

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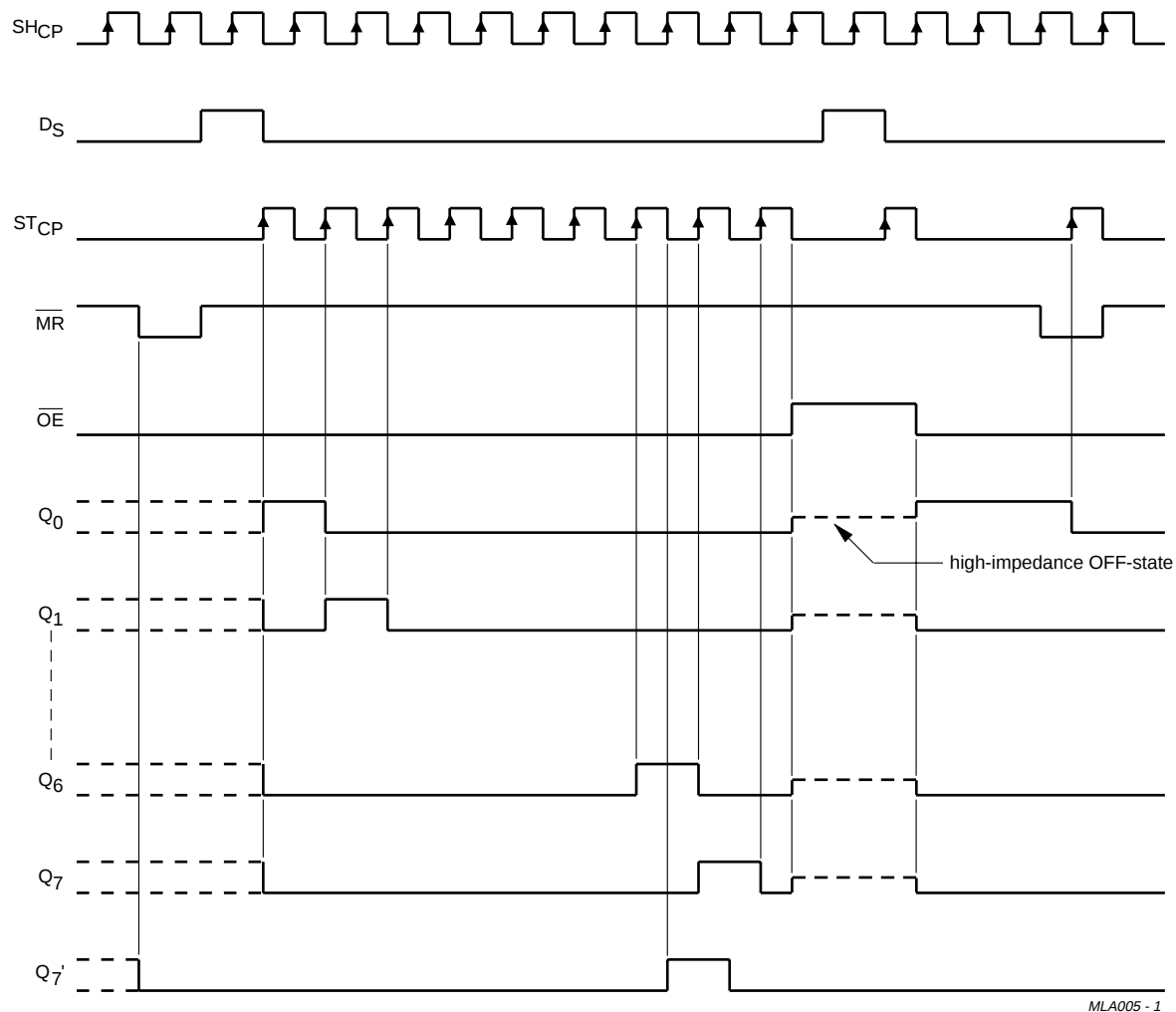


Fig.6 Timing diagram.

# 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: parallel outputs, bus driver, serial output, standard  $I_{CC}$  category: MSI.

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

| SYMBOL                             | PARAMETER                                                 | T <sub>amb</sub> (°C) |     |     |            |     |             |     | UNIT | TEST CONDITION         |           |
|------------------------------------|-----------------------------------------------------------|-----------------------|-----|-----|------------|-----|-------------|-----|------|------------------------|-----------|
|                                    |                                                           | +25                   |     |     | −40 to +85 |     | −40 to +125 |     |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                    |                                                           | min                   | typ | max | min        | max | min         | max |      |                        |           |
| t <sub>PHL</sub> /t <sub>PLH</sub> | propagation delay<br>SH <sub>CP</sub> to Q <sub>7</sub> ' | −                     | 52  | 160 | −          | 200 | −           | 240 | ns   | 2.0                    | Fig.7     |
|                                    |                                                           | −                     | 19  | 32  | −          | 40  | −           | 48  |      | 4.5                    |           |
|                                    |                                                           | −                     | 15  | 27  | −          | 34  | −           | 41  |      | 6.0                    |           |
| t <sub>PHL</sub> /t <sub>PLH</sub> | propagation delay<br>ST <sub>CP</sub> to Q <sub>n</sub>   | −                     | 55  | 175 | −          | 220 | −           | 265 | ns   | 2.0                    | Fig.8     |
|                                    |                                                           | −                     | 20  | 35  | −          | 44  | −           | 53  |      | 4.5                    |           |
|                                    |                                                           | −                     | 16  | 30  | −          | 37  | −           | 45  |      | 6.0                    |           |
| t <sub>PHL</sub>                   | propagation delay<br>MR to Q <sub>7</sub> '               | −                     | 47  | 175 | −          | 220 | −           | 265 | ns   | 2.0                    | Fig.10    |
|                                    |                                                           | −                     | 17  | 35  | −          | 44  | −           | 53  |      | 4.5                    |           |
|                                    |                                                           | −                     | 14  | 30  | −          | 37  | −           | 45  |      | 6.0                    |           |
| t <sub>PZH</sub> /t <sub>PZL</sub> | 3-state output<br>enable time<br>OE to Q <sub>n</sub>     | −                     | 47  | 150 | −          | 190 | −           | 225 | ns   | 2.0                    | Fig.11    |
|                                    |                                                           | −                     | 17  | 30  | −          | 38  | −           | 45  |      | 4.5                    |           |
|                                    |                                                           | −                     | 14  | 26  | −          | 33  | −           | 38  |      | 6.0                    |           |
| t <sub>PHZ</sub> /t <sub>PLZ</sub> | 3-state output<br>disable time<br>OE to Q <sub>n</sub>    | −                     | 41  | 150 | −          | 190 | −           | 225 | ns   | 2.0                    | Fig.11    |
|                                    |                                                           | −                     | 15  | 30  | −          | 38  | −           | 45  |      | 4.5                    |           |
|                                    |                                                           | −                     | 12  | 26  | −          | 33  | −           | 38  |      | 6.0                    |           |
| t <sub>W</sub>                     | shift clock pulse<br>width HIGH or<br>LOW                 | 75                    | 17  | −   | 95         | −   | 110         | −   | ns   | 2.0                    | Fig.7     |
|                                    |                                                           | 15                    | 6   | −   | 19         | −   | 22          | −   |      | 4.5                    |           |
|                                    |                                                           | 13                    | 5   | −   | 16         | −   | 19          | −   |      | 6.0                    |           |
| t <sub>W</sub>                     | storage clock<br>pulse width HIGH<br>or LOW               | 75                    | 11  | −   | 95         | −   | 110         | −   | ns   | 2.0                    | Fig.8     |
|                                    |                                                           | 15                    | 4   | −   | 19         | −   | 22          | −   |      | 4.5                    |           |
|                                    |                                                           | 13                    | 3   | −   | 16         | −   | 19          | −   |      | 6.0                    |           |
| t <sub>W</sub>                     | master reset<br>pulse width LOW                           | 75                    | 17  | −   | 95         | −   | 110         | −   | ns   | 2.0                    | Fig.10    |
|                                    |                                                           | 15                    | 6.0 | −   | 19         | −   | 22          | −   |      | 4.5                    |           |
|                                    |                                                           | 13                    | 5.0 | −   | 16         | −   | 19          | −   |      | 6.0                    |           |
| t <sub>su</sub>                    | set-up time D <sub>S</sub> to<br>SH <sub>CP</sub>         | 50                    | 11  | −   | 65         | −   | 75          | −   | ns   | 2.0                    | Fig.9     |
|                                    |                                                           | 10                    | 4.0 | −   | 13         | −   | 15          | −   |      | 4.5                    |           |
|                                    |                                                           | 9.0                   | 3.0 | −   | 11         | −   | 13          | −   |      | 6.0                    |           |
| t <sub>su</sub>                    | set-up time SH <sub>CP</sub><br>to ST <sub>CP</sub>       | 75                    | 22  | −   | 95         | −   | 110         | −   | ns   | 2.0                    | Fig.8     |
|                                    |                                                           | 15                    | 8   | −   | 19         | −   | 22          | −   |      | 4.5                    |           |
|                                    |                                                           | 13                    | 7   | −   | 16         | −   | 19          | −   |      | 6.0                    |           |

8-bit serial-in/serial or parallel-out shift  
register with output latches; 3-state

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| SYMBOL           | PARAMETER                                                          | T <sub>amb</sub> (°C) |     |     |            |     |             |     | UNIT | TEST CONDITION      |              |
|------------------|--------------------------------------------------------------------|-----------------------|-----|-----|------------|-----|-------------|-----|------|---------------------|--------------|
|                  |                                                                    | +25                   |     |     | −40 to +85 |     | −40 to +125 |     |      | V <sub>CC</sub> (V) | WAVEFORMS    |
|                  |                                                                    | min                   | typ | max | min        | max | min         | max |      |                     |              |
| t <sub>h</sub>   | hold time D <sub>S</sub> to SH <sub>CP</sub>                       | 3                     | −6  | −   | 3          | −   | 3           | −   | ns   | 2.0                 | Fig.9        |
|                  |                                                                    | 3                     | −2  | −   | 3          | −   | 3           | −   |      | 4.5                 |              |
|                  |                                                                    | 3                     | −2  | −   | 3          | −   | 3           | −   |      | 6.0                 |              |
| t <sub>rem</sub> | removal time $\overline{\text{MR}}$ to SH <sub>CP</sub>            | 50                    | −19 | −   | 65         | −   | 75          | −   | ns   | 2.0                 | Fig.10       |
|                  |                                                                    | 10                    | −7  | −   | 13         | −   | 15          | −   |      | 4.5                 |              |
|                  |                                                                    | 9                     | −6  | −   | 11         | −   | 13          | −   |      | 6.0                 |              |
| f <sub>max</sub> | maximum clock pulse frequency SH <sub>CP</sub> or ST <sub>CP</sub> | 9                     | 30  | −   | 4.8        | −   | 4           | −   | MHz  | 2.0                 | Figs 7 and 8 |
|                  |                                                                    | 30                    | 91  | −   | 24         | −   | 20          | −   |      | 4.5                 |              |
|                  |                                                                    | 35                    | 108 | −   | 28         | −   | 24          | −   |      | 6.0                 |              |

# 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: parallel outputs, bus driver; serial output, standard  $I_{CC}$  category: MSI.

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

| INPUT           | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| $D_S$           | 0.25                  |
| $\overline{MR}$ | 1.50                  |
| $SH_{CP}$       | 1.50                  |
| $ST_{CP}$       | 1.50                  |
| $\overline{OE}$ | 1.50                  |

# 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

## AC CHARACTERISTICS FOR 74HCT

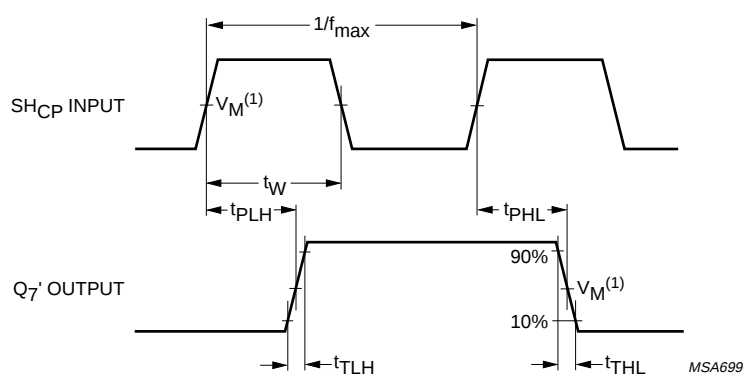
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

| SYMBOL                              | PARAMETER                                                                | T <sub>amb</sub> (°C) |     |     |            |     |             |     | UNIT | TEST CONDITION      |              |
|-------------------------------------|--------------------------------------------------------------------------|-----------------------|-----|-----|------------|-----|-------------|-----|------|---------------------|--------------|
|                                     |                                                                          | +25                   |     |     | −40 to +85 |     | −40 to +125 |     |      | V <sub>CC</sub> (V) | WAVEFORMS    |
|                                     |                                                                          | min                   | typ | max | min        | max | min         | max |      |                     |              |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>SH <sub>CP</sub> to Q <sub>7</sub> '                | –                     | 25  | 42  | –          | 53  | –           | 63  | ns   | 4.5                 | Fig.7        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>ST <sub>CP</sub> to Q <sub>n</sub>                  | –                     | 24  | 40  | –          | 50  | –           | 60  | ns   | 4.5                 | Fig.8        |
| t <sub>PHL</sub>                    | propagation delay<br>MR to Q <sub>7</sub> '                              | –                     | 23  | 40  | –          | 50  | –           | 60  | ns   | 4.5                 | Fig.10       |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable<br>time OE to Q <sub>n</sub>                       | –                     | 21  | 35  | –          | 44  | –           | 53  | ns   | 4.5                 | Fig.11       |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable<br>time OE to Q <sub>n</sub>                      | –                     | 18  | 30  | –          | 38  | –           | 45  | ns   | 4.5                 | Fig.11       |
| t <sub>W</sub>                      | shift clock pulse<br>width HIGH or LOW                                   | 16                    | 6   | –   | 20         | –   | 24          | –   | ns   | 4.5                 | Fig.7        |
| t <sub>W</sub>                      | storage clock pulse width<br>HIGH or LOW                                 | 16                    | 5   | –   | 20         | –   | 24          | –   | ns   | 4.5                 | Fig.8        |
| t <sub>W</sub>                      | master reset<br>pulse width LOW                                          | 20                    | 8   | –   | 25         | –   | 30          | –   | ns   | 4.5                 | Fig.10       |
| t <sub>su</sub>                     | set-up time D <sub>S</sub> to<br>SH <sub>SP</sub>                        | 16                    | 5   | –   | 20         | –   | 24          | –   | ns   | 4.5                 | Fig.9        |
| t <sub>su</sub>                     | set-up time SH <sub>CP</sub><br>to ST <sub>CP</sub>                      | 16                    | 8   | –   | 20         | –   | 24          | –   | ns   | 4.5                 | Fig.8        |
| t <sub>h</sub>                      | hold time D <sub>S</sub> to SH <sub>CP</sub>                             | 3                     | −2  | –   | 3          | –   | 3           | –   | ns   | 4.5                 | Fig.9        |
| t <sub>rem</sub>                    | removal time MR to<br>SH <sub>CP</sub>                                   | 10                    | −7  | –   | 13         | –   | 15          | –   | ns   | 4.5                 | Fig.10       |
| f <sub>max</sub>                    | maximum clock<br>pulse frequency<br>SH <sub>CP</sub> or ST <sub>CP</sub> | 30                    | 52  | –   | 24         | –   | 20          | –   | MHz  | 4.5                 | Figs 7 and 8 |

# 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

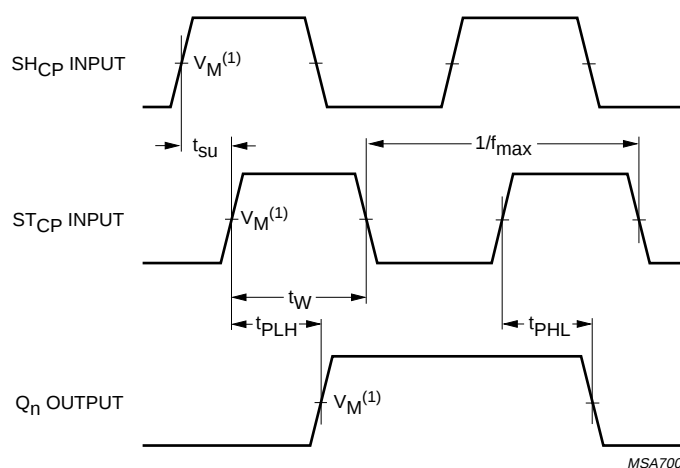
74HC/HCT595

## AC WAVEFORMS



- (1) HC:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$   
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the clock (SH<sub>CP</sub>) to output (Q<sub>7'</sub>) propagation delays, the shift clock pulse width and maximum shift clock frequency.

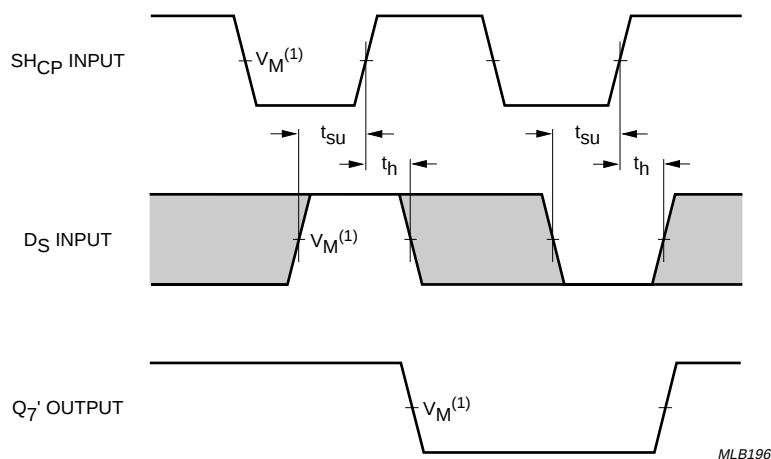


- (1) HC:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$   
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.8 Waveforms showing the storage clock (ST<sub>CP</sub>) to output (Q<sub>n</sub>) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

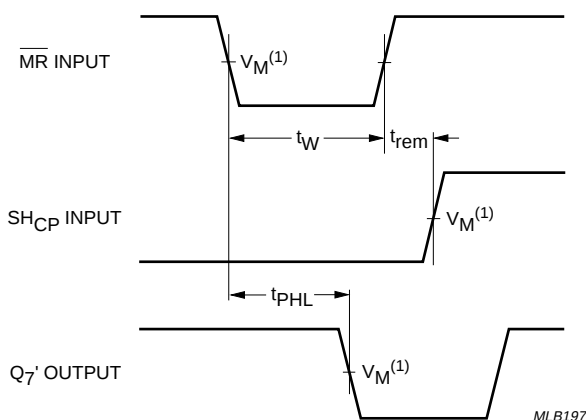
# 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595



- (1) HC:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$   
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.9 Waveforms showing the data set-up and hold times for the  $D_S$  input.

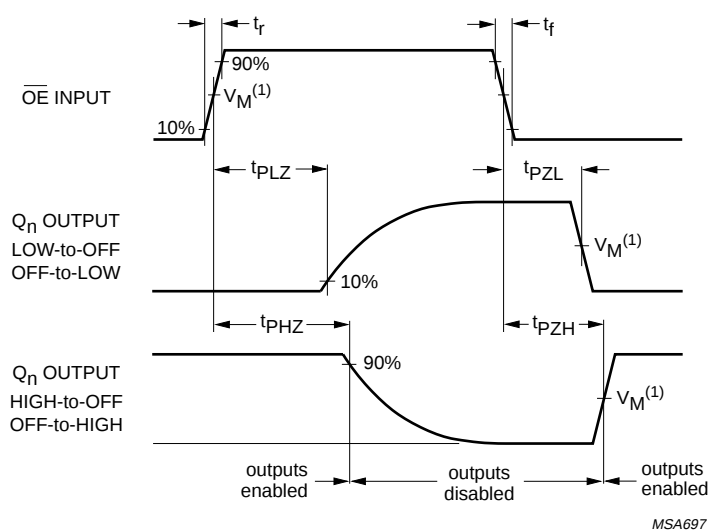


- (1) HC:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$   
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.10 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width, the master reset to output ( $Q_7'$ ) propagation delay and the master reset to shift clock ( $SH_{CP}$ ) removal time.

# 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595



MSA697

- (1) HC:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$   
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.11 Waveforms showing the 3-state enable and disable times for input  $\overline{OE}$ .

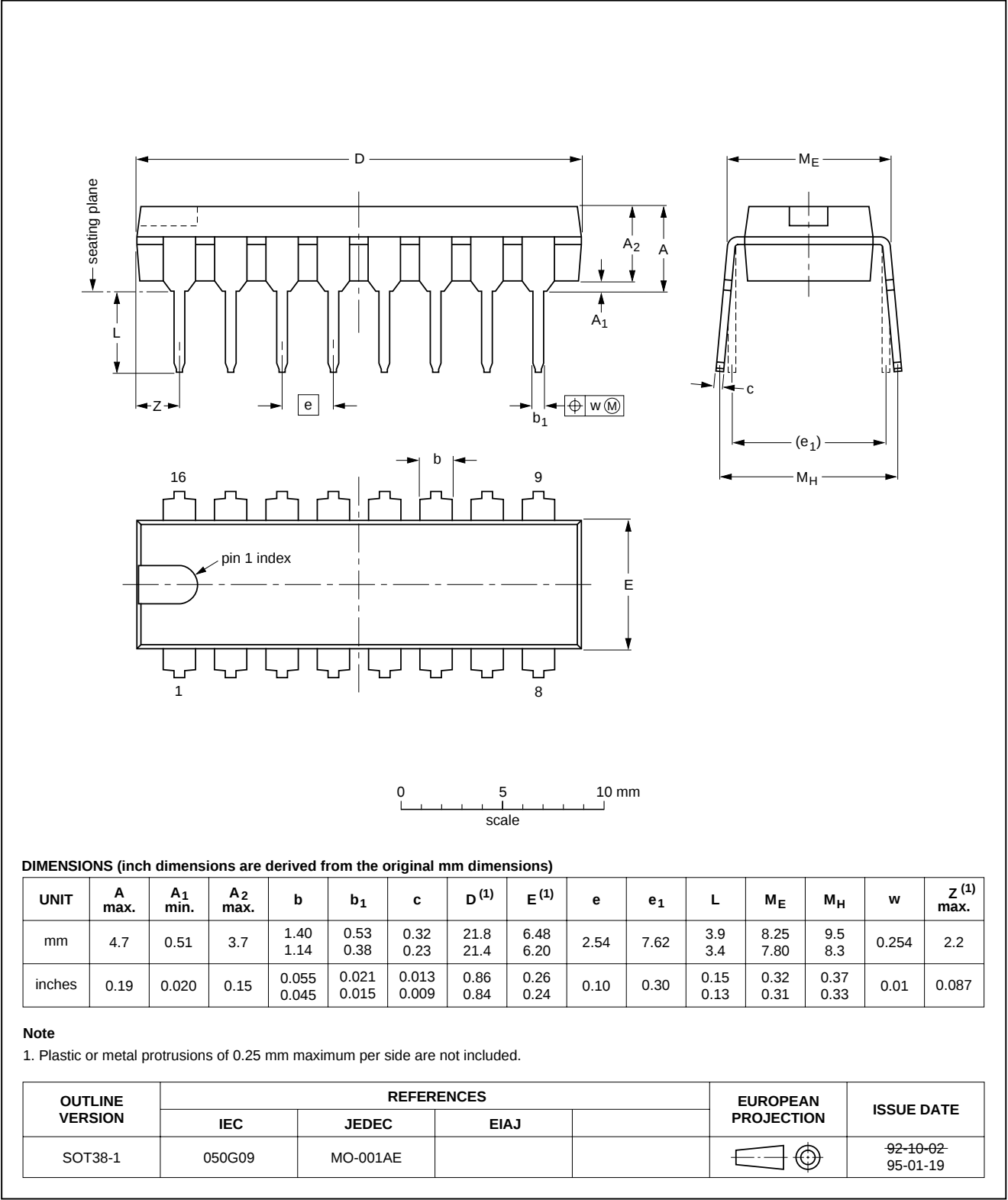
8-bit serial-in/serial or parallel-out shift  
register with output latches; 3-state

74HC/HCT595

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1

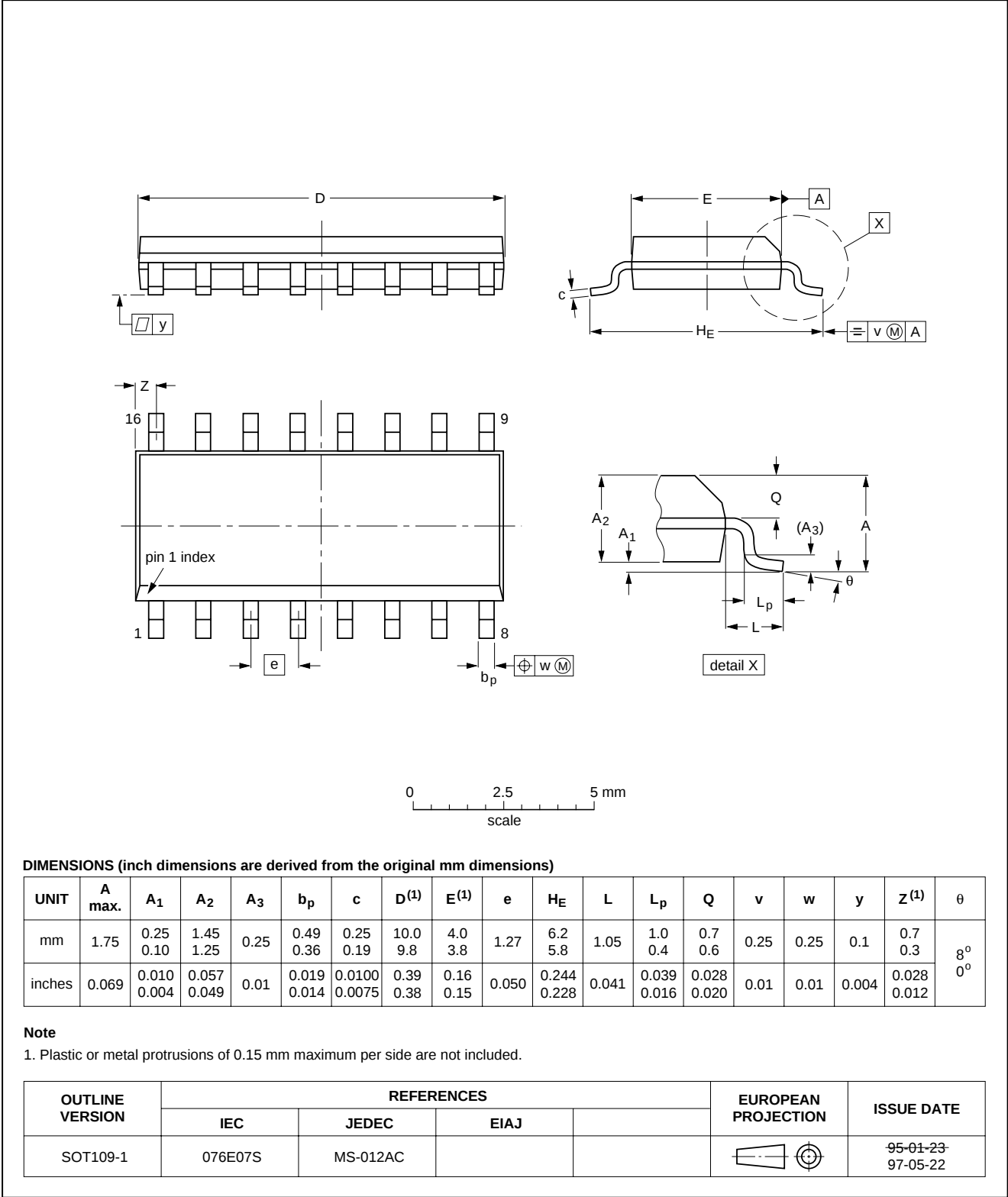


8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

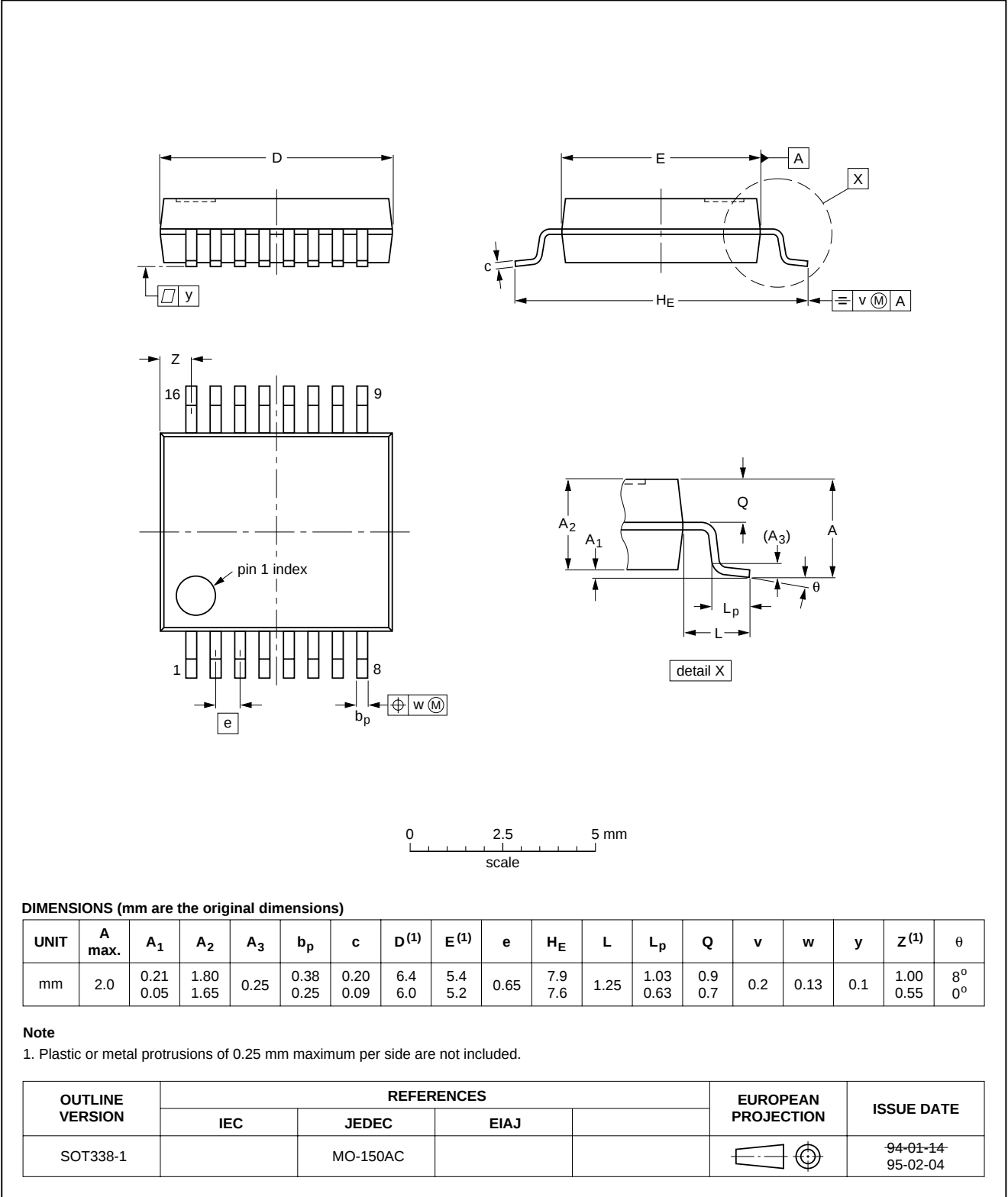


8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

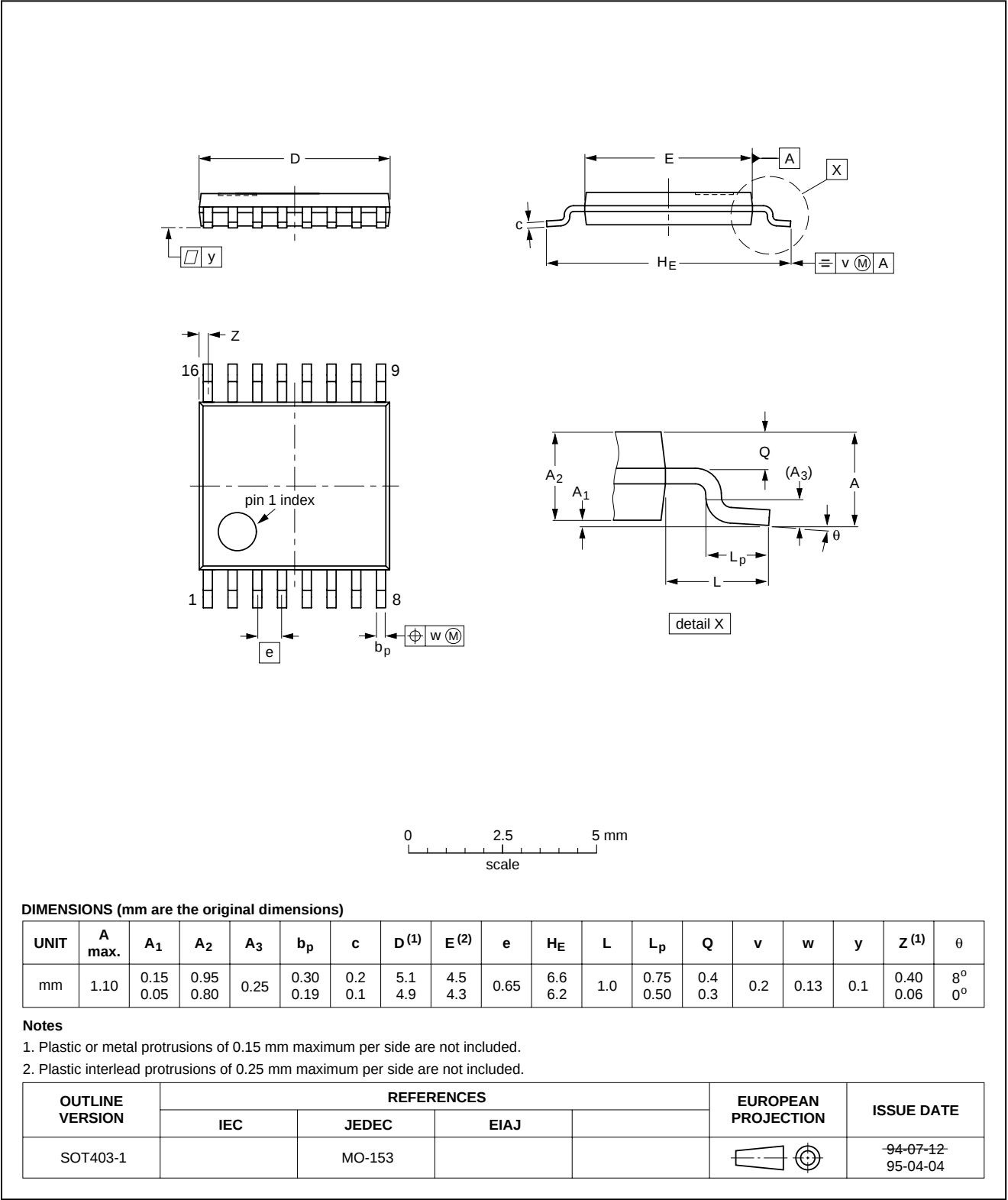


8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



## 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

#### DIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### SO, SSOP and TSSOP

#### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### WAVE SOLDERING

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

## 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

## 74HC/HCT595

### Even with these conditions:

- Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

### DEFINITIONS

| Data sheet status                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                       |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification                                                                                                                                                                                                                                                                                                                                                                                                                                   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification                                                                                                                                                                                                                                                                                                                                                                                                                                 | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification                                                                                                                                                                                                                                                                                                                                                                                                                                     | This data sheet contains final product specifications.                                |
| Limiting values                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                       |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |                                                                                       |
| Application information                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                                                                       |
| Where application information is given, it is advisory and does not form part of the specification.                                                                                                                                                                                                                                                                                                                                                       |                                                                                       |

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.