



3.3V CMOS PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET, 5 VOLT TOLERANT I/O

IDT74LVC163A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Vcc = 3.3V ± 0.3V, Normal Range
- Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs, and I/Os are 5V tolerant
- Supports hot insertion
- Available in QSOP, SOIC, SSOP, and TSSOP packages

DRIVE FEATURES:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

The LVC163A is a synchronous presettable binary counter, which features an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all the flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

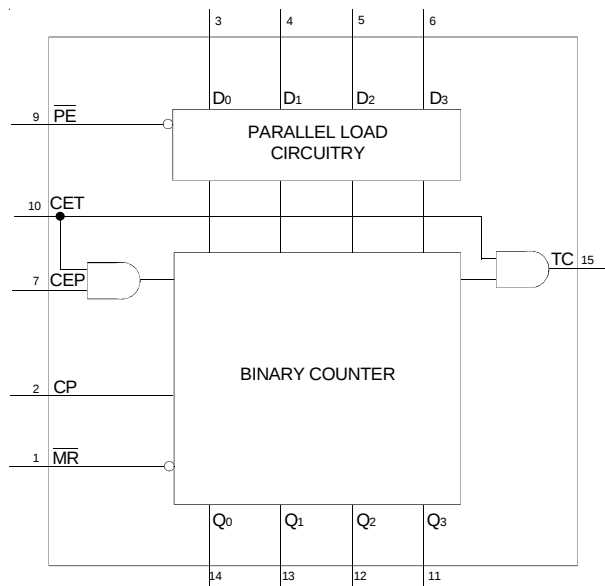
Outputs (Q₀ to Q₃) may be preset to a high or low level. A low level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D₀ to D₃) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q₀ to Q₃) to low level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for PE are met).

This action occurs regardless of the levels of CP, $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

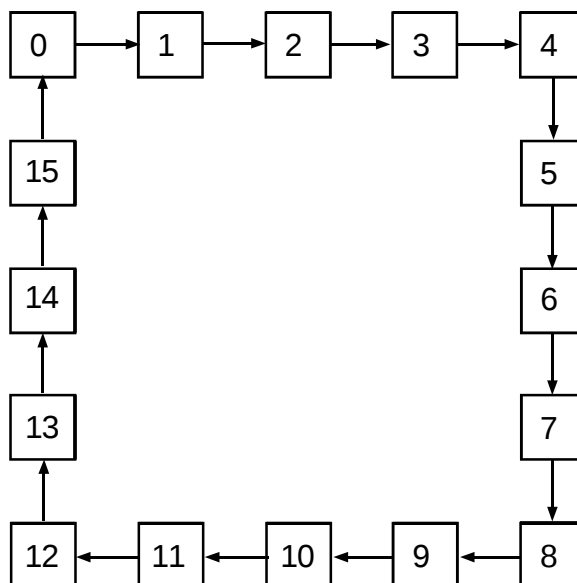
The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be high to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a high output pulse of a duration approximately equal to a high level output of Q₀. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{\max} = \frac{1}{t_{p(\max)} (\text{CP to TC}) + t_{su} (\text{CEP to CP})}$$

FUNCTIONAL DIAGRAM



STATE DIAGRAM

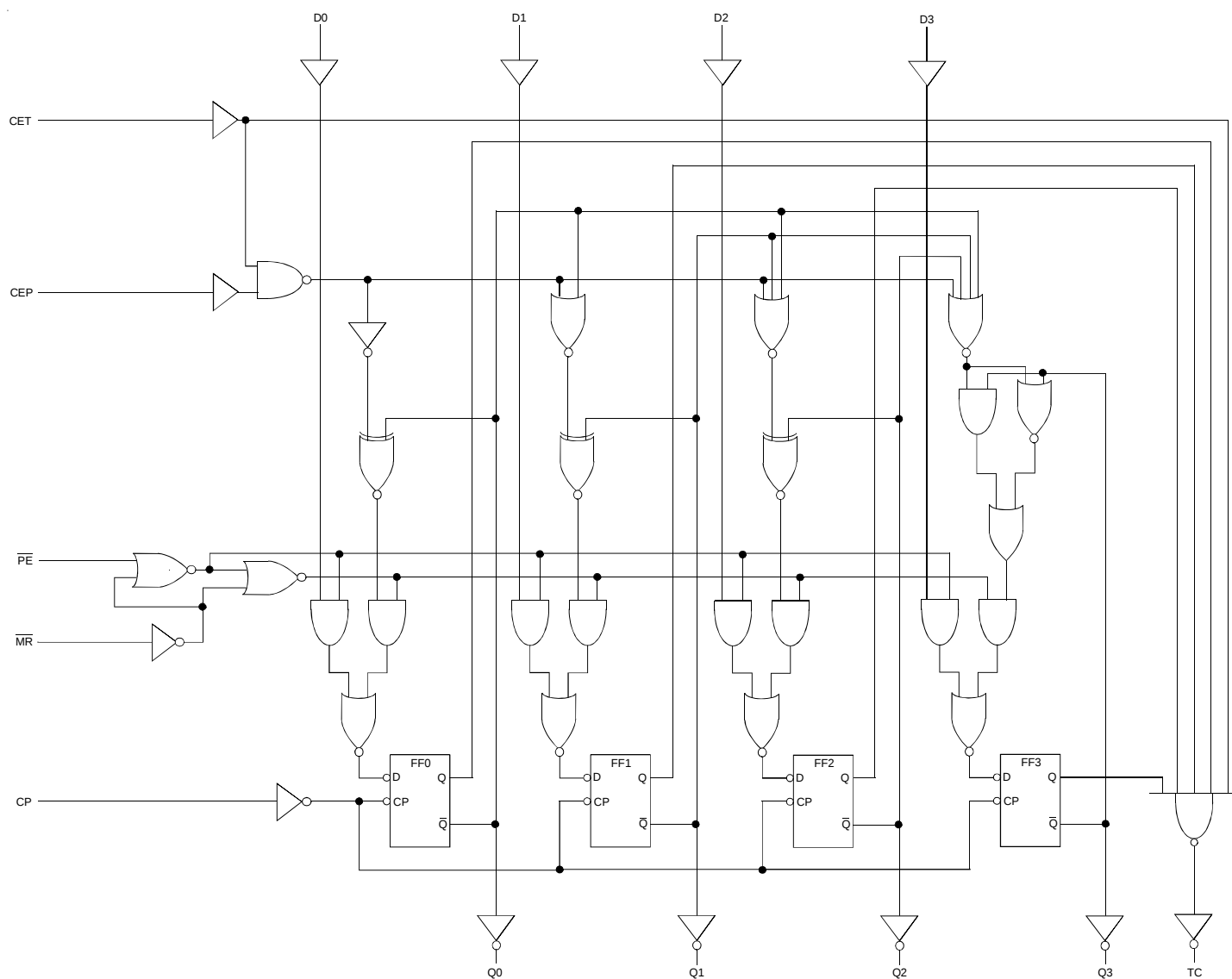


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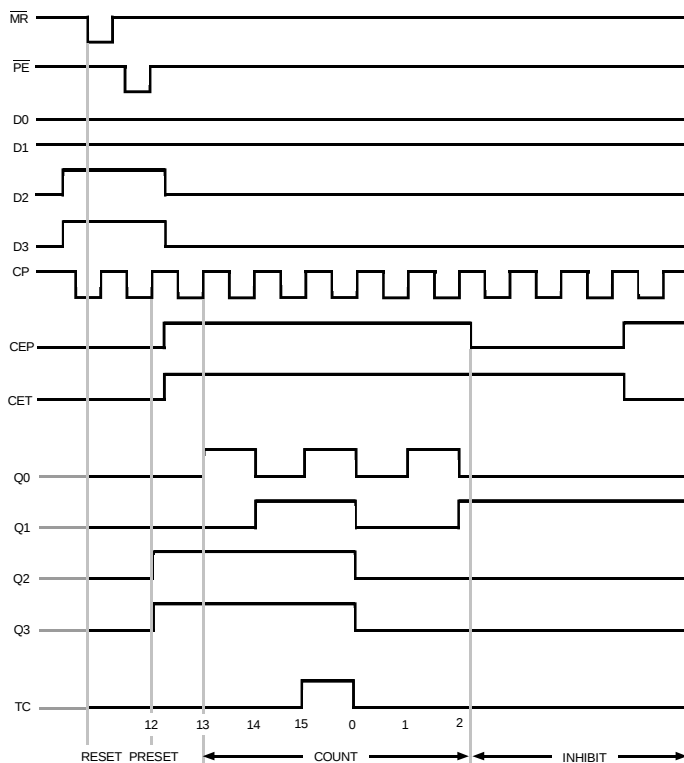
INDUSTRIAL TEMPERATURE RANGE

OCTOBER 1999

FUNCTIONAL BLOCK DIAGRAM



TYPICAL TIMING SEQUENCE



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	-50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

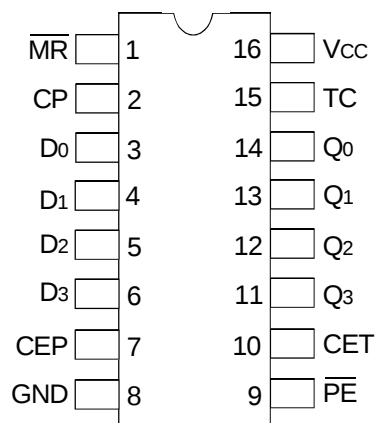
CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

PIN CONFIGURATION



SOIC/ SSOP/ TSSOP/ QSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{MR}$	Asynchronous Master Reset (Active LOW)
CP	Clock Input (LOW-to-HIGH, Edge-Triggered)
Dx	Data Inputs
CEP	Count Enable Inputs
GND	Ground (0V)
$\overline{PE}$	Parallel Enable Input (Active LOW)
CET	Count Enable Carry Input
Qx	Flip-Flop Outputs
TC	Terminal Count Output
V _{CC}	Positive Supply Voltage

FUNCTION TABLE (1)

OPERATING MODES	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dx	Qx	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
Count	h	↑	h	h	h	X	count	*
Hold	h	X	l	X	h	X	Q ⁽²⁾	*
(do nothing)	h	X	X	l	h	X	Q ⁽²⁾	L

NOTE:

- H = HIGH Voltage Level
 h = HIGH Voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW Voltage Level
 l = LOW Voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care
 * = The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH).
 ↑ = LOW-to-HIGH clock transition
- Indicates the state of the referenced output one set up time prior to the LOW-to-HIGH clock transition.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH} ⁽²⁾	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC} L I _{CC} H I _{CC} Z	Quiescent Power Supply Current	V _{CC} = 3.6V, V _{IN} = GND or V _{CC}		—	—	10	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

NOTES:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Clock Pin (CP) requires a minimum V_{IH} of 2.5V.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = – 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IoL = 0.1mA	—	0.2	V
		VCC = 2.3V	IoL = 6mA	—	0.4	
			IoL = 12mA	—	0.7	
		VCC = 2.7V	IoL = 12mA	—	0.4	
		VCC = 3V	IoL = 24mA	—	0.55	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance	CL = 0pF, f = 10Mhz	—	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay CP to Qx	—	9	—	8	ns
tPLH tPHL	Propagation Delay CP to TC	—	11	—	9.5	ns
tPLH tPHL	Propagation Delay CET to TC	—	8.8	—	7.8	ns
tW	Clock Pulse Width, HIGH or LOW	5	—	4	—	ns
tSU	Set-Up Time, Dx to CP	3.5	—	3	—	ns
tSU	Set-Up Time, MR, PE to CP	3.5	—	3	—	ns
tSU	Set-Up Time, CEP, CET to CP	5.5	—	5	—	ns
tH	Hold Time, Dx, PE, CEP, CET, MR to CP	0	—	0	—	ns
tsk(0)	Output Skew ⁽²⁾	—	—	—	500	ps

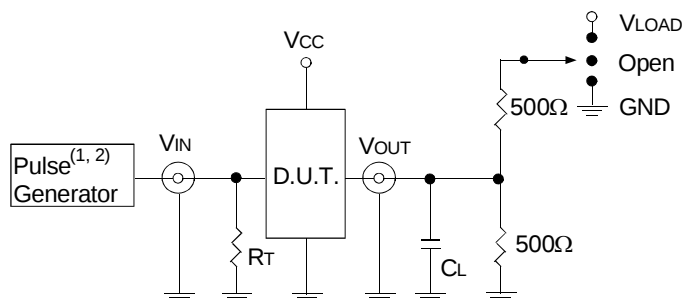
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. TA = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ = 2.5V ± 0.2V	V _{CC} ⁽²⁾ = 3.3V ± 0.3V & 2.7V	Unit
V _{LOAD}	2 x V _{CC}	6	V
V _{IH}	V _{CC}	2.7	V
V _T	V _{CC} / 2	1.5	V
V _{LZ}	150	300	mV
V _{HZ}	150	300	mV
C _L	30	50	pF



Test Circuit for All Outputs

DEFINITIONS:

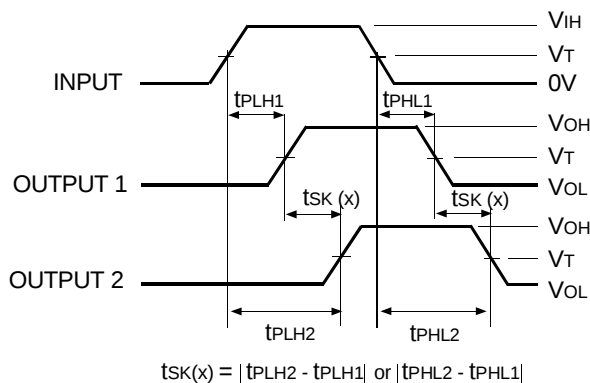
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.

SWITCH POSITION

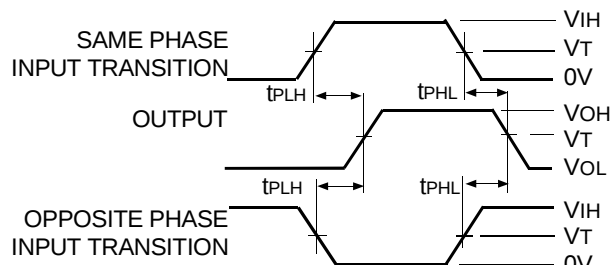
Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



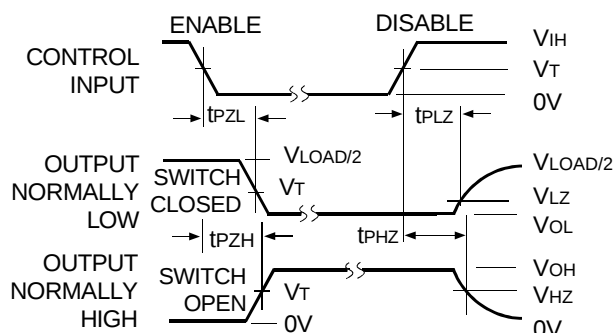
Output Skew - t_{SK}(x)

NOTES:

1. For t_{SK}(0) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.



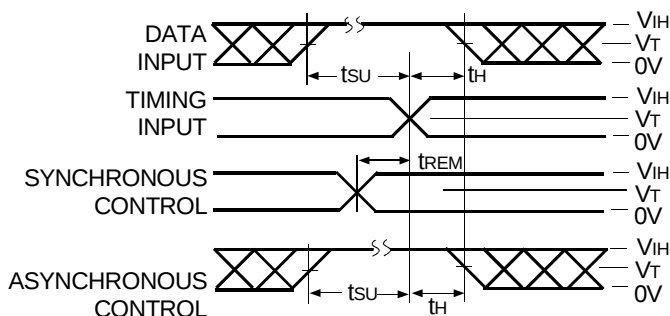
Propagation Delay



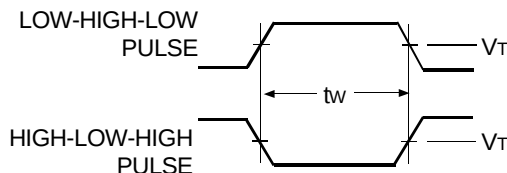
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT	XX	LVC	XXXX	XX	
Temp. Range		Device Type		Package	
				Q	Quarter Size Outline Package
				DC	Small Outline IC
				PY	Shrink Small Outline Package
				PG	Thin Shrink Small Outline Package
				163A	3.3V CMOS Presettable Synchronous 4-Bit Binary Counter with Synchronous Reset, 5 Volt Tolerant I/O, $\pm 24\text{mA}$
				74	-40°C to $+85^{\circ}\text{C}$



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