M58BF008

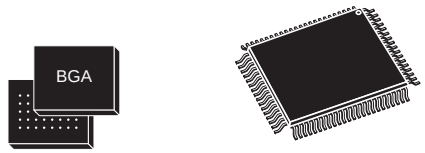
8 Mbit (256Kb x32, Burst) Flash Memory

PRELIMINARY DATA

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{DD} = 5V for Program, Erase and Read
  - V_{DDQ} = 3.3V for I/O Buffers
  - V_{PP} = 12V for fast Program (optional)
- CONFIGURABLE OPTIONS
  - Synchronous or Asynchronous write mode
  - Burst Wrap
  - Critical Word X (3 or 4) and Burst Word Y (1 or 2) latency times
- ACCESS TIME
  - Synchronous X-Y-Y-Y Burst Read up to 40MHz
  - Asynchronous Read: 90ns
- PROGRAMMING TIME: 10µs typical
- MEMORY BLOCKS
  - 32 equal Main blocks of 256 Kbit
  - One Overlay block of 256 Kbit
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code: F0h
  - Version Code: 0-7h

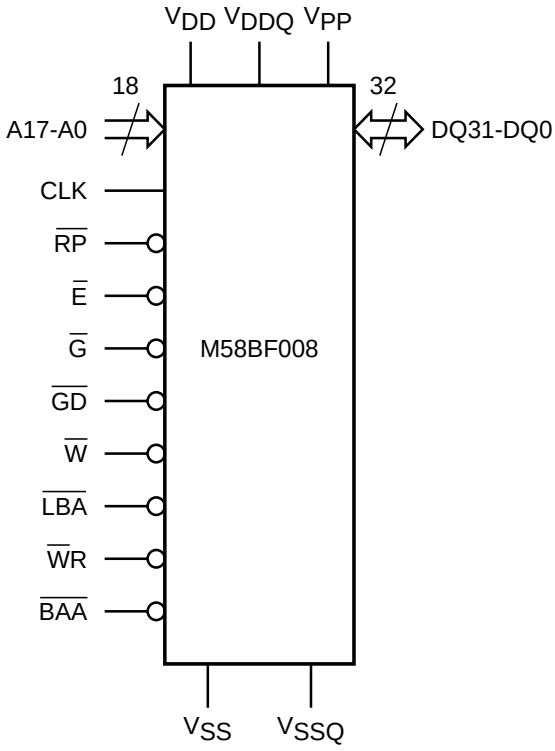
Figure 1. Packages



LBGA80 (ZA)
10 x 8 ball array

PQFP80 (T)

Figure 2. Logic Diagram



DESCRIPTION

The M58BF008 is a family of 8 Mbit non-volatile Flash memories that can be erased electrically at the block level and programmed in-system. Family members are configured during product testing for a specific Synchronous or Asynchronous Write mode, a Burst Wrap and for Critical Word X = 3 or 4 and Burst Word Y = 1 or 2 latency times. The Main memory array matrix allows each of the 32 equal blocks of 256 Kbit to be erased separately and re-programmed without affecting other blocks. The memory features a 256 Kbit Overlay block having the same address space as the Main block 0. The Overlay block provides a secure storage area that is controlled by special Instructions and an external input. A separate supply V_{DDQ} allows the Input/Output signals to be at 3.3V levels, while the main supply V_{DD} is 5V.

When the V_{PP} supply is at V_{SS} this prevents programming and erasure of the memory blocks and, in addition, it prevents reading of the Overlay block. When the V_{PP} supply is at 5V it enables both in-system program/erase and read access to the Overlay block. For a limited time and number of program/erase cycles the V_{PP} supply may be raised to 12V to provide fast program and erase times.

A Command Interface decodes the Instructions written to the memory to access or modify the memory content, to toggle the enable/disable of read access to the Overlay block, to toggle the Synchronous or Asynchronous Read mode. A Program/Erase Controller (P/E.C.) executes the algorithms taking care of the timings necessary for program and erase operations. The P/E.C. also takes care of verification to unburden the system microprocessor, while a Status Register tracks the status of each operation.

The following Instructions are executed by the memory in either Asynchronous or Synchronous mode.

Access or modify memory content:

- Read Array
- Read or Clear Status Register
- Read Electronic Signature
- Erase Main memory block or Overlay block
- Program Main memory or Overlay memory
- Program Erase Suspend or Resume

Toggle:

– Asynchronous/Synchronous Read

– Overlay Block Read Enable/Disable

The M58BF008 devices are offered in PQFP80 and LBGA80 1.0mm ball pitch packages.

Table 1. Signal Names

A0-A17	Address Inputs
DQ0-DQ31	Data Input/Output
CLK	System Clock
$\overline{RP}$	Reset/Power-down
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{GD}$	Output Disable
$\overline{W}$	Write Enable
$\overline{LBA}$	Load Burst Address
$\overline{WR}$	Write/Read
$\overline{BAA}$	Burst Address Advance
V_{DD}	Supply Voltage
V_{DDQ}	Supply Voltage for Input/Output Buffers
V_{PP}	Optional Supply Voltage for Fast Program and fast Erase Operations
V_{SS}	Ground
V_{SSQ}	Input/Output Ground
DU	Don't Use as Internally Connected
NC	Not Connected Internally

Figure 3. LBGA Connections (Top view through package)

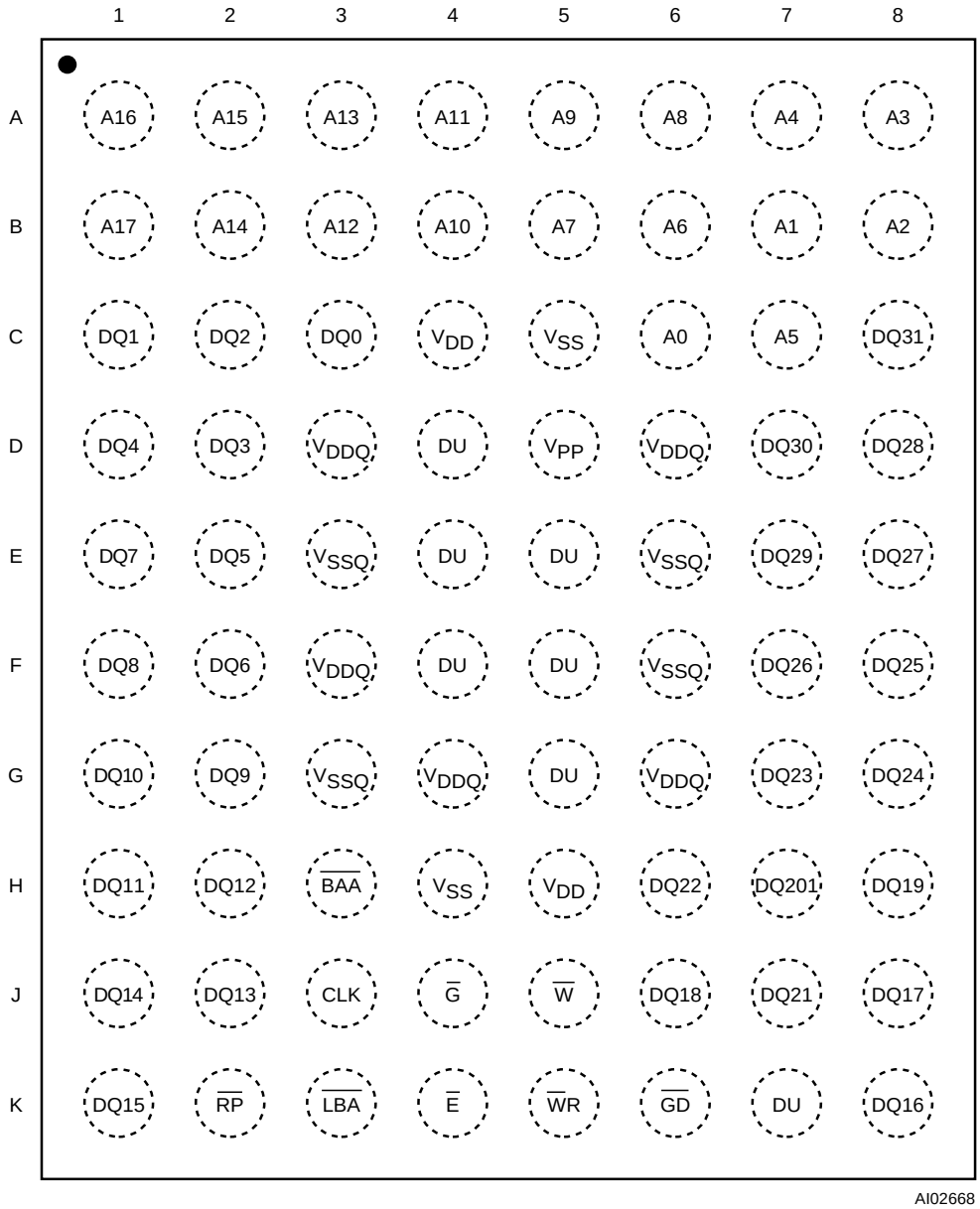


Figure 4. PQFP Connections

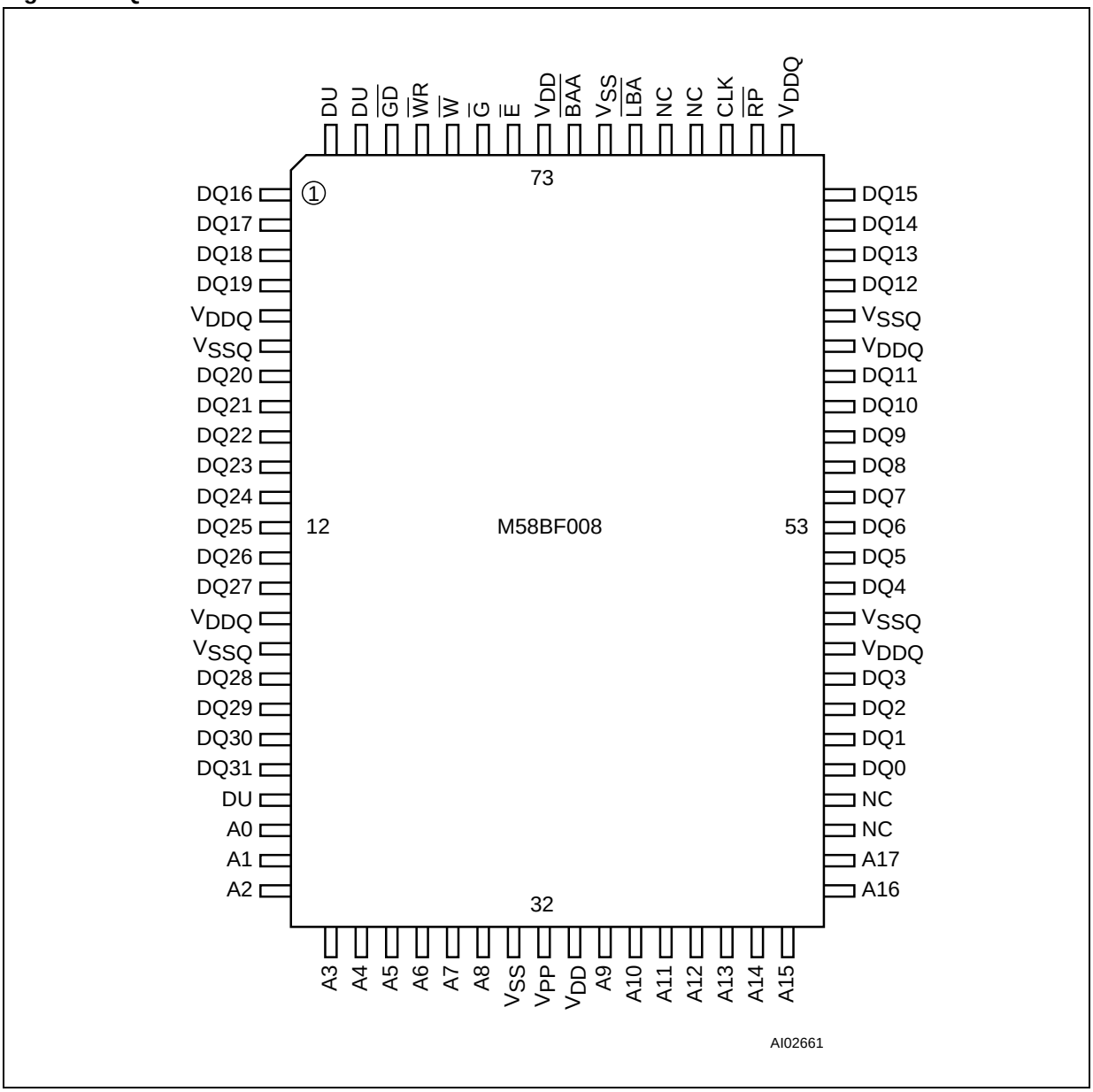


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–40 to 125	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IO}	Input Output Voltage	–0.6 to V_{DDQ} +0.6	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.6 to 7	V
V_{PP}	Program Voltage	–0.6 to 13.5	V

Note: 1. Stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device.

ORGANIZATION

The M58BF008 has a data path width of 32 bit (Double-Word) and is organised as a Main memory array of 32 blocks of 256 Kbit plus an Overlay block of 256 Kbit having the same address space as the Main block 0. The memory map is shown in Table 3.

The memory is addressed by A0-A17 which are static for Asynchronous or latched for Synchronous operation. Data Input/Output is static or latched on DQ0-DQ31, these signals output data, status or signatures read from the memory, or they input data to be programmed or Instruction commands to the Command Interface.

Asynchronous mode

Memory control is provided by Chip Enable $\overline{E}$, Output Enable $\overline{G}$, Output Disable $\overline{GD}$ and Write Enable $\overline{W}$ for read and write operations.

Synchronous mode

Memory control is provided by Load Burst Address $\overline{LBA}$ which loads a read or write address. A Synchronous Single Read or a Synchronous Burst Read is performed under control of Output Enable $\overline{G}$ and Output Disable $\overline{GD}$. Synchronous Write is controlled by Write/Read Enable $\overline{WR}$, Load Burst Address $\overline{LBA}$ and Write Enable $\overline{W}$. Internal advance of the burst address is controlled by Burst Address Advance $\overline{BAA}$.

Table 3. Block Addresses

#	Size (Kbit)	Address Range
31	256	3E000-3FFFF
30	256	3C000-3DFFF
29	256	3A000-3BFFF
28	256	38000-39FFF
27	256	36000-37FFF
26	256	34000-35FFF
25	256	32000-33FFF
24	256	30000-31FFF
23	256	2E000-2FFFF
22	256	2C000-2DFFF
21	256	2A000-2BFFF
20	256	28000-29FFF
19	256	26000-27FFF
18	256	24000-25FFF
17	256	22000-23FFF
16	256	20000-21FFF
15	256	1E000-1FFFF
14	256	1C000-1DFFF
13	256	1A000-1BFFF
12	256	18000-19FFF
11	256	16000-17FFF
10	256	14000-15FFF
9	256	12000-13FFF
8	256	10000-11FFF
7	256	0E000-0FFFF
6	256	0C000-0DFFF
5	256	0A000-0BFFF
4	256	08000-09FFF
3	256	06000-07FFF
2	256	04000-05FFF
1	256	02000-03FFF
0	256	00000-01FFF
Overlay Block	256	00000-01FFF

SIGNAL DESCRIPTIONS

See Figure 2 and Table 1.

Address Inputs (A0-A17). The address signal A17 is the MSB and A0 the LSB.

In the Asynchronous mode the addresses must be stable before Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ go to V_{IL}. They must remain stable during the read or write cycle.

In the Synchronous modes, the addresses are latched by the rising edge of the System Clock CLK when both Latch Burst Address LBA and Chip Enable $\overline{E}$ are at V_{IL}. The addresses are latched for a read operation if Write/Read WR is at V_{IH} or for a write operation when it is at V_{IL}.

Data Input/Output (DQ0-DQ31). The data signal DQ31 is the MSB and DQ0 the LSB. Commands are input on DQ0-DQ7.

Data input is a Double-Word to be programmed in the memory or an Instruction command to the Command Interface. Data is read from the Main or Overlay memory blocks, the Status Register or the Electronic Signature.

In the Asynchronous mode data is read when the addresses are stable and Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are at V_{IL} and Output Disable $\overline{GD}$ is at V_{IH}. Commands or address/data are written when Chip Enable $\overline{E}$ and Write $\overline{W}$ are at V_{IL}.

In the Synchronous mode, after addresses are latched, data is read on a rising edge of the System Clock CLK when Chip Enable $\overline{E}$ is at V_{IL} and if Output Enable was at V_{IL} on the previous rising clock edge. Data is written on a rising edge of the System Clock CLK when Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are at V_{IL}.

The outputs are high impedance when Chip Enable $\overline{E}$ or Output Enable $\overline{G}$ are at V_{IH}, or when Output Disable $\overline{GD}$ is at V_{IL}. Outputs are also high impedance when System Reset $\overline{RP}$ is at V_{IL}.

System Clock (CLK). During synchronous read/write modes, signals are input and output relative to the System Clock. Input signals must respect the set-up and hold times relative to the System Clock rising edge.

Reset/Power-down ($\overline{RP}$). The Reset/Power-down RP input provides a hardware reset for the memory. When Reset/Power-down $\overline{RP}$ is at V_{IL} the memory is reset and in the Power-down mode. In this mode the outputs are high impedance and the current consumption is minimised. When Reset/Power-down $\overline{RP}$ is at V_{IH} the memory is in the normal operating mode. When leaving the Power-down mode the memory enters the Asynchronous Read Array mode and the VPP voltage level is sampled to decide if the overlay block is enabled.

Reset/Power-down has a weak pull-up resistor to V_{DDQ} and will assume a high level if not externally connected.

Chip Enable ($\overline{E}$). When the Chip Enable $\overline{E}$ input is at V_{IL} it activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable $\overline{E}$ is at V_{IH} the memory is deselected and the power consumption is reduced to the standby level.

Output Enable ($\overline{G}$). Output Enable $\overline{G}$ controls the data output buffers with the combination of $\overline{GD}$ (see Table 4). In the Asynchronous mode data is output when Output Enable $\overline{G}$ is at V_{IL}. In the Synchronous mode, Output Enable $\overline{G}$ is sampled on the rising edge of the System Clock CLK. If Output Enable $\overline{E}$ is at V_{IL} then valid output data on DQ0-DQ31 can be read at the next rising edge of the System Clock CLK.

Table 4. Data Output Contol

$\overline{G}$	$\overline{GD}$	DQ0-DQ31
V_{IH}	V_{IH}	Hi-Z
V_{IL}	V_{IH}	Active
V_{IH}	V_{IL}	Hi-Z
V_{IL}	V_{IL}	Hi-Z

Output Disable ($\overline{GD}$). In the Asynchronous mode the data outputs DQ0-DQ31 are high impedance when Output Disable $\overline{GD}$ is at V_{IL}, irrespective of the state of Output Enable $\overline{G}$. In Synchronous mode Output Disable $\overline{GD}$ is sampled, together with Output Enable $\overline{G}$, on the rising edge of the System Clock CLK. If Output Disable is at V_{IL} then the data outputs DQ0-DQ31 are high impedance at the next rising edge of the System Clock CLK, irrespective of the state of Output Enable $\overline{G}$.

Output Disable has a weak pull-up resistor to V_{DDQ} and will assume a high level if not externally connected.

Write Enable ($\overline{W}$). The Write Enable $\overline{W}$ input controls the writing of commands or input data. In the Asynchronous Write mode commands or data are written when Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are at V_{IL}. In the Synchronous Write mode with Chip Enable $\overline{E}$ at V_{IL}, input data is sampled if Write Enable $\overline{W}$ is at V_{IL} on the rising edge of the System Clock CLK.

Load Burst Address ($\overline{LBA}$). In the Asynchronous read/write mode Load Burst Address $\overline{LBA}$ is Don't Care (but if it falls during an asynchronous read then a new read cycle is started). In the Synchronous mode Load Burst Address $\overline{LBA}$ enables latching of the burst starting address for Synchronous read or write. The address is latched on the rising edge of the System Clock CLK if Load Burst Address $\overline{LBA}$ is at V_{IL}.

Write/Read ($\overline{WR}$). Write/Read $\overline{WR}$ is used to control the synchronous write or read mode operations. If Load Burst Address $\overline{LBA}$ is at V_{IL} and Write/Read is at V_{IL} then the rising edge of the System Clock CLK latches a write address. If Write/Read is at V_{IH} then a read address is latched. In asynchronous read and write mode $\overline{WR}$ doesn't affect the status of the device.

Write/Read has a weak pull-up resistor to V_{DDQ} and will assume a high level if not externally connected.

Burst Address Advance ($\overline{BAA}$). When Burst Address Advance $\overline{BAA}$ is at V_{IL}, the rising edge of the System Clock CLK advances the burst address. When Burst Address Advance $\overline{BAA}$ is at V_{IH} the advance is suspended.

V_{DD} Supply Voltage. The supply V_{DD} provides the power to the internal circuits of the memory. The V_{DD} supply voltage is 4.5 to 5.5V.

V_{DDQ} Input/Output Supply Voltage. The Input/Output supply V_{DDQ} provides the power for the input/outputs of the memory, independent from the supply V_{DD}. The Input/Output supply V_{DDQ} may be connected to the V_{DD} supply or it can use a separate supply of 3.0 to 3.6V.

V_{PP} Program/Erase Supply Voltage. The Program/Erase supply V_{PP} is used for programming and erase operations. The memory normally executes program and erase operations at the supply V_{PP1} voltage levels.

In a manufacturing environment, programming may be speeded up by applying a higher V_{PPH} level to the V_{PP} Program/Erase Supply. This is not intended for extended use. The V_{PPH} supply may be applied for a total of 80 hours maximum and during program and erase for a maximum of 1000 cycles. Stressing the device beyond these limits could damage the device.

When V_{PP} Program/Erase supply is at V_{SS} all blocks are protected from programming or erase. Leaving V_{PP} floating is equivalent to connecting it to V_{SS} due to an internal pull-down circuit.

The overlay block can be entered in read mode only if V_{PP} is in the range from V_{PPL} to V_{PPH}.

Ground (V_{SS} and V_{SSQ}). The Ground V_{SS} is the reference for the internal supply voltage V_{DD}. The Ground V_{SSQ} is the reference for the Input/Output supply V_{DDQ}.

DEVICE OPERATIONS

See Table 5 for Asynchronous or Synchronous Bus Operations.

In the Asynchronous read/write mode the memory is selected with Chip Enable $\overline{E}$ Low. The data outputs are enabled by Output Enable $\overline{G}$ Low or disabled by Output Disable $\overline{GD}$ Low. Data is input by Write Enable $\overline{W}$ Low.

In the Synchronous read/write mode the memory latches addresses and data (input or output) on the rising edge of the System Clock CLK. Burst address latching is enabled by Load Burst Address $\overline{LBA}$ Low with Write/Read $\overline{WR}$ Low for a write cycle or High for a read cycle.

Data outputs are enabled for reading on the rising edge of the System Clock CLK when Output Enable $\overline{G}$ is low. Data is input on the rising edge of the System Clock CLK when Write Enable $\overline{W}$ is Low.

The memory is deselected and in standby mode when Chip Enable $\overline{E}$ is High, and it is reset or in power-down mode when Reset/Power-Down $\overline{RP}$ is Low.

Read. Read operations are used to output the contents of the memory, the Electronic Signature or the Status Register. The data read depends on the previous Instruction given to the memory.

Read operations can be Asynchronous or Synchronous, with a single or burst read. On power-up the device is in Asynchronous read mode, the Instruction Asynchronous/Synchronous Read Toggle ART can be used to enter the Synchronous read mode.

- **Asynchronous Read.** To read a data Double-Word in Asynchronous mode the address inputs must be stable and Chip Enable $\overline{E}$ must be Low during the read cycle. Output Enable $\overline{G}$ must be Low and Output Disable $\overline{GD}$ High. The Load Burst Address $\overline{LBA}$ is Don't Care, but its falling edge will start a new read cycle.
- **Synchronous Single Read.** To read a single data Double-Word in Synchronous mode Chip Enable $\overline{E}$ must be Low. Load Burst Address $\overline{LBA}$ must be Low for one System Clock CLK rising edge with Write/Read $\overline{WR}$ High. This latches the read address, after which the address bus inputs are Don't Care. The Output Enable $\overline{G}$ is

Low for a single System Clock CLK cycle. The Double-Word of valid data is output on the next System Clock CLK rising edge.

– **Synchronous Burst Read.** To read a burst of four Double-Words in Synchronous mode Chip Enable $\overline{E}$ must be Low. Load Burst Address $\overline{LBA}$ must be Low for one System Clock CLK rising edge with Write/Read $\overline{WR}$ High. This latches the first address of the burst sequence, after which the address bus inputs are Don't Care. The Output Enable $\overline{G}$ is driven Low before the burst output sequence. Four Double-Words of data are output on the subsequent System Clock CLK rising edges if Burst Address Advance $\overline{BAA}$ is maintained Low. The address advance for synchronous burst read is suspended if Burst Address Advance $\overline{BAA}$ goes High and the output data remains constant. The data bus will go high impedance on the rising edge of the System Clock CLK after Output Enable $\overline{G}$ goes High or $\overline{GD}$ goes Low.
The burst timing depends on the device configuration for the Critical Word X and Burst Word Y latency times. The operation burst wrap is shown in Table 12. The wrap sequence uses only the address bits A0 and A1 and does not repeat after the last Double-Word has been output.
Critical Word X (3 or 4) is defined as the number of clock periods that occours from the address latching to the data strobe.
Burst Word Y (1 or 2) is the number of clock period(s) occourring from one data valid to the next (see Figure 5).

Read Overlay Block. The Overlay block can be read, as for a Main block, after it has been enabled. To enable the Overlay block the Overlay Block Enable bit OBEB and the Overlay Block Status bit OBS in the Status Register must be set to '1' (see Table 10).

The Overlay Block Enable bit OBEB can be set to '1' in three ways (see Table 11):

– By Toggling the Reset/Power-Down signal $\overline{RP}$ with the V_{PP} Program/Erase supply in the range V_{PP1} or V_{PPH}. V_{PP} out of range will reset the OBEB bit to '0'.

– By a leaving power-on reset with V_{PP} Program/Erase supply in the range V_{PP1} or V_{PPH}. V_{PP} out of range will reset the OBEB bit to '0'.

– By giving the Overlay Block Enable/Disable for Read Instruction OBT.

The Overlay Block Status bit OBS monitors the V_{PP} Program/Erase supply and will be set to '1' when in the range V_{PP1} or V_{PPH}. The Overlay block is enabled with OBEB at '1' but will not be read unless OBS status bit is also at '1'. If it is not then a read operation will read the contents of the Main block 0 at the same address.

When the Overlay block is enabled for reading, only this one block of 256 Kbit is accesible and none of the other Main blocks may be accessed, the address signals A13-A17 are Don't Care.

Read Electronic Signature. The memory contains three Electronic Signature codes identifying the manufacturer, device and version, which can be read after giving the Instruction RSIG. The manufacturer code 00000020h is read when the address inputs A0 and A1 are at V_{IL}. The device code 000000F0h is read when A0 is at V_{IH} and A1 is at V_{IL}. The version code 0000000xh is read when A0 is at V_{IL} and A1 is at V_{IH}. The codes are read on DQ0-DQ31, all other address signal inputs are Don't Care. See Table 6.

Write. Write operations are used to give commands to the memory that latch input data and addresses to program or block addresses to erase.

– **Asynchronous Write.** To write data in the Asynchronous mode the address inputs must be stable and Chip Enable $\overline{E}$ must be Low during the write cycle. Write $\overline{W}$ must be Low and input data valid on the rising edge of Write $\overline{W}$.

– **Synchronous Write.** To write input data in Synchronous mode Chip Enable $\overline{E}$ must be Low. Load Burst Address $\overline{LBA}$ must be Low for one System Clock CLK rising edge with Write/Read $\overline{WR}$ Low. This latches the write address, after which the address bus inputs are Don't Care. When Write Enable $\overline{W}$ is Low input data is latched on the next System Clock CLK rising edge.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High or when the Output Disable $\overline{GD}$ is Low, independent of the level on Output Enable $\overline{G}$.

Standby. The memory is in standby when the P/E.C. is not running, the memory is in read mode and Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

If Chip Enable goes High during a program or erase operation the device enters the standby mode when the internal algorithm has finished.

Reset/Power-down. During power-down all internal circuits are switched off, the memory is deselected and the outputs are high impedance. The memory is in Power-down mode when Reset/Power-down $\overline{RP}$ is Low. The power consumption is reduced to the power-down level, independent of the Chip Enable $\overline{E}$, Load Burst Address $\overline{LBA}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

If Reset/Power-down $\overline{RP}$ is pulled Low during a program or erase operation this is aborted and the memory content is no longer valid.

Table 5. Bus Operations (1,2)

Operation	$\overline{RP}$	CLK	$\overline{E}$	$\overline{LBA}$	$\overline{WR}$	$\overline{W}$	$\overline{GD}$	$\overline{G}$	DQ0-DQ31
Asynchronous Read	V_{IH}	X	V_{IL}	X	X	V_{IH}	V_{IH}	V_{IL}	Data Output
Asynchronous Write	V_{IH}	X	V_{IL}	X	X	V_{IL}	V_{IH}	V_{IH}	Data Input
Synchronous Read	V_{IH}	⎍	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}	V_{IL}	Data Output
Synchronous Address latch Read	V_{IH}	⎍	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	V_{IH}	X
Synchronous Address latch Write	V_{IH}	⎍	V_{IL}	V_{IL}	V_{IL}	X	V_{IH}	V_{IH}	X
Synchronous Data Write	V_{IH}	⎍	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Data Input
Output Disabled by $\overline{G}$	V_{IH}	X	V_{IL}	X	X	X	V_{IH}	V_{IH}	Hi-Z
Output Disabled by $\overline{GD}$	V_{IH}	X	V_{IL}	X	X	X	V_{IL}	X	Hi-Z
Standby	V_{IH}	X	V_{IH}	X	X	X	X	X	Hi-Z
Reset / Power-down	V_{IL}	X	X	X	X	X	X	X	Hi-Z

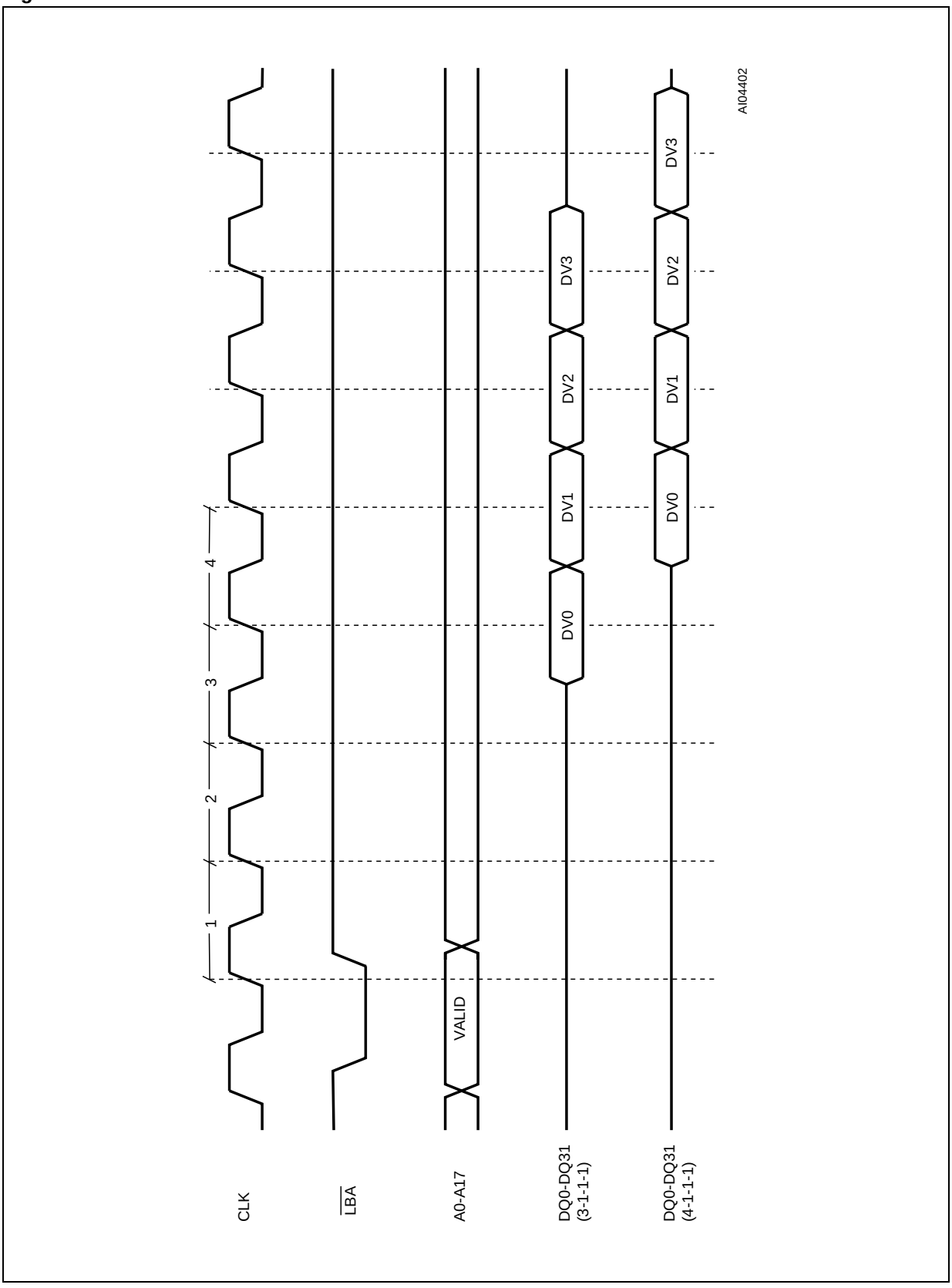
Note: 1. See Device Operations, Instructions and Commands, sections for more details.
2. X=V_{IL} or V_{IH}.

Table 6. Read Electronic Signature

Code	$\overline{RP}$	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A2-A17	DQ0-DQ31
Manufacturer	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Don't Care	00000020h
Device	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	000000F0h
Version	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Don't Care	(Note 1)

Note: "x" = version level. The first version is "0" and it can have a value up to "7".
1. Version code from 0h to 7h.

Figure 5. Burst Latencies 3-1-1-1 and 4-1-1-1



INSTRUCTIONS AND COMMANDS

The Instructions are listed in Tables 7 and 8. They may be broadly divided into two types, those that access or modify the memory content and those that toggle a mode or function.

Table 7. Commands

Code	Command
02h	Overlay Block Erase Set-up
04h	Overlay Block Program Set-up
06h	Overlay Block Read Enable/ Disable
0Dh	Overlay Block Erase Confirm
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
60h	Asynchronous/Synchronous Read Toggle
70h	Read Status Register
90h	Read Electronic Signature
B0h	Program/Erase Suspend
D0h	Program/Erase Resume or Erase Confirm
FFh	Read Memory Array

The Instructions that access or modify the memory content include:

– Read Memory Array (RD)
– Read Status Register (RSR) and Clear Status Register (CLRS)
– Read Electronic Signature (RSIG)
– Erase (EE) and Overlay Block Erase (OBEE)
– Program (PG) and Overlay Block Program (OB-PG)
– Program or Erase Suspend (PES) and Program or Erase Resume (PER)

The Instructions that toggle a mode or function include:

– Asynchronous/Synchronous Read mode Toggle (ART)
– Overlay Block Enable/Disable function Toggle (OBT)

Instructions are written, in one or more write cycles, to the memory Command Interface (C.I.) for decoding. The Command Interface is reset to Read Memory Array at power-up, when exiting from power-down. Any invalid sequence of commands will also reset the Command Interface to Read Memory Array.

A Program/Erase Controller (P/E.C.) handles all the timing and verifies the correct execution of the Program or Erase instructions. The P/E.C. has a Status Register which monitors the operations and which may be read at any time during program or erase. The Status Register bits indicate the operation and exit status of the internal algorithms.

The V_{PP} Program and Erase Supply Voltage must be within the range V_{PP1} or V_{PPH} for programming or erasure. If V_{PP} out of range, the program or erase algorithms do not start and Status Register bit V_{PP} Status V_{PPS} will be set to '1'.

Read Memory Array (RD). The Read Memory Array instruction consists of one write cycle giving the command FFh at the address 00000h. Subsequent read operations will read the addressed location and output the memory data. The data can be read from the Main memory Array or the Overlay memory block if it is enabled.

Read Status Register (RSR). The Read Status Register instruction consists of one write cycle giving the command 70h at the address 00000h. Subsequent read operations will output the Status Register contents. See Table 9 for an explanation of the Status Register bits. The Status Register indicates when a program or Erase operation is complete and its success or failure. The Status Register also indicates if the Overlay block is accessible for reading. The Read Status Register instruction may be given at any time, including while a program or erase operation in progress.

Clear Status Register (CLRS). The Clear Status Register instruction consists of one write cycle giving the command 50h at the address 00000h. The Clear Status Register command clears the bits 3, 4 and 5 of the Status Register if they have been set to '1' by the P/E.C. operation. The Clear Status Register command should be given after an error has been detected and before any new operation is attempted. A Read Memory Array command should also be given before data can be read from the memory array.

Read Electronic Signature (RSIG). The Read Electronic Signature instruction consists of a first write cycle giving the command 90h at the address 00000h. This is followed by three read operations at addresses xxxx0h, xxxx1h and xxxx2h which output the manufacturer, device and version codes respectively.

Erase (EE). The Erase instruction consists of two write cycles, the first is the erase set-up command 20h at the address 00000h. This is followed by the

Erase Confirm command D0h written to an address within the block to be erased. If the second is not the Erase Confirm command the Status Register bits 4 and 5 are set to '1' and the instruction aborts. While erasing is in progress only the Read Status Register and Erase Suspend instructions are valid.

Blocks are erased one at a time. An erase operation sets all bits in a block to '1'. The erase algorithm automatically programs all bits to '0' before erasing the block to all '1's.

Read operations output the Status Register after the erase operation has started. The Status Register bit 7 is '0' while the erase is in progress and is set to '1' when it is completed. After completion the Status Register bit 5 is set to '1' if there has been an erase failure.

Erasure should not be attempted when the V_{PP} Program/Erase Supply Voltage is out of the range V_{PP1} or V_{PPH} as the results will be uncertain. The Status Register bit 3 is set to '1' if V_{PP} is not within the allowed ranges when erasing is attempted or if it falls out of the ranges during erase execution.

The erase operation aborts if V_{PP} drops out of the allowed range or if Reset/Power-down $\overline{RP}$ falls to V_{IL}. As data integrity cannot be guaranteed when the erase operation is aborted, the erase must be repeated.

A Clear Status Register instruction must be given to clear the Status Register bits.

Overlay Block Erase (OBEE). The Overlay Block Erase instruction consists of two write cycles, the first is the Overlay block erase set-up command 02h at the address 00000h. This is followed by the Overlay Block Erase Confirm command 0Dh written to an address within the Overlay block. If the second is not the Overlay Block Erase Confirm command the Status Register bit 5 is set to '1' and the instruction aborts. While erasing is in progress only the Read Status Register instruction is valid.

The operation is executed as described for the Erase (EE) instruction of the Main memory array.

A Clear Status Register instruction must be given to clear the Status Register bits.

Program (PG). The Program instruction consists of two write cycles, the first is the program set-up command 40h at the address 00000h. This is followed by a second write cycle to latch the address and data to be programmed. This second command starts the P/E.C. A program operation can be aborted by writing FFFFFFFFh to any address after the program set-up command has been given. While programming is in progress only the Read Status Register and Program Suspend instructions are valid.

Read operations output the Status Register after the program operation has started. The Status Register bit 7 is '0' while programming is in progress and is set to '1' when it is completed. After completion the Status Register bit 4 is set to '1' if there has been a programming failure.

Programming should not be attempted when the V_{PP} Program/Erase Supply Voltage is out of the range V_{PP1} or V_{PPH} as the results will be uncertain. The Status Register bit 3 is set to '1' if V_{PP} is not within the allowed ranges when programming is attempted or if it falls out of the ranges during program execution.

The program operation aborts if V_{PP} drops out of the allowed ranges or if Reset/Power-Down $\overline{RP}$ falls to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the memory block must be erased and programming repeated.

A Clear Status Register instruction must be given to clear the Status Register bits.

Overlay Block Program (OBPG). The Overlay Block Program instruction consists of two write cycles, the first is the program set-up command 04h at the address 00000h. This is followed by a second write cycle to latch the address and data to be programmed. This second command starts the P/E.C.

The operation is executed as described for the Program (PG) instruction of the Main memory array.

While programming of the Overlay block in progress only the Read Status Register instruction is valid.

Program/Erase Suspend (PES). As memory erasure takes of the order of seconds to complete and programming a few microseconds, a Program/Erase Suspend instruction is implemented. Program/Erase Suspend interrupts the operations to allow reading or programming in a block other than one in which program or erase is suspended. A Program/Erase Suspend instruction is accepted only during a Program or Erase instruction. When the Program/Erase Suspend command is written to the Command Interface, the P/E.C. freezes the program or erase operation. The suspended program or erase operation may be restarted by using the Program/Erase Resume instruction. Program/Erase Suspend is not allowed during the Overlay block program/erase operation and the command is ignored.

The Program/Erase Suspend instruction consists of one write cycle giving the command B0h at the address 00000h.

If a program operation is in progress when the instruction is given, the Status Register bits 4 and 6 are set to '1' after it has been suspended. If an erase operation is in progress when the instruction

is given, the Status Register bits 5 and 6 are set to '1' after it has been suspended.

The valid instructions that may be given to the memory while programing is suspended are

– Read Memory Array (RD)
– Read Status Register (RSR)
– Read Electronic Signature (RSIG)
– Program/Erase Resume (PER)

In addition, while erasure is suspended, the Program (PG) instruction may be given.

In Program/Erase Suspend mode the memory can be placed in a pseudo-standby mode by taking Chip Enable /E to VIH to reduce power consumption.

Program/Erase Resume (PER). If a Program/Erase Suspend instruction has previously been executed, then the operation may be resumed by giving the command D0h at the address 00000h.

The Status Register bits 4, 5 and 6 are cleared when program or erase resumes. A Read Memory Array instruction will output the Status Register after program or erase is resumed.

Suggested flow charts for software that uses programming, erasure and program/erase suspend/resume operations are shown in Figures 13, 14, 15 and 16.

Asynchronous/Synchronous Read Toggle (ART).

Asynchronous Read Memory Array is the memory default at power-up or when returning from Power-Down. To read data in Synchronous mode, either single or burst, the Asynchronous/Synchronous Read Toggle instruction must be used.

The Asynchronous/Synchronous Read Toggle instruction consists of one write cycle giving the command 60h at the address 00000h. Two consecutive instructions are not recognised and another Instruction, for example the Read Memory Array, must be given before another Asynchronous/Synchronous Read Toggle will be recognised.

Overlay Block Read Enable/Disable Toggle (OBT). Read operations in the Overlay block can be enabled or disabled using the Overlay Block Read Enable/Disable Toggle instruction. This toggle instruction consists of one write cycle giving the command 06h at the address 00000h. Two consecutive instructions are not recognised.

The Status Register bit 1 (OBEB) is set to '1' when the Overlay block is enabled. Refer to Table 10, 11 for Overlay block access conditions.

Table 8. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address	Data	Operation	Address.	Data
RD	Read Memory Array	1+	Write	00000h	FFh	Read	Read Address	Data Output
RSR	Read Status Register	1+	Write	00000h	70h	Read	X	Status Register
CLRS	Clear Status Register	1	Write	00000h	50h			
RSIG	Read Electronic Signature	1+++	Write	00000h	90h	Read	Signature Address	Electronic Signature
EE	Erase	2	Write	00000h	20h	Write	Block Address	D0h
OBEE	Overlay Block Erase	2	Write	00000h	02h	Write	Overlay Block Address	0Dh
PG	Program	2	Write	00000h	40h	Write	Program Address	Data Input
OBPG	Overlay Block Program	2	Write	00000h	04h	Write	Overlay Block Program Address	Data Input
PES	Program/Erase Suspend	1	Write	00000h	B0h			
PER	Program/Erase Resume	1	Write	00000h	D0h			
ART	Asynch/Synch Read Toggle	1	Write	00000h	60h			
OBT	Overlay Block Read En/Dis Toggle	1+	Write	00000h	06h	Read	Read Address	Data Output

Table 9. Status Register Bits

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	Indicates the P/E.C. status, check during Program or Erase
			'0'	Busy	
PESS	6	Program/Erase Suspend Status	'1'	Suspend	On Program/Erase Suspend instruction both P/ECS and PESS bits are set to '1'. Either ES bit or PS bit is set to '1'. PESS and either ES or PS bits remain at '1' until Erase Resume instruction is given.
			'0'	In Progress or Completed	
ES	5	Erase Status	'1'	Erase Error or Erase Suspend	ES bit is set to '1' if either PESS instruction is given or Erase operation fails. If ES bit is '1', check PESS bit.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error or Program Suspend	PS bit is set to '1' if either PESS instruction is given or Program operation fails. If PS bit is '1', check PESS bit.
			'0'	Program Success	
VPPS	3	V_{PP} Status	'1'	V_{PP} Invalid	VPPS bit is set to '1' if initially V_{PP} is not V_{PPH} nor V_{PP1}, when Program or Erase Instruction are executed.
			'0'	V_{PP} OK	
Reserved	2				
OBEB	1	Overlay Block Enable Bit	'1'	Enabled	OBEB bit is set to '1' when Overlay Block is Enabled.
			'0'	Disabled	
OBS	0	Overlay Block Status	'1'	Activated	OBS bit is set to '1' when OBEB is '1' and V_{PP} is in the range V_{PP1} or V_{PPH}.
			'0'	Not Activated	

Table 10. Read Access to Overlay Block or Main Block

OBEB Status Bit	V_{PP}	OBS Status Bit	Read Access
1	In the range V_{PP1} or V_{PPH}	1	Overlay Block
1	Out of the range V_{PP1} or V_{PPH}	0	Main Block
0	X	0	Main Block
1	Unknown	Not guaranteed	Unknown

Table 11. Overlay Block Enable/Disable Bit (OBEB)

Method	V_{PP}	OBEB Status Bit	
		Prior state of OBEB	Next state of OBEB
Toggle $\overline{RP}$ (1)	In the range V_{PP1} or V_{PPH}	X	1
	Out of the range V_{PP1} or V_{PPH}	X	0
Power-on-reset	In the range V_{PP1} or V_{PPH}	X	1
	Out of the range V_{PP1} or V_{PPH}	X	0
Overlay Block Read Enable/Disable instruction OBT	–	0	1
	–	1	0

Note: 1. Toggle H-L-H for t_{PLPH} minimum.

CONFIGURATION

The M58BF008 is configured during testing which sets the default for the write and burst interface. The settings are:

Write Interface. The write interface permanently configured at factory level to either Asynchronous or Synchronous. Note that the read interface is not affected by this configuration and defaults to Asynchronous read at power-up, it can be toggled to Synchronous read and back using the Asynchronous/Synchronous Read Toggle Instruction.

Critical Word and Burst Word Latency Times. The Critical Word and Burst Word latency times can be set permanently to

– Critical Word Latency Time X = 3 or 4

– Burst Word Latency Time Y = 1 or 2

A burst sequence is described as X-Y-Y-Y.

Table 12. Wrap Burst Sequence

First Burst Address A1-A0	Data Wrap
00	Double-Word 0 ⇒ 1 ⇒ 2 ⇒ 3
01	Double-Word 1 ⇒ 2 ⇒ 3 ⇒ 0
10	Double-Word 2 ⇒ 3 ⇒ 0 ⇒ 1
11	Double-Word 3 ⇒ 0 ⇒ 1 ⇒ 2

POWER CONSUMPTION

The M58BF008 places itself in one of three different modes depending on the status of the control signals which define decreasing levels of current consumption. This minimises the memory power consumption, allowing an overall decrease in the system power consumption without affecting performance. A different recovery time is, however, linked to the different modes - see the AC timing tables.

Active Power mode. When Chip Enable $\overline{E}$ is at V_{IL} and Reset/Power-Down $\overline{RP}$ is at V_{IH} the memory is in Active Power mode. The DC characteristics tables show the current consumption figures.

Standby mode. Refer to the Device Operating section

Power-Down mode. Refer to the Device Operating section.

Power Up. The V_{DD} Supply Voltage, V_{DDQ} Input/Output Supply Voltage and the V_{PP} Program/Erase Supply Voltage can be applied in any order. The memory Command Interface is reset on power-up to Read Memory Array, but a negative transition on Chip Enable $\overline{E}$ or a change of the addresses is required to ensure valid data is output.

Care must be taken to avoid writes to the memory when the V_{DD} Supply Voltage is above V_{LKO} and V_{PP} Program/Erase Supply Voltage powers-up first. Writes can be inhibited by driving either Write Enable $\overline{W}$ or Write/Read $\overline{WR}$ to V_{IH}.

The memory is disabled until Reset/Power-Down $\overline{RP}$ is up to V_{IH}.

SUPPLY RAILS

Normal precautions must be taken for supply rail decoupling. Each device in a system should have the V_{DD}, V_{DDQ} and V_{PP} rails decoupled with a 0.1µF capacitor close to the package pins. PCB track widths should be sufficient to carry the required program and erase currents on the V_{PP} supply.

DC AND AC PARAMETERS

Table 13. AC Measurement Conditions

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0 to V_{DDQ}
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$

Figure 6. AC Testing Input Output Waveform

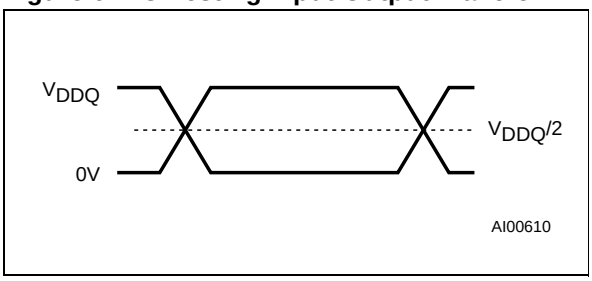


Figure 7. AC Testing Load Circuit

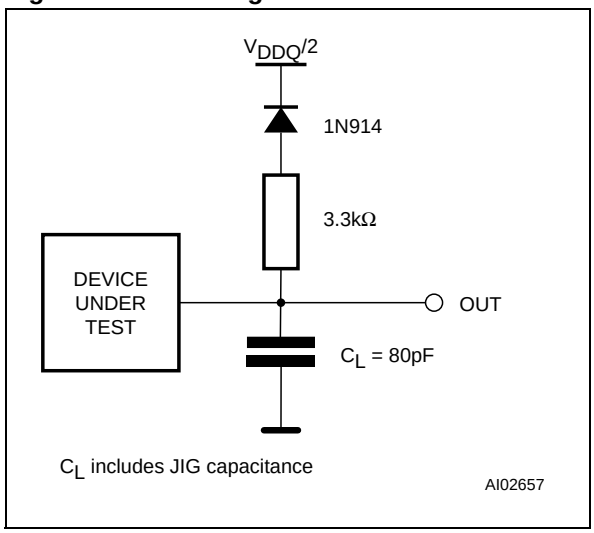


Table 14. Capacitance (1) (T_A = 25 °C, f = 1MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 15. DC Characteristics
(T_A = –40 to 125°C; V_{DD} = 5V ± 10% and V_{DDQ} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$		±10	µA
I_{LT1}	Input Leakage Current pull-up	$0V \le V_{IN} \le V_{DDQ}$	–20	–600	µA
I_{LIVPP}	Input Leakage Current pull-down	$0 \le V_{PP} \le 12.6$		200	µA
I_{CC}	Supply Current (Async. Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		25	mA
I_{CCB}	Supply Current (Burst Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 40MHz		25	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		10	µA
I_{CC2}	Supply Current (Power-down)	$\overline{RP} = V_{IL}$		10	µA
I_{CC3}	Supply Current (Program) Program in Progress	$V_{PP} = V_{PP1}$		25	mA
		$V_{PP} = V_{PPH}$		25	mA
I_{CC4}	Supply Current (Erase) Erase in Progress	$V_{PP} = V_{PP1}$		25	mA
		$V_{PP} = V_{PPH}$		25	mA
I_{PP}	Program Current (Read or Standby)	$V_{PP} \ge V_{PP1}$		200	µA
I_{PP1}	Program Current (Read or Standby)	$V_{PP} \le V_{PP1}$		±15	µA
I_{PP2}	Program Current (Power-down)	$\overline{RP} = V_{IL}$		5	µA
I_{PP3}	Program Current (Program) Program in Progress	$V_{PP} = V_{PP1}$		15	mA
		$V_{PP} = V_{PPH}$		25	mA
I_{PP4}	Program Current (Erase) Erase in Progress	$V_{PP} = V_{PP1}$		15	mA
		$V_{PP} = V_{PPH}$		25	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{DDQ} +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA, $V_{DD} = V_{DD}$ min, $V_{DDQ} = V_{DDQ}$ min		0.2	V
V_{OH}	Output High Voltage	I_{OL} = –100µA, $V_{DD} = V_{DD}$ min, $V_{DDQ} = V_{DDQ}$ min	V_{DDQ} –0.2		V
V_{PP1}	Program Voltage (Program or Erase operations)		4.5	5.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{LKO}	V_{DD} Supply Voltage Lock-out			1.5	V
V_{PPLK}	Program Voltage Lock-out			1.5	V

Figure 8. Asynchronous Read AC Waveforms

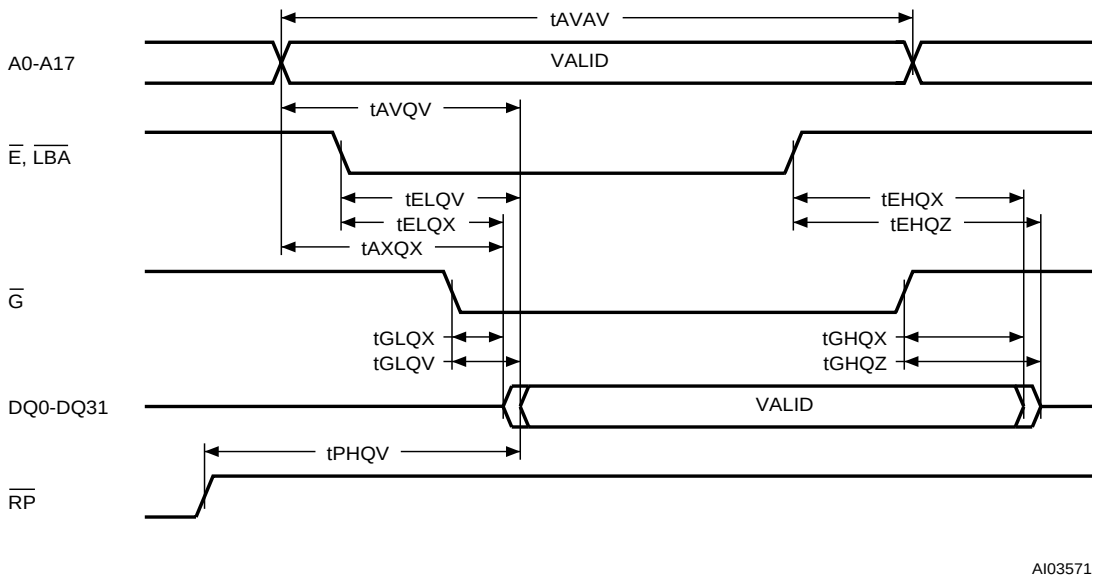
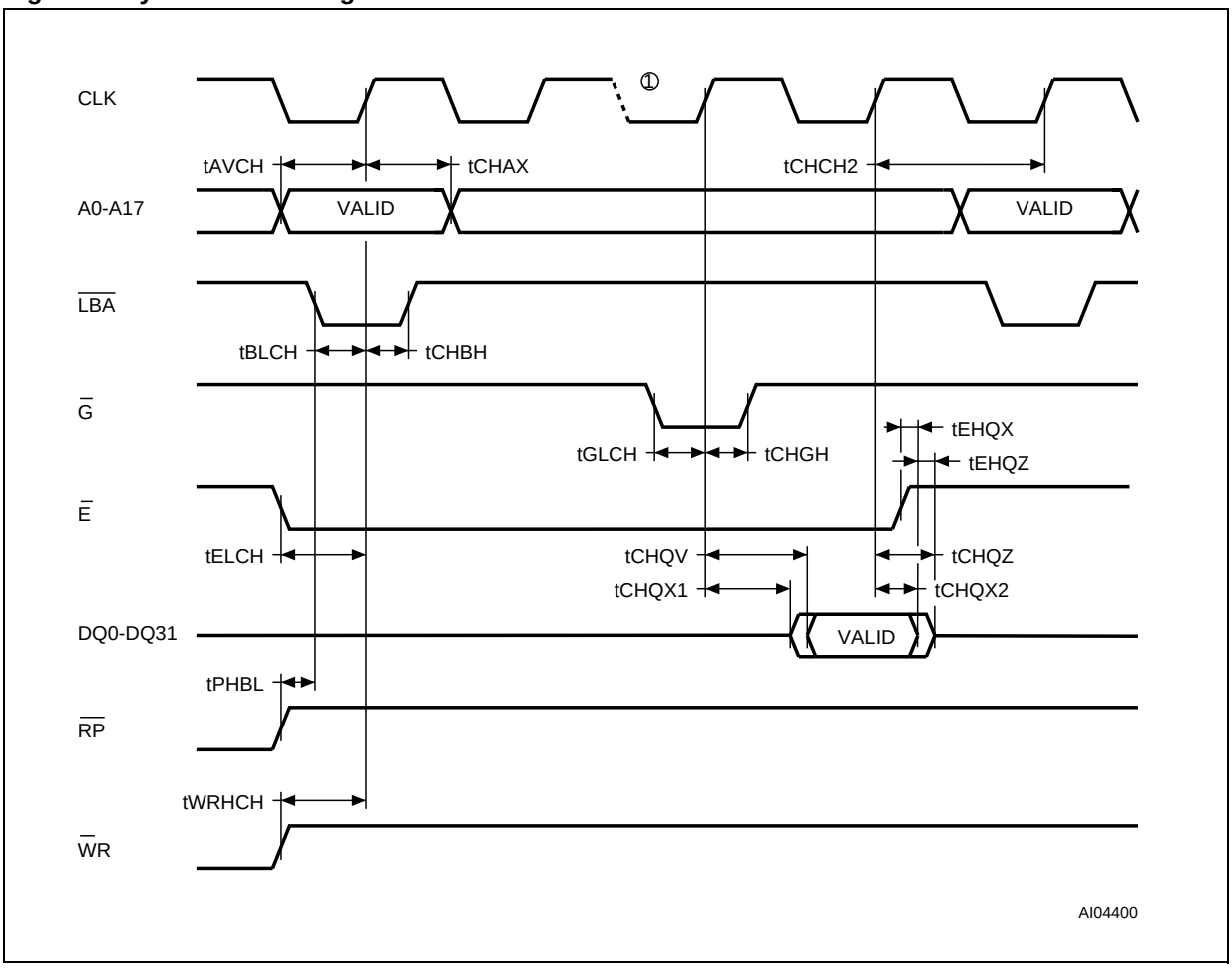


Table 16. Asynchronous Read AC Characteristics (1)
(T_A = –40 to 125°C; V_{DD} = 5V ± 10% and V_{DDQ} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	90		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid		90	ns
t_{AXQX} (2)	t_{OH}	Address Transition to Output Transition	0		ns
t_{EHQX} (2)	t_{OH}	Chip Enable High to Output Transition	0		ns
t_{ELQV} (2, 3)	t_{CE}	Chip Enable Low to Output Valid		90	ns
t_{ELQX} (2)	t_{LZ}	Chip Enable Low to Output Transition	0		ns
t_{EHQZ} (2)	t_{HZ}	Chip Enable High to Output Hi-Z		20	ns
t_{GHQX} (2)	t_{OH}	Output Enable High to Output Transition	0		ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z		25	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid		28	ns
t_{GLQX}	t_{OLZ}	Output Enable Low to Output Transition	0		ns

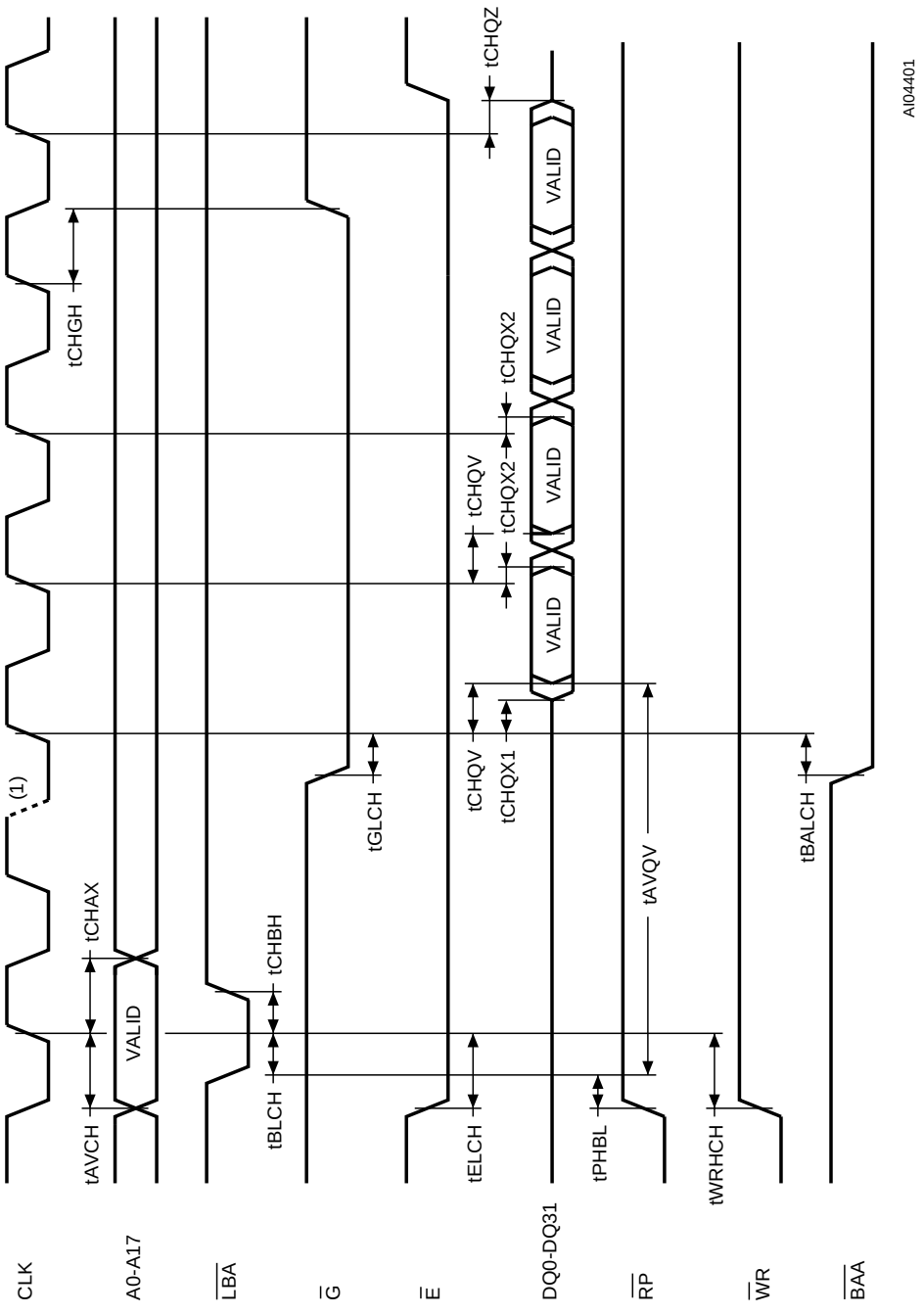
Note: 1. See AC Testing Measurements Conditions for timing measurements.
2. Sampled only, not 100% tested.
3. $\overline{G}$ may be delayed up to t_{ELQV}-t_{GLQV} after falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 9. Synchronous Single Read AC Waveforms



Note: 1. Add one clock period when using 4-1-1-1 read configuration.
2. If GD is at V_{IL} G control is overridden and the data outputs are in HiZ.
3. GD timings are t_{CHGDL} and t_{GDHCH}.

Figure 10. Synchronous Burst Read AC Waveforms



Note: 1. Add one clock period when using 4-1-1-1 read configuration.

Table 17. Synchronous Read AC Characteristics (1)
(T_A = –40 to 125°C; V_{DD} = 5V ± 10% and V_{DDQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit
DC_{CLK}	System Clock Duty Cycle	45	55	%
t_{AVCH} (2)	Address Valid to System Clock High	8		ns
t_{BALCH}	Burst Address Advance Low to System Clock High	8		ns
t_{BLCH} (2)	Load Burst Address Low to System Clock High	8		ns
t_{CHAX} (2)	System Clock High to Address Transition	3		ns
t_{CHBH} (2)	System Clock High to Load Burst Address High	3		ns
t_{CHCH2}	System Clock Data Strobe to Next Address Valid	25		ns
t_{CHCL}	System Clock Fall Time		5	ns
t_{CHGDL} (2)	System Clock High to Output Disable High	5		ns
t_{CHGH} (2)	System Clock High to Output Enable High	5		ns
t_{CHQV} (2)	System Clock High to Data Valid		18	ns
t_{CHQX1} (2)	System Clock High to Data Transition	0		ns
t_{CHQX2} (2)	System Clock High to Data Transition	5		ns
t_{CHQZ} (2)	System Clock High to Data Hi-Z		20	ns
t_{CLCH}	System Clock Rise Time		5	ns
t_{CLCL}	System Clock Period	25		ns
t_{ELCH}	Chip Enable Low to System Clock High	8		ns
t_{GDHCH} (2)	Output Disable Low to System Clock High	10		ns
t_{GLCH} (2)	Output Enable Low to System Clock High	10		ns
t_{PHBL}	Reset/Power-down High to Load Burst Address Low	20		ns
t_{WRHCH}	Write/Read High to System Clock High	8		ns

Note: 1. See AC Testing Measurement Conditions for timing measurements.
2. Sampled only, not 100% tested.

Figure 11. Asynchronous Write AC Waveforms

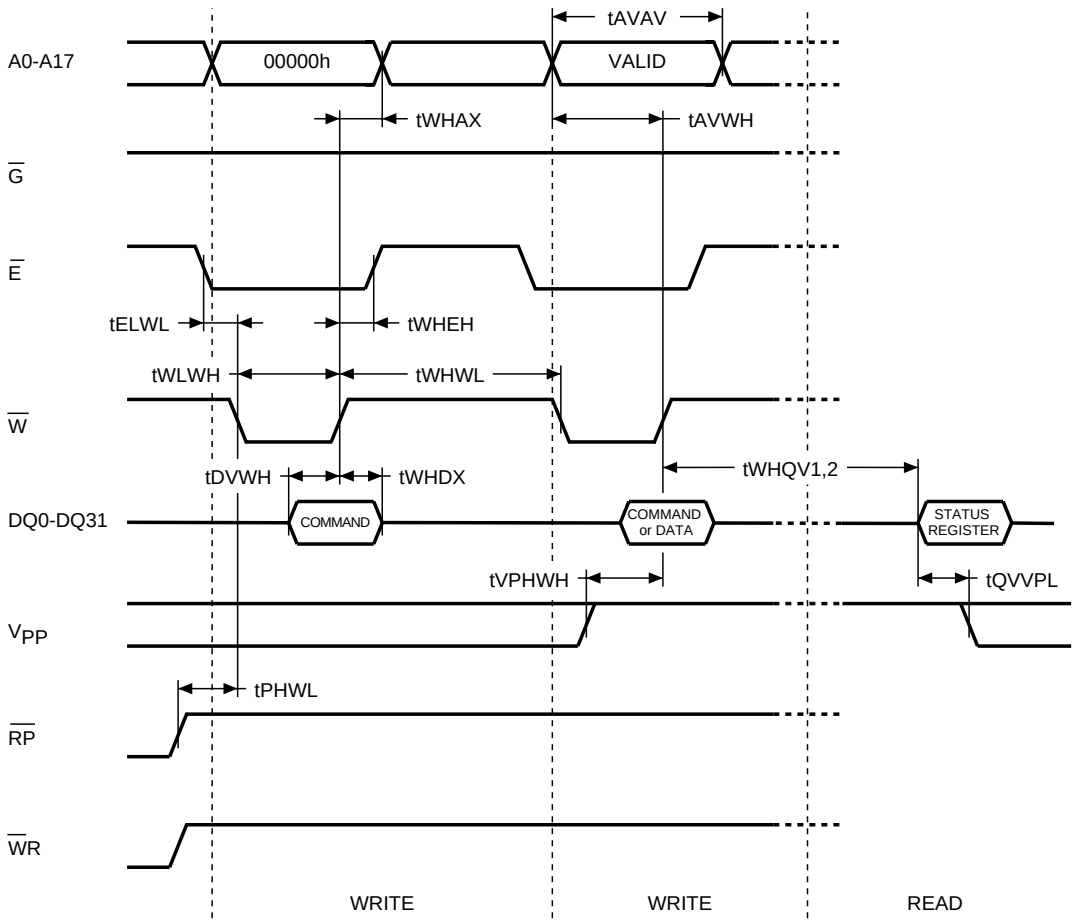


Table 18. Asynchronous Write AC Characteristics (1)
(T_A = –40 to 125°C; V_{DD} = 5V ± 10% and V_{DDQ} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	70		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	70		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	70		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		ns
t_{PHWL}	t_{PS}	Reset/Power-down High to Write Enable Low	70		ns
t_{QVVPL} (2)		Output Valid to V_{PP} out of the range V_{PP1} or V_{PPH}	0		ns
t_{VPHWH} (2)	t_{VPS}	V_{PP} High to Write Enable High	200		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	0		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		ns
t_{WHQV1} (3)		Write Enable High to Output Valid, Program	10		µs
t_{WHQV2} (3)		Write Enable High to Output Valid, Erase	2.1		sec
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	70		ns

Note: 1. See AC Testing Measurement conditions for timing measurements.
2. Sampled only, not 100% tested.
3. Time is measured to Status Register Read giving bit b7 = '1'.

Figure 12. Synchronous Write AC Waveforms

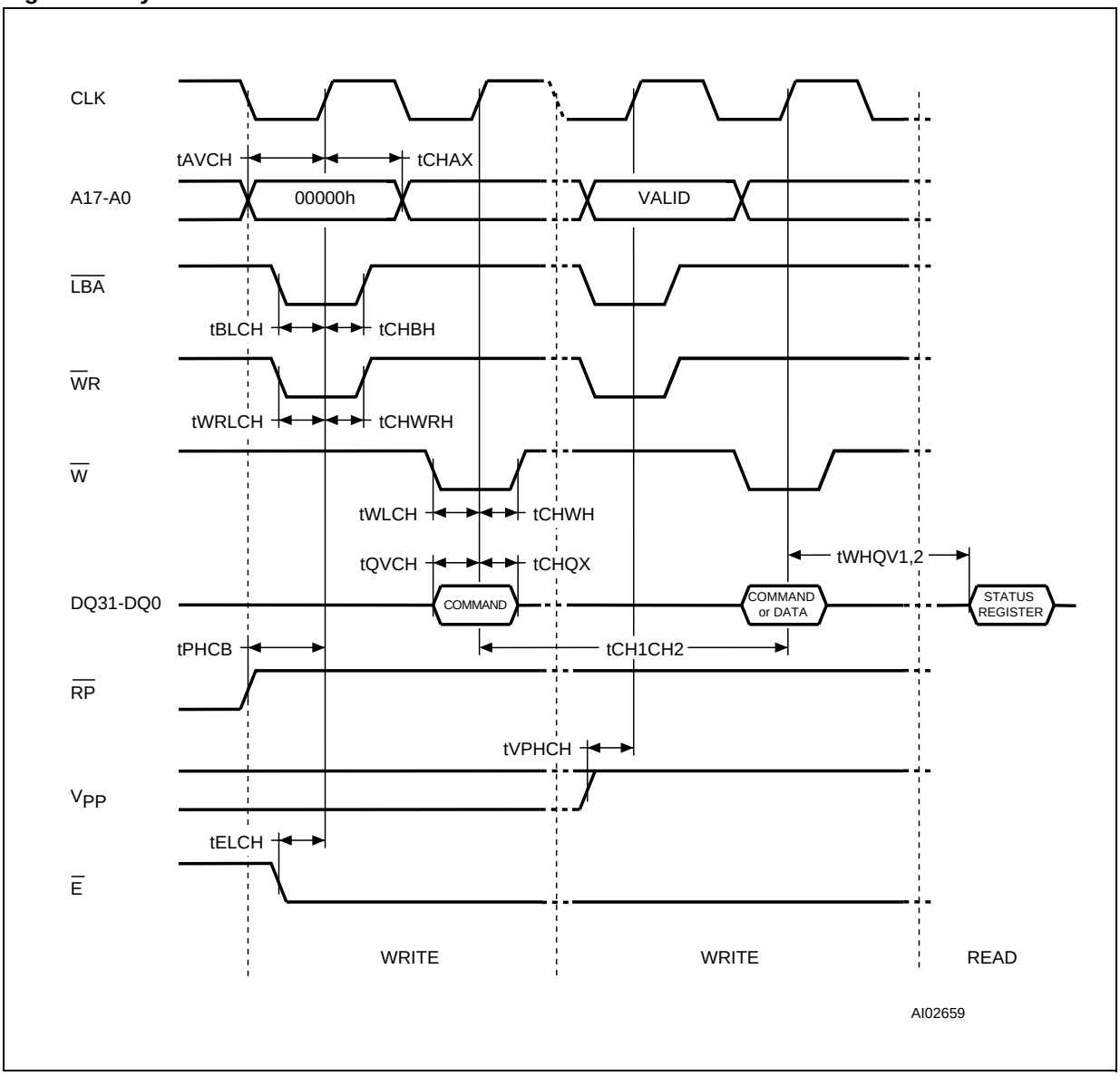


Table 19. Synchronous Write AC Characteristics (1)
(T_A = –40 to 125°C; V_{DD} = 5V ± 10% and V_{DDQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit
DC_{CLK}	System Clock Duty Cycle	45	55	%
t_{AVCH} (2)	Address Valid to System Clock High	8		ns
t_{BLCH} (2)	Load Burst Address Low to System Clock High	8		ns
t_{CH1CH2}	Command to Command	100		ns
t_{CHAX} (2)	System Clock High to Address Transition	3		ns
t_{CHBH} (2)	System Clock High to Load Burst Address High	3		ns
t_{CHCL}	System Clock Fall Time		5	ns
t_{CHQV1} (3)	System Clock High to Output Valid, Program	10		µs
t_{CHQV2} (3)	System Clock High to Output Valid, Erase	2.1		sec
t_{CHQX} (2)	System Clock High to Data Transition	5		ns
t_{CHWH} (2)	System Clock High to Write/Read High	3		ns
t_{CHWRH} (2)	System Clock High to Write Enable High	3		ns
t_{CLCH}	System Clock Rise Time		5	ns
t_{CLCL}	System Clock Period	25		ns
t_{ELCH}	Chip Enable Low to System Clock High	8		ns
t_{PHCH}	Reset/Power-down High to System Clock High		200	ns
t_{QVCH} (2)	Data Valid to System Clock High	8		ns
t_{QVVPL} (2)	Output Valid to V_{PP} out of range V_{PP1} or V_{PPH}	0		ns
t_{VPHCH} (2)	V_{PP} High to System Clock High	200		ns
t_{WLCH} (2)	Write Enable Low to System Clock High	8		ns
t_{WRLCH} (2)	Write/Read Low to System Clock High	8		ns

Note: 1. See AC Testing Measurement conditions for timing measurements.
2. Sampled only, not 100% tested.
3. Time is measured to Status Register Read giving bit b7 = '1'.

Figure 13. Reset/Power-down AC Waveforms

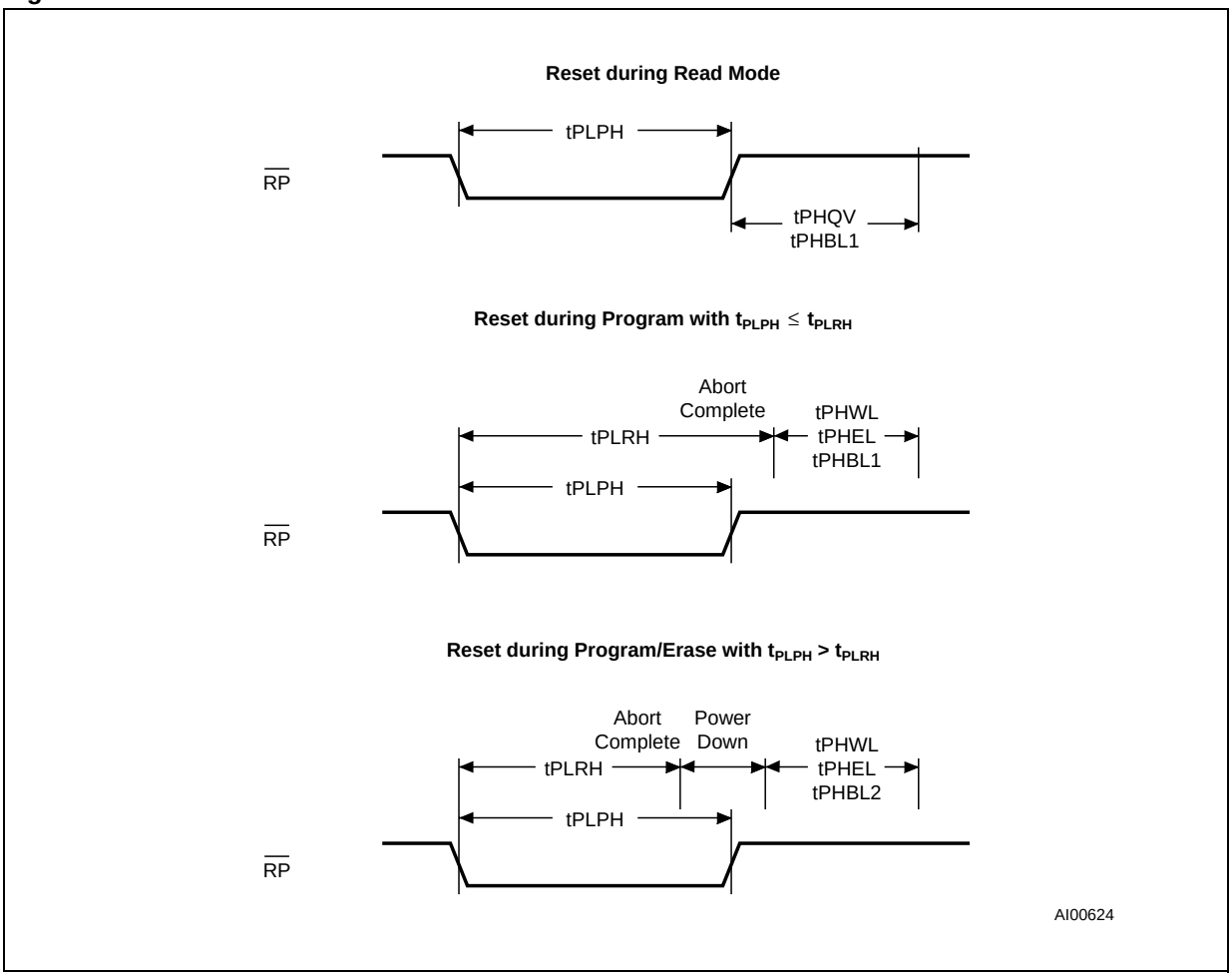


Table 20. Reset/Power-down AC Characteristics
(T_A = –40 to 125°C; V_{DD} = 5V ± 10% and V_{DDQ} = 3.3V ± 0.3V)

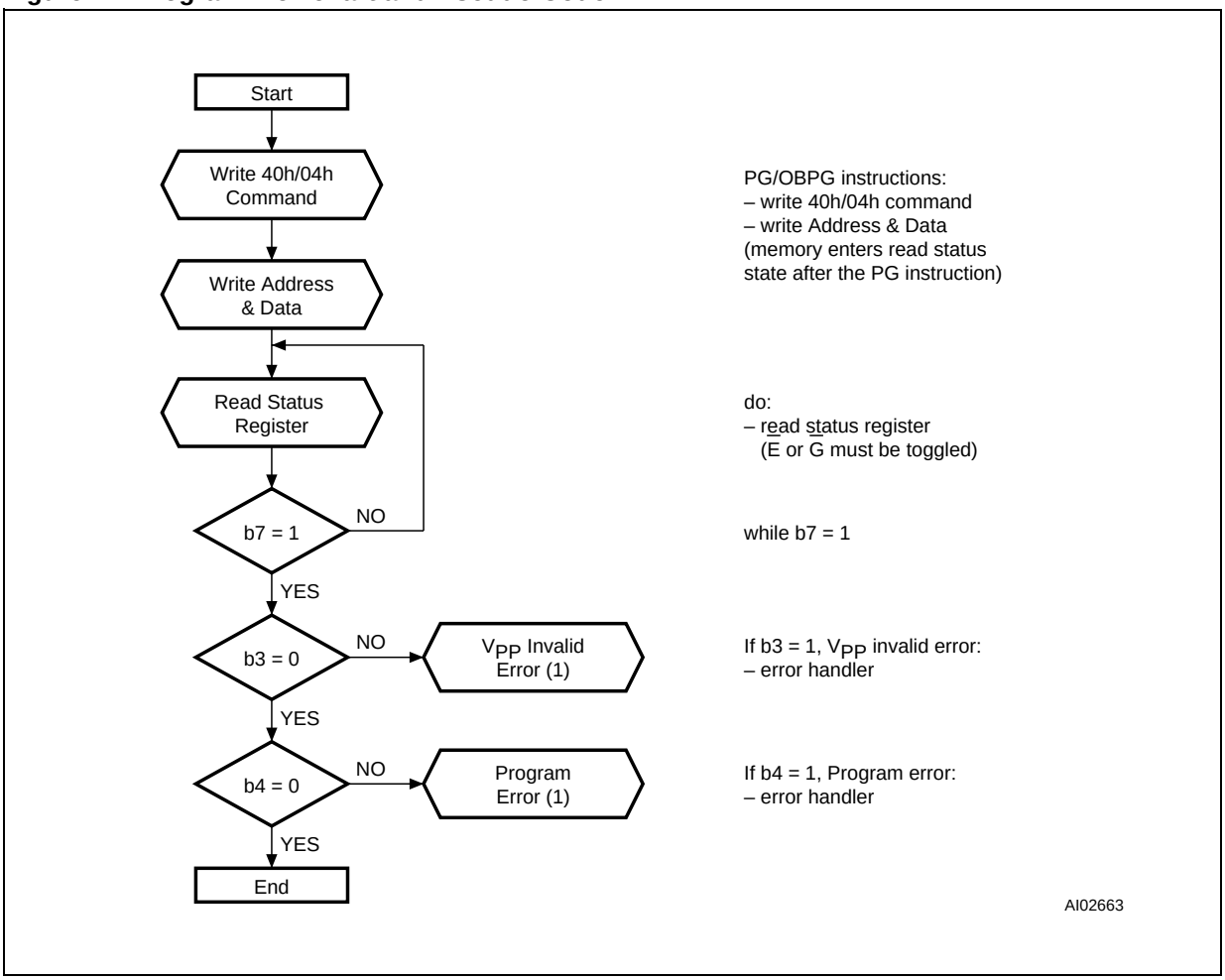
Mode	Symbol	Parameter	Min	Max	Unit
Async	t_{PHEL}	Reset/Power-down High to Chip Enable Low	70		ns
	t_{PHQV}	Reset/Power-down High to Output Valid		100	ns
	t_{PHWL}	Reset/Power-down High to Write Enable Low	70		ns
	t_{PLPH} (1)	Reset/Power-down Pulse Width	100		ns
	t_{PLRH}	Reset/Power-down Low to Program Erase Abort		22	µs
Sync	t_{PHBL1}	Reset/Power-down High to Load Burst Address Low	20		ns
	t_{PHBL2}	Reset/Power-down High to Load Burst Address Low		22	µs

Note: 1. The device Reset is possible but not guaranteed if t_{PLPH} < 100ns.
A Reset will complete within 100ns if $\overline{RP}$ is Low while not in Program or Erase.

Table 21. Program, Erase Times and Program/Erase Endurance Cycles
(T_A = –40 to 125°C; V_{DD} = 5V ± 10% and V_{DDQ} = 3.3V ± 0.3V)

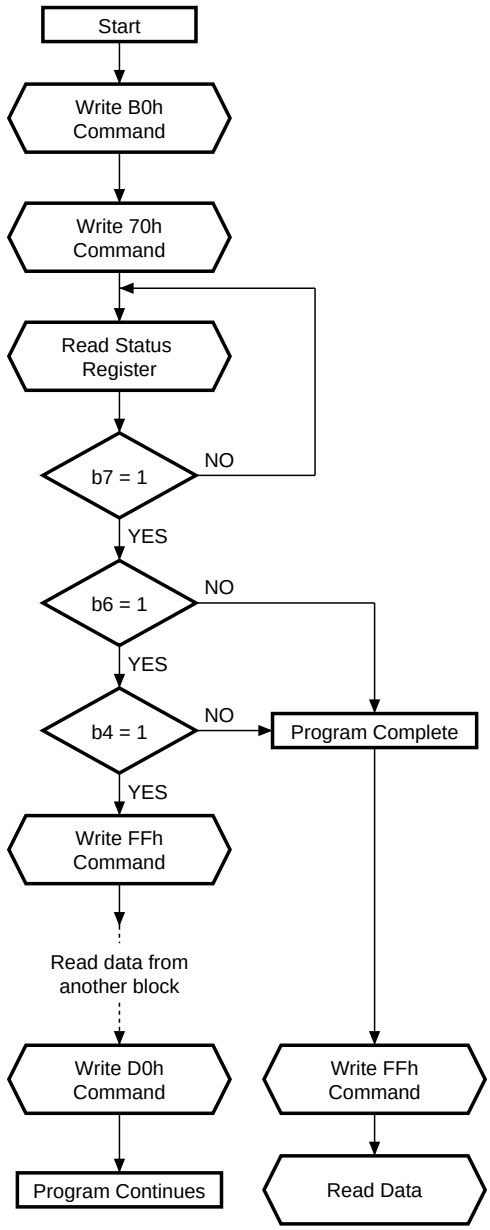
Parameter	Test Conditions	Min	Typ	Max	Unit
Main/Overlay Block Program Time	$V_{PP} = V_{PPH}$		0.14	1.4	sec
	$V_{PP} = V_{PP1}$		0.18	1.8	sec
Main/Overlay Block Erase Time	$V_{PP} = V_{PPH}$		0.21	2.1	sec
	$V_{PP} = V_{PP1}$		0.33	3.3	sec
Program/Erase Cycles (per Block)	$V_{PP} = V_{PPH}$	1,000			cycles
	$V_{PP} = V_{PP1}$	10,000			cycles

Figure 14. Program Flowchart and Pseudo Code



Note: 1. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 15. Program Suspend & Resume Flowchart and Pseudo Code



PES instruction (note 1):
– write B0h command
(memory enters read register state after the PES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

If b4 = 0, Program completed
(at this point the memory will accept only the RD or PER instruction)

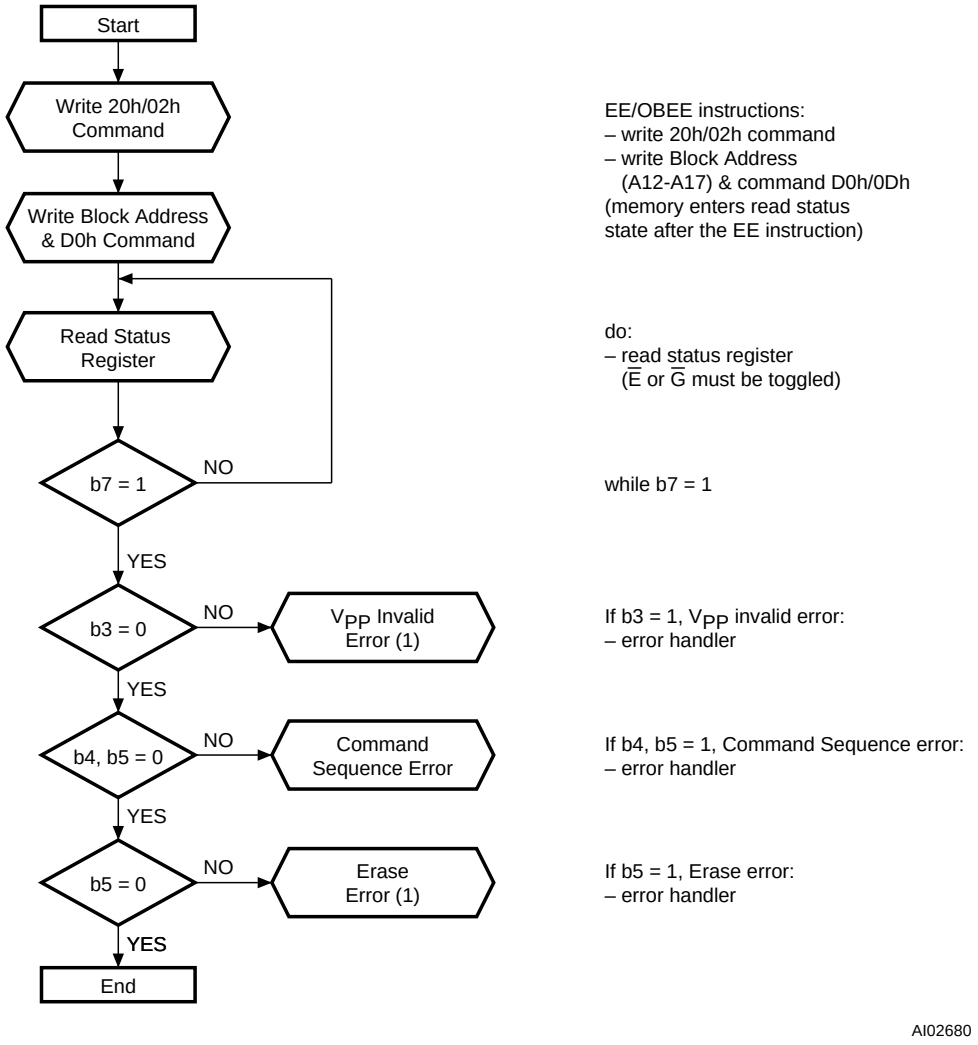
RD instruction:
– write FFh command
– one or more data reads from another block

PER instruction:
– write D0h command to resume erasure
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase suspend was not issued).

AI02664

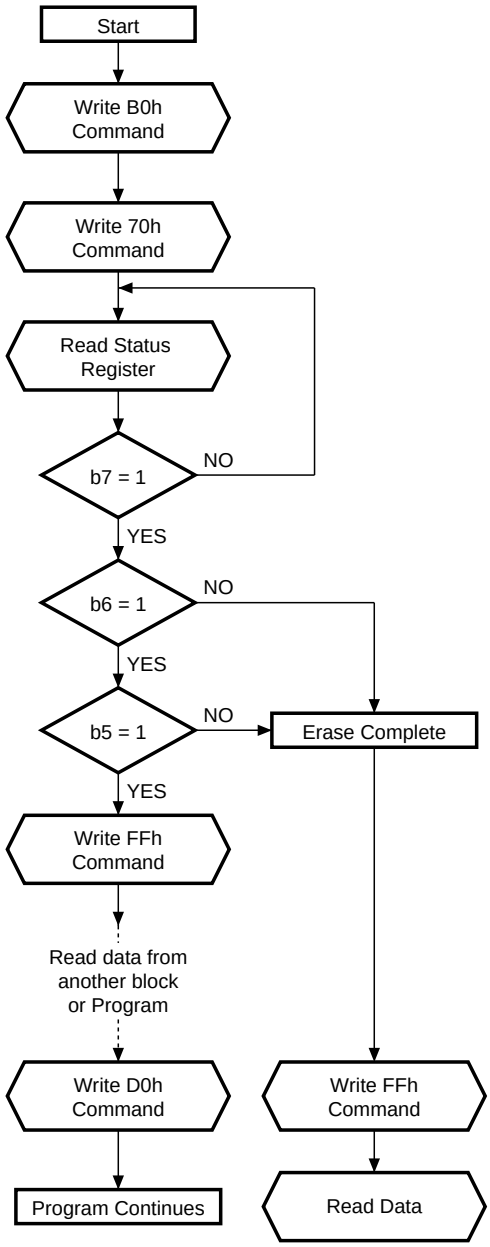
Note: 1. PES instruction is not allowed during OBPG operation.

Figure 16. Erase Flowchart and Pseudo Code



Note: 1. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 17. Erase Suspend & Resume Flowchart and Pseudo Code



PES instruction (note 1):
– write B0h command
(memory enters read register state after the PES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

If b6 = 0, Erase completed
(at this point the memory wich accept only the RD or PER instruction)

RD instruction:
– write FFh command
– one o more data reads from another block

PG instruction:
– write 40h command
– write Address & Data

PER instruction:
– write D0h command to resume erasure
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase suspend was not issued).

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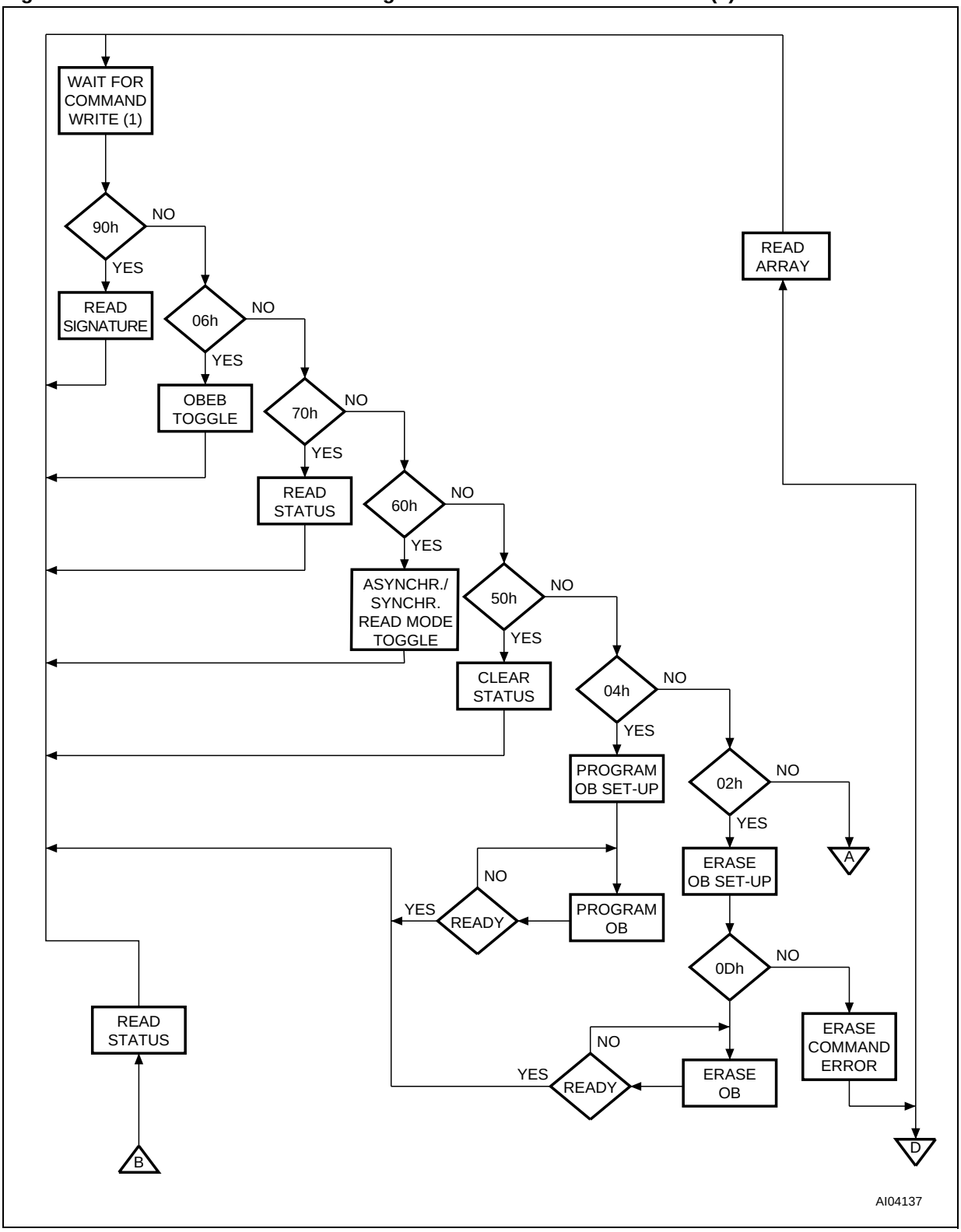
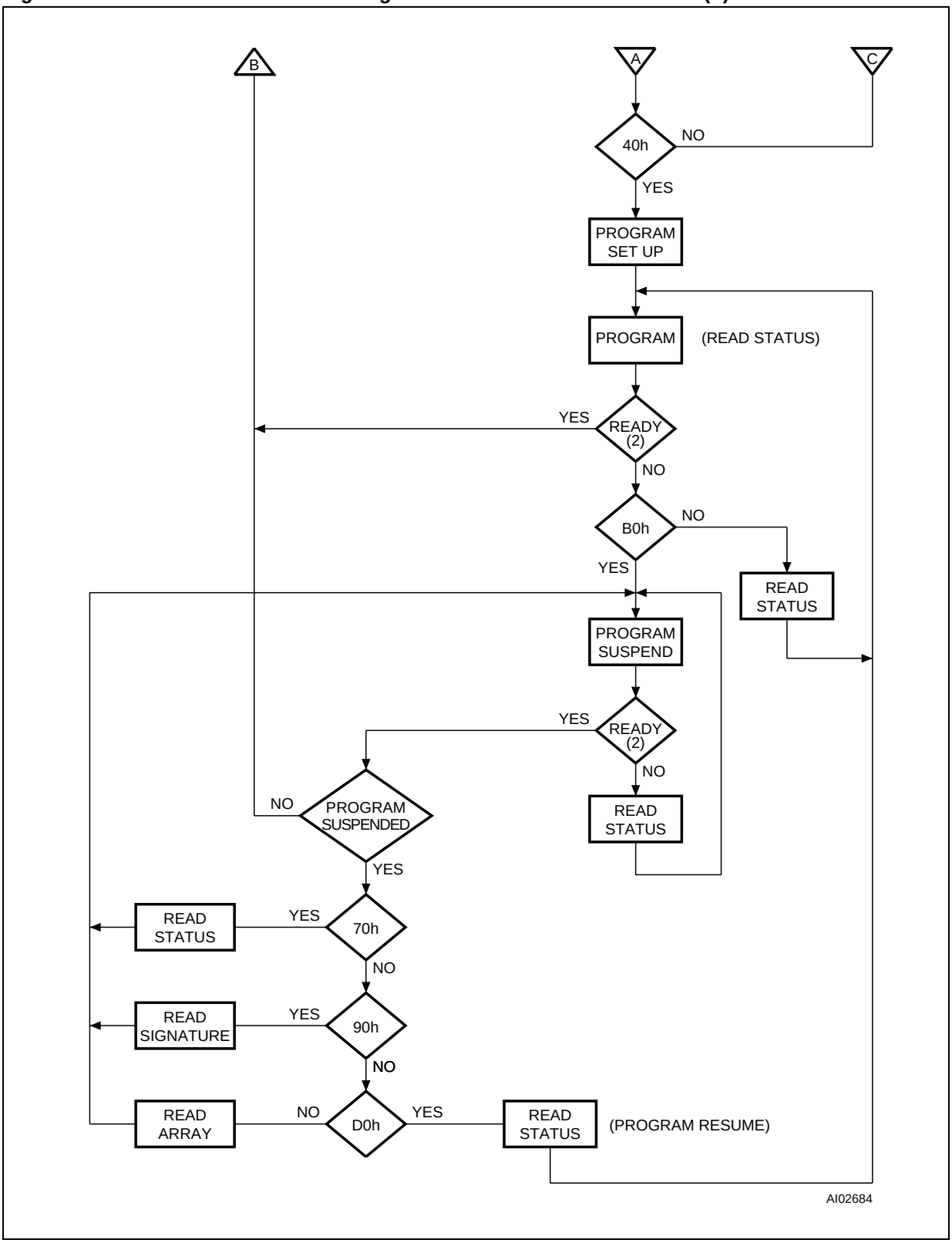
Note: 1. PES instruction is not allowed during OBEE operation.

Figure 18. Command Interface and Program Erase Controller Flowchart (a)



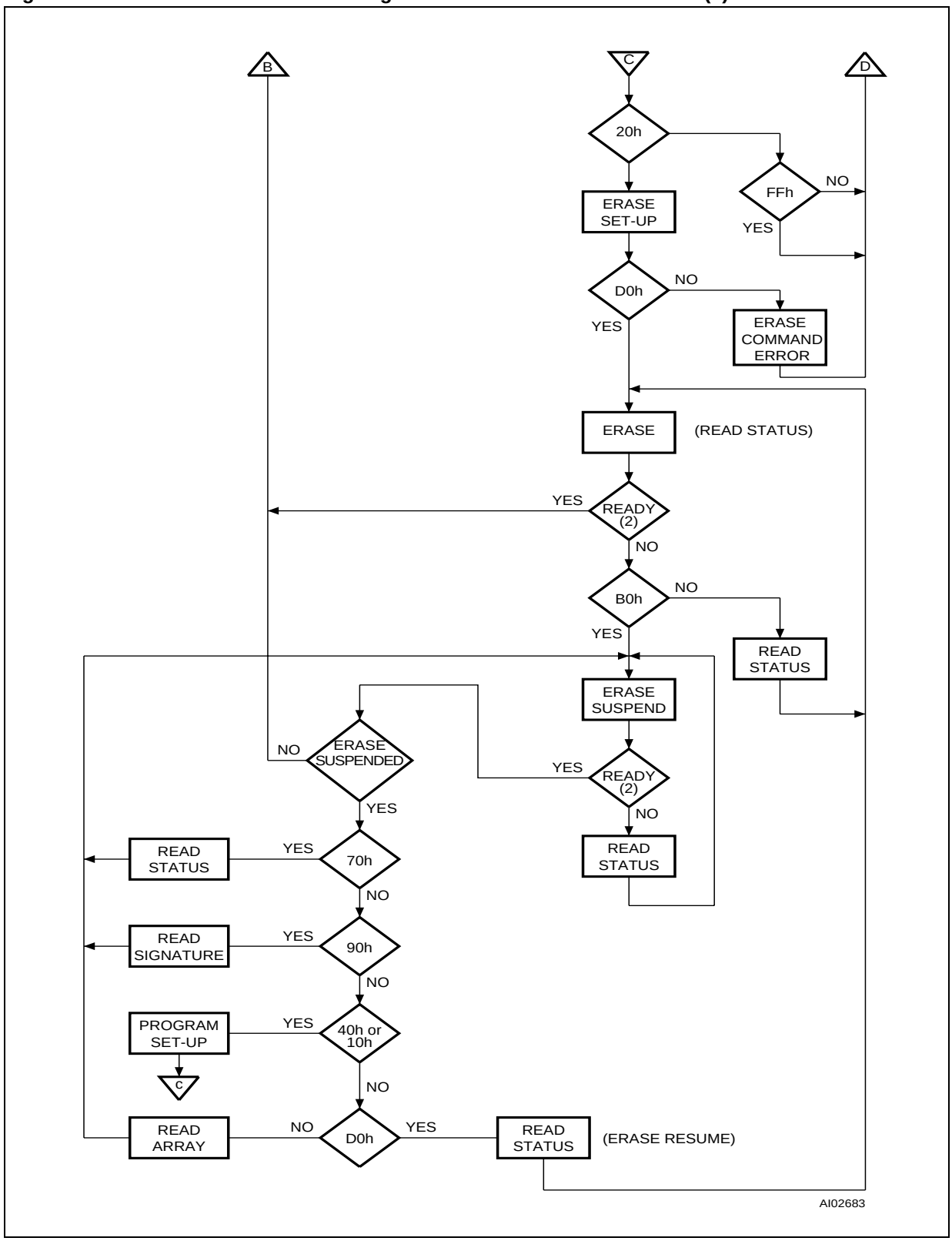
Note: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{DD} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 19. Command Interface and Program Erase Controller Flowchart (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 20. Command Interface and Program Erase Controller Flowchart (c)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

PART NUMBERING

Table 22. Ordering Information Scheme

Example: M58BF008B 100 ZA 3 T

Device Type
M58

Architecture
B = Burst Mode

Operating Voltage
F = V_{DD} = 5V ± 10%; V_{DDQ} = 3.0V or 3.6V

Device Function
008 = 8 Mbit (x32), Burst

Configuration
B = Synchronous Write, Burst Wrap,
Critical Word Latency = 3
Burst Word Latency = 1

D = Synchronous Write, Burst Wrap,
Critical Word Latency = 4
Burst Word Latency = 1

Speed
90 = 90ns

Package
T = PQFP80
ZA = LBGA80: 1.0 mm pitch

Temperature Range
3 = –40 to 125 °C

Option
T = Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Configuration, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

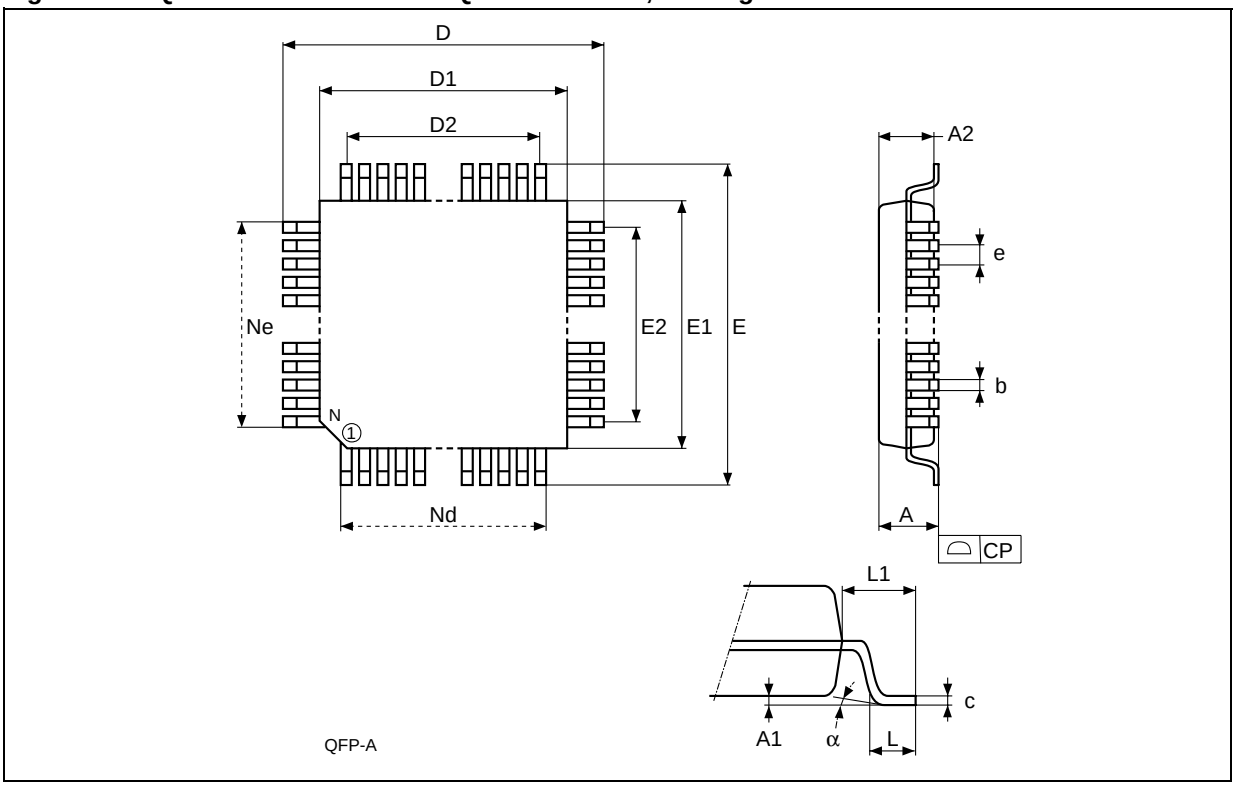
REVISION HISTORY

Table 23. Document Revision History

Date	Version	Revision Details
January 2001	-01	First Issue
11-Jul-2001	-02	From Target Specification to Preliminary Data

PACKAGE MECHANICAL

Figure 21. PQFP80 - 80 lead Plastic Quad Flat Pack, Package Outline

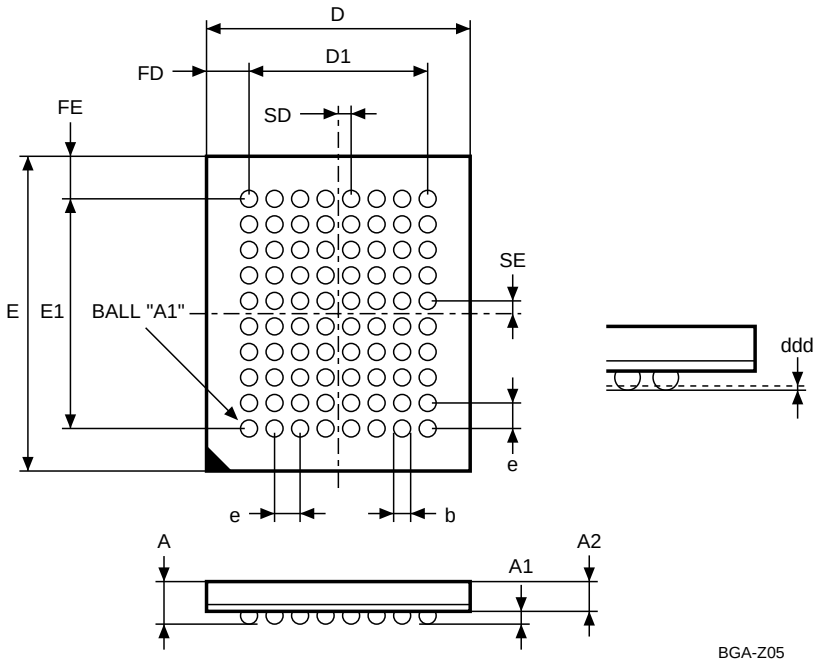


Note: Drawing is not to scale.

Table 24. PQFP80 - 80 lead Plastic Quad Flat Pack, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.40			0.1339
A1		0.25			0.0098	
A2	2.80	2.55	3.05	0.1102	0.1004	0.1201
b		0.30	0.45		0.0118	0.0177
c		0.11	0.23		0.0043	0.0091
D	23.90	–	–	0.9409	–	–
D1	20.00	–	–	0.7874	–	–
e	0.80	–	–	0.0315	–	–
E	17.90	–	–	0.7047	–	–
E1	14.00	–	–	0.5512	–	–
L	0.88	0.73	1.03	0.0346	0.0287	0.0406
α	3.5 °	0 °	7 °	3.5 °	0 °	7 °
N	80			80		
Nd	24			24		
Ne	16			16		
CP			0.250			0.0098

Figure 22. LBGA80 - 10 x 8 ball array, 1mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 25. LBGA80 - 10 x 8 ball array, 1mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.700			0.0669
A1	0.400	0.350	0.450	0.0157	0.0138	0.0177
A2	1.100			0.0433		
b	0.500	–	–	0.0197	–	–
D	10.000	–	–	0.3937	–	–
D1	7.000	–	–	0.2756	–	–
ddd			0.150			0.0059
E	12.000	–	–	0.4724	–	–
E1	9.000	–	–	0.3543	–	–
e	1.000	–	–	0.0394	–	–
FD	1.500	–	–	0.0591	–	–
FE	1.500	–	–	0.0591	–	–
SD	0.500	–	–	0.0197	–	–
SE	0.500	–	–	0.0197	–	–