



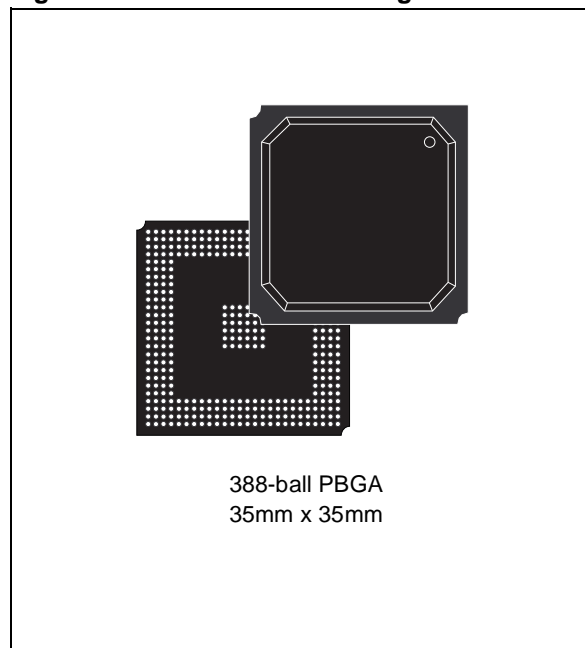
64K x 72-bit Entry NETWORK PACKET SEARCH ENGINE

DATA BRIEFING

FEATURES SUMMARY

- 64K DATA ENTRIES IN 72-BIT MODE
- TABLE MAY BE PARTITIONED INTO UP TO EIGHT (8) OCTANTS
(Data entry width in each octant is configurable as 36, 72, 144, or 288 bits.)
- UP TO 100 MILLION SUSTAINED SEARCHES PER SECOND IN 72-BIT and 144-BIT CONFIGURATIONS
- UP TO 50 MILLION SEARCHES PER SECOND IN 36-BIT and 288-BIT CONFIGURATIONS
- SEARCHES ANY SUB-FIELD IN A SINGLE CYCLE
- OFFERS BIT-BY-BIT and GLOBAL MASKING
- SYNCHRONOUS, PIPELINED OPERATION
- UP TO 31 SEARCH ENGINES CASCADABLE WITHOUT PERFORMANCE DEGRADATION
- WHEN CASCADED, THE DATABASE ENTRIES CAN SCALE FROM 496K TO 3968K DEPENDING ON THE WIDTH OF THE ENTRY
- GLUELESS INTERFACE TO INDUSTRY-STANDARD SRAMS
- SIMPLE HARDWARE INSTRUCTION INTERFACE
- IEEE 1149.1 TEST ACCESS PORT
- OPERATING SUPPLY VOLTAGES INCLUDE:
 V_{DD} (Operating Core Supply Voltage) = 1.5V for 66 and 83MSPS; 1.65V for 100MSPS
 V_{DDQ} (Operating Supply Voltage for I/O) = 2.5 or 3.3V
- 388 PBGA, 35mm x 35mm

Figure 1. 388-ball PBGA Package



DESCRIPTION

Overview

ST Microelectronics, Inc.'s M7040N Search Engine incorporates patent-pending Associative Processing Technology™ (APT) and is designed to be a high-performance, pipelined, synchronous, 64K-entry network database search engine. The M7040N database entry size can be 72 bits, 144 bits, or 288 bits. In the 72-bit entry mode, the size of the database is 64K entries. In the 144-bit mode, the size of the database is 32K entries, and in the 288-bit mode, the size of the database is 16K entries. The M7040N is configurable to support multiple databases with different entry sizes. The 36-bit entry table can be implemented using the Global Mask Registers (GMRs) building-database size of 128K entries with a single device.

Performance

The Search Engine can sustain 100 million transactions per second when the database is programmed or configured as 72 or 144 bits. When the database is programmed to have an entry size

of 36 or 288 bits, the Search Engine will perform at 50 million transactions per second. STM's M7040N can be used to accelerate network protocols such as Longest-prefix Match (CIDR), ARP, MPLS, and other Layer 2, 3, and 4 protocols.

Applications

This high-speed, high-capacity Search Engine can be deployed in a variety of networking and communications applications. The performance and features of the M7040N make it attractive in applications such as Enterprise LAN switches and routers and broadband switching and/or routing equipment supporting multiple data rates at OC-48 and beyond. The Search Engine is designed to be scalable in order to support network database sizes to 3968K entries specifically for environments that require large network policy databases. Figure 4, page 5 shows the block diagram for the M7040N device.

Table 1. Product Range

Part Number	Operating Supply Voltage	Operating I/O Voltage	Speed	Temperature Range
M7040N-100ZA1	1.65V	2.5 or 3.3V	100MHz	Commercial
M7040N-083ZA1	1.5V	2.5 or 3.3V	83MHz	Commercial
M7040N-066ZA1	1.5V	2.5 or 3.3V	66MHz	Commercial

Figure 2. Switch/Router Implementation Using the M7040N

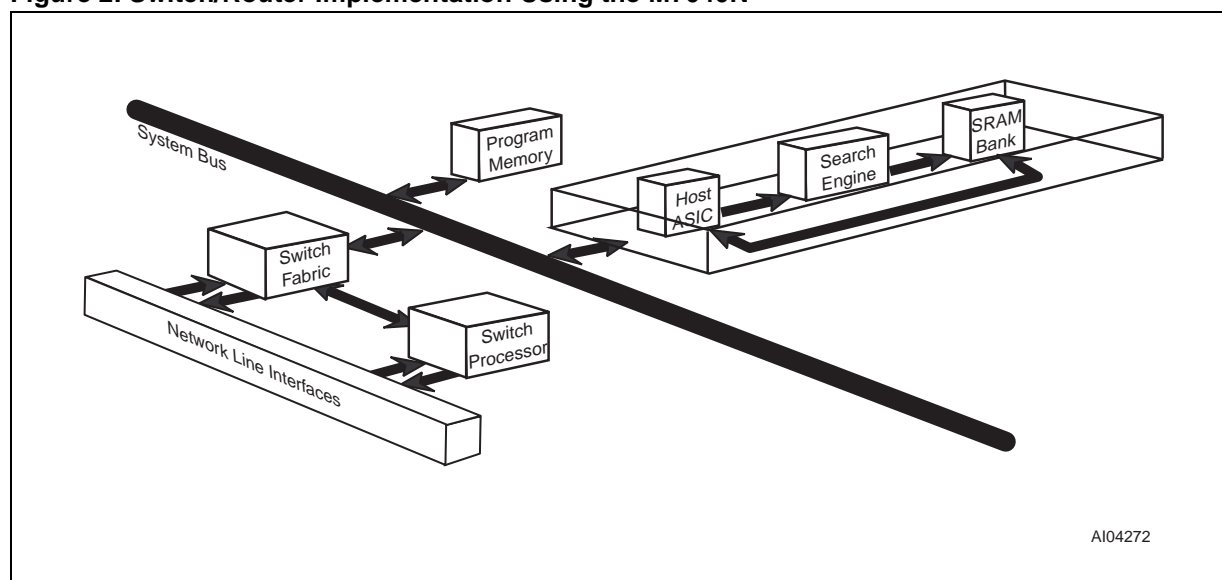


Table 2. Signal Names

Symbol	Type ⁽¹⁾	Description
Clocks and Reset		
CLK_MODE	I	Clock Mode
CLK2X_CLK1X	I	Master Clock
PHS_L	I	Phase
TEST_CO ⁽²⁾	I	Test Output (ST Use Only)
TEST	I	Test Input (ST Use Only)
TEST_FM	I	Test Input (ST Use Only)
RST_L	I	Reset
TEST_PB ⁽³⁾	I	Test Input (ST Use Only)
CFG_L	I	Configuration
Command and DQ Bus		
CMD[10:0]	I	Command Bus
CMDV	I	Command Valid
DQ[71:0]	I/O	Address/Data Bus
ACK ⁽⁴⁾	T	READ Acknowledge
EOT ⁽⁴⁾	T	End of Transfer
SSF	T	SEARCH Successful Flag
SSV	T	SEARCH Successful Flag Valid
MULTI_HIT	O	Multiple Hit Flag
HIGH_SPEED	I	100MHz Indicator
CLKTUNE[3:0]	I	PLL Tuner

SRAM Interface		
SADR[23:0]	T	SRAM Address
CE_L	T	SRAM Chip Enable
WE_L	T	SRAM Write Enable
OE_L	T	SRAM Output Enable
ALE_L	T	Address Latch Enable
Cascade Interface		
LHI[6:0]	I	Local Hit In
LHO[1:0]	O	Local Hit Out
BHI[2:0]	I	Block Hit In
BHO[2:0]	O	Block Hit Out
FULI[6:0]	I	Full In
FULO[1:0]	O	Full Out
FULL	O	Full Flag
Device Identification		
ID[4:0]	I	Device Identification
Supplies		
V _{DD}	n/a	Chip Core Supply (1.5V for 66 and 83MSPS; 1.65 for 100MSPS)
V _{DDQ}	n/a	Chip I/O Supply (2.5 or 3.3V)
Test Access Port		
TDI	I	Test Access Port's Test Data In
TCK	I	Test Access Port's Test Clock
TDO	T	Test Access Port's Test Data Out
TMS	I	Test Access Port's Test Mode Select
TRST_L	I	Test Access Port's Reset

- Note: 1. Signal types are: I = Input only; I/O = Input or Output; O = Output; and T = Tristate
 See DESCRIPTIONS FOR CONNECTION DIAGRAM (Figure 3, page 9), page 152 for individual connection details.
 2. In the previous versions of this specification, this signal was called, "CLK_OUT."
 3. In previous versions of this specification, this signal was called, "PLL_BYPASS."
 4. ACK and EOT Signals require a weak, external pull-down resistor of 47 K Ω or 100 K Ω .

Figure 3. Connections

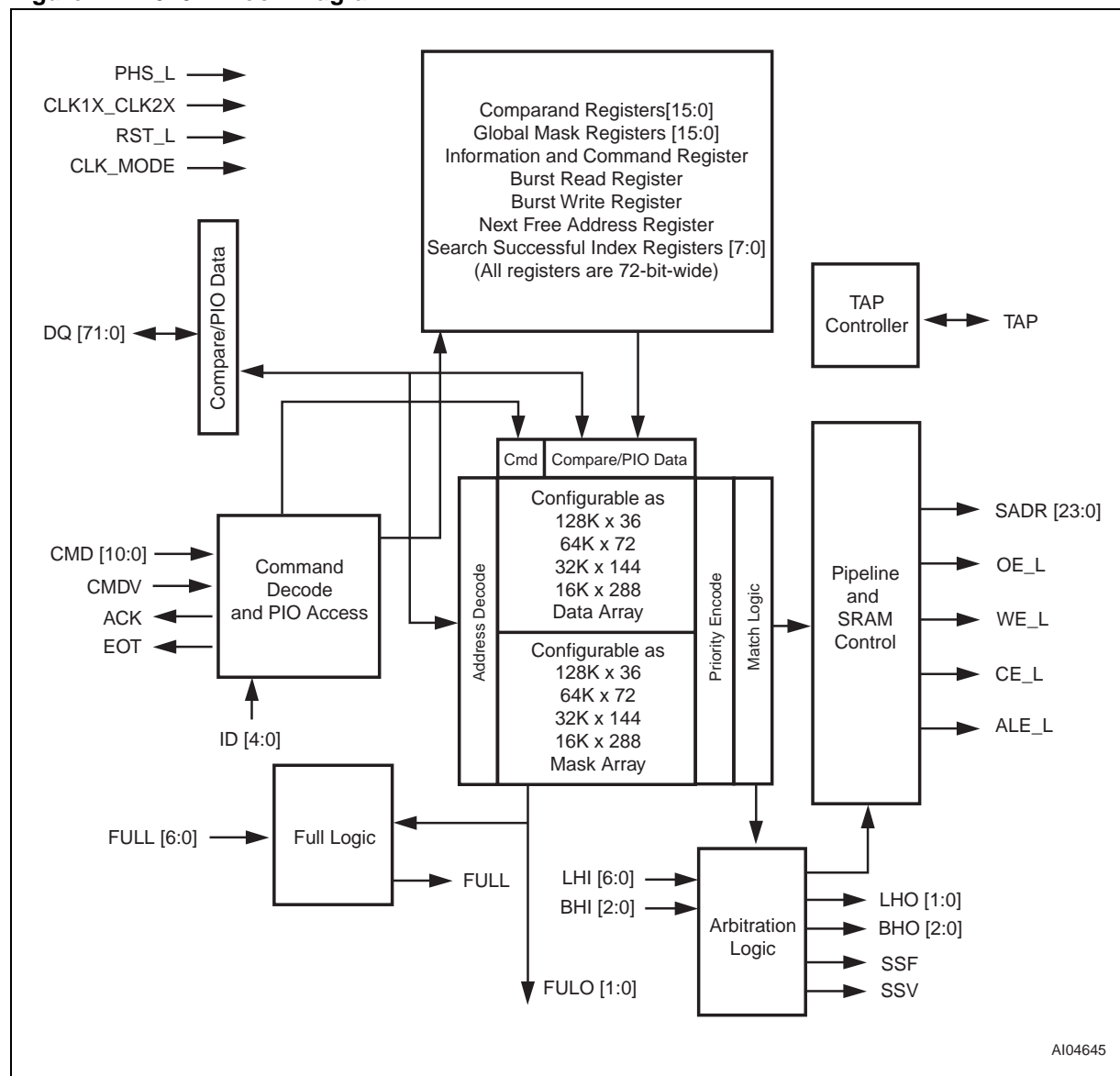
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	CLK_TUNE3	DQ71	VDDQ	DQ67	DQ63	VDDQ	DQ57	DQ53	DQ51	DQ43	DQ41	DQ37	DQ35	DQ31	VDDQ	DQ25	DQ21	DQ17	VDDQ	DQ9	DQ5	DQ3	TEST_FM	VDDQ	HIGH_SPEED	CLK_TUNE0	A
B	TDI	VSS	DQ69	DQ65	DQ61	DQ59	DQ55	VDDQ	DQ47	DQ45	DQ39	VDDQ	DQ33	DQ29	DQ27	DQ23	VDDQ	DQ15	DQ11	DQ7	VDDQ	DQ1	TEST_PB	CFG_L	VSS	SADR_0	B
C	TCK	TMS	VDD	VDD	VDD	VDD	NC8	DQ49	VDDQ	VDD	VDD	VDD	VDD	VDD	VDD	DQ19	DQ13	NC7	VDD	VDD	VDD	VDD	VDD	VDD	SADR_1	VDDQ	C
D	TRST_L	TDO	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	SADR_3	SADR_2	D
E	ID0	VDDQ	VDD	VSS																			VSS	VDD	SADR_5	SADR_4	E
F	ID1	ID2	VDD	VSS																			VSS	VDD	SADR_6	VDDQ	F
G	ID3	ID4	VDD	VSS																			VSS	VDD	SADR_8	SADR_7	G
H	LHI0	LHI1	NC1	VSS																			VSS	NC6	VDDQ	SADR_9	H
J	LHI2	LHI3	VDDQ	VSS																			VSS	SADR_11	SADR_12	SADR_10	J
K	LHI6	LHI4	LHI5	VSS																			VSS	SADR_13	VDDQ	SADR_14	K
L	LHO0	LHO1	VDD	VDD																			VDD	VDD	SADR_15	SADR_16	L
M	VDDQ	BHI0	VDD	VDD																			VDD	VDD	VDDQ	SADR_17	M
N	BHI1	BHI2	VDD	VDD																			VDD	VDD	SADR_19	SADR_18	N
P	BHO0	MULTI_HIT	VDD	VDD																			VDD	VDD	SADR_21	SADR_20	P
R	VDDQ	BHO1	VDD	VDD																			VDD	VDD	SADR_22	VDDQ	R
T	BHO2	VSS	VDD	VDD																			VDD	VDD	CLK_MODE	SADR_23	T
U	FULI0	VDDQ	FULI1	VSS																			VSS	OE_L	PHS_L	CLK1w/CLK2x	U
V	FULI2	FULI3	FULI4	VSS																			VSS	CE_L	VDDQ	WE_L	V
W	VDDQ	FULI5	NC2	VSS																			VSS	NC5	CMDV	ALE_L	W
Y	FULI6	FULO0	VDD	VSS																			VSS	VDD	CMD1	CMD0	Y
AA	FULO1	VDDQ	VDD	VSS																			VSS	VDD	CMD3	CMD2	AA
AB	FULL	ACK	VDD	VSS																			VSS	VDD	CMD5	CMD4	AB
AC	VSS	EOT	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	CMD6	VDDQ	AC
AD	RST_L	VDDQ	VDD	VDD	VDD	VDD	NC3	VDDQ	DQ46	VDD	VDD	VDD	VDD	VDD	VDD	VDD	DQ20	DQ16	NC4	VDD	VDD	VDD	VDD	VDD	CMD8	CMD7	AD
AE	TEST	VSS	DQ70	VDDQ	DQ64	DQ60	DQ58	DQ54	DQ50	DQ44	DQ42	DQ38	VDDQ	DQ32	DQ28	DQ26	VDDQ	DQ18	DQ12	DQ10	DQ6	VDDQ	DQ0	VDDQ	VSS	CLK_TUNE1	AE
AF	TEST_CO	CLK_TUNE2	DQ68	DQ66	DQ62	VDDQ	DQ56	DQ52	DQ48	VDDQ	DQ40	DQ36	DQ34	DQ30	VDDQ	DQ24	DQ22	DQ14	VDDQ	DQ8	DQ4	DQ2	SSV	SSF	CMD10	CMD9	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS

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Note: This diagram is TOP VIEW perspective (view through package).

Figure 4. M7040N Block Diagram



PART NUMBERING**Table 3. Ordering Information Scheme**

Example:	M70	40	N	-100	ZA	1	T
Device Type							
M70 Search Engine							
Density							
40 = 4.5Mb (64K x 72-bit Table Entries)							
Operating Supply Voltage							
N = $V_{DD} = 1.5V$ for -066 and -083 speed grades $V_{DD} = 1.65V$ for -100 speed grade							
Speed							
-100 = 100 Million Searches per Second -083 = 83 Million Searches per Second -066 = 66 Million Searches per Second							
Package							
PBGA = 388-ball count, 35mm x 35mm ⁽¹⁾ , 1.27mm ball pitch							
Temperature Range							
1 = 0 to 70°C							
Shipping Option							
Tape & Reel Packing = T							

Note: 1. Where "Z" is the symbol for BGA packages and "A" denotes 1.27mm ball pitch

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

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