



STW200NF03

N-CHANNEL 30V - 0.002 Ω - 120A TO-247 ULTRA LOW ON-RESISTANCE STripFET™ II MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STW200NF03	30V	<0.0028 Ω	120A

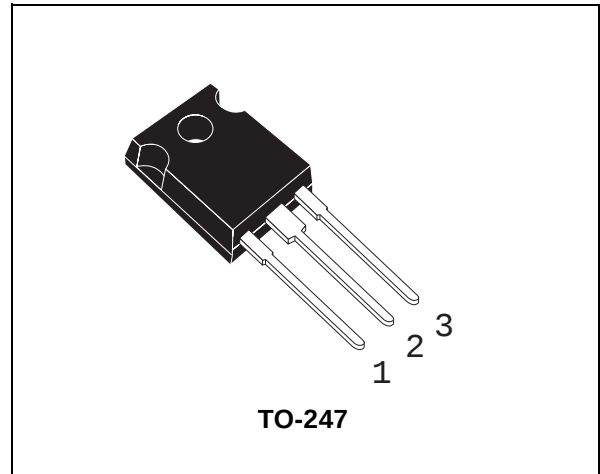
- TYPICAL R_{DS(on)} = 0.002 Ω
- 100% AVALANCHE TESTED

DESCRIPTION

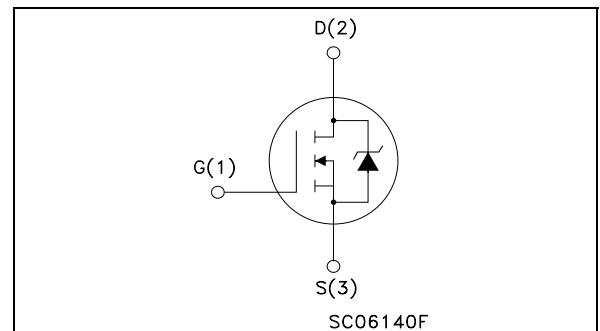
This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is particularly suitable in OR-ing function circuits and synchronous rectification.

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- HIGH CURRENT, HIGH SWITCHING SPEED
- OR-ING FUNCTION



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	30	V
V _{GS}	Gate- source Voltage	± 20	V
I _D (●)	Drain Current (continuous) at T _C = 25°C	120	A
I _D	Drain Current (continuous) at T _C = 100°C	120	A
I _{DM} (●●)	Drain Current (pulsed)	480	A
P _{tot}	Total Dissipation at T _C = 25°C	350	W
	Derating Factor	2.33	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	1.5	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	4	J
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Operating Junction Temperature		

(●●) Pulse width limited by safe operating area.

(●) Current limited by package

(1) I_{SD} ≤ 120A, di/dt ≤ 200A/μs, V_{DD} ≤ V(BR)_{DSS}, T_j ≤ T_{JMAX}.

(2) Starting T_j = 25 °C, I_D = 60 A, V_{DD} = 15V

THERMAL DATA

R _{thj-case}	Thermal Resistance Junction-case	Max	0.43	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	50	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	Typ	300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 60 A		0.002	0.0028	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 15 V I _D = 60 A		200		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		10		nF
C _{oss}	Output Capacitance			3.35		nF
C _{rss}	Reverse Transfer Capacitance			385		pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ $I_D = 60\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		50 300		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=15\text{V}$ $I_D=120\text{A}$ $V_{GS}= 10\text{ V}$ (see test circuit, Figure 4)		210 63.5 63.5	280	nC nC nC

SWITCHING OFF

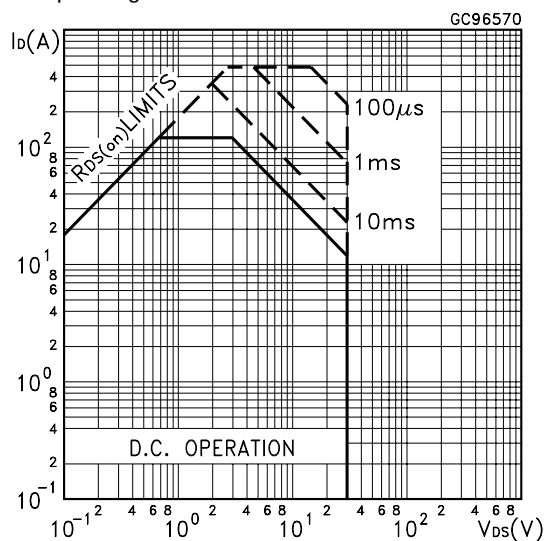
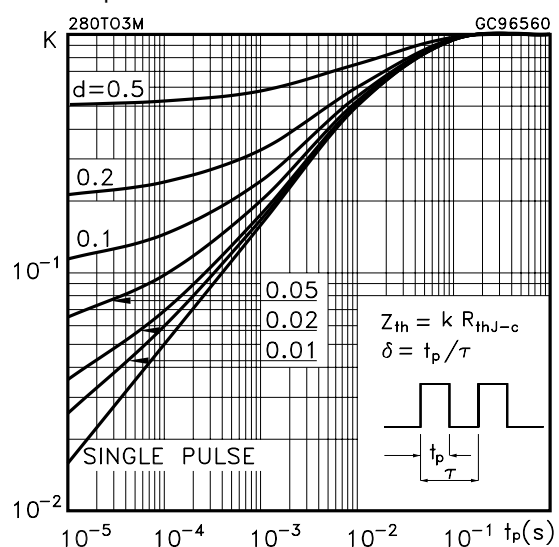
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ $I_D = 60\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		100 80		ns ns

SOURCE DRAIN DIODE

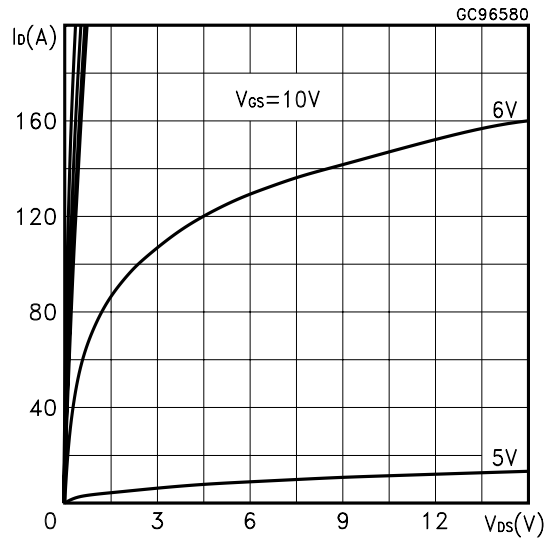
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				120 480	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 120\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 120\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		90 250 5.5		ns nC A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

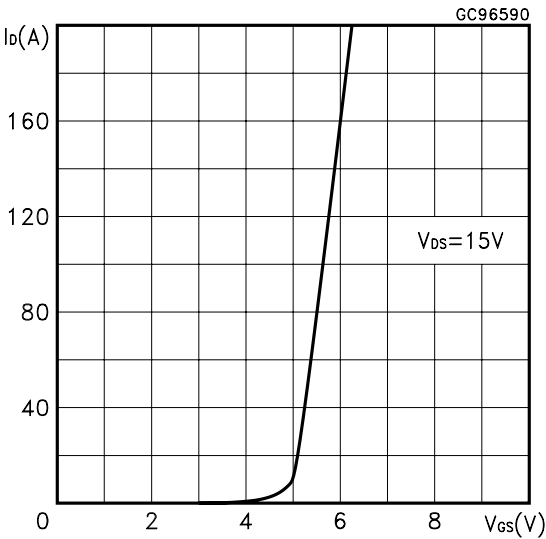
(•) Pulse width limited by safe operating area.

Safe Operating Area**Thermal Impedance**

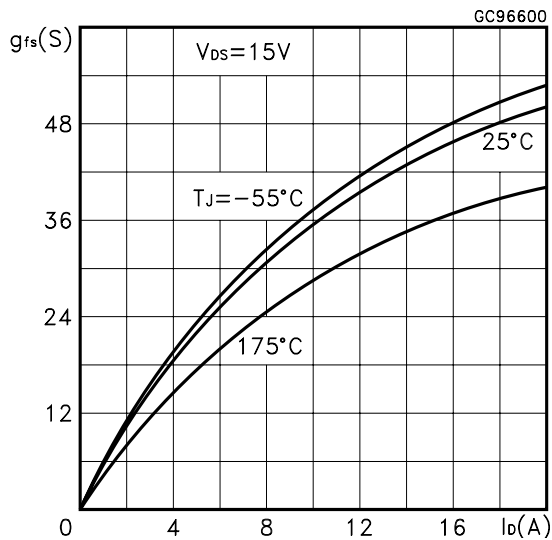
Output Characteristics



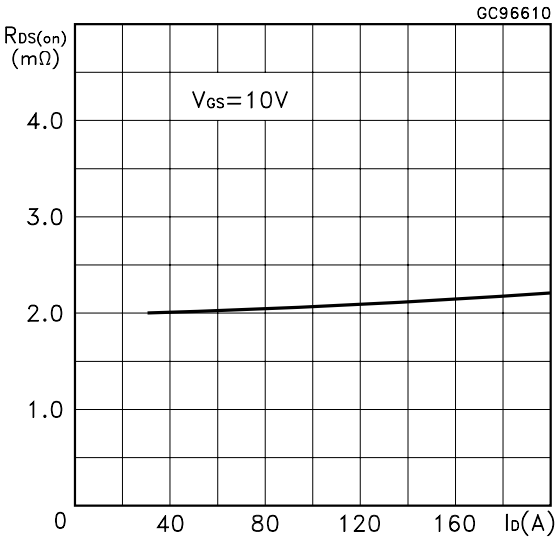
Transfer Characteristics



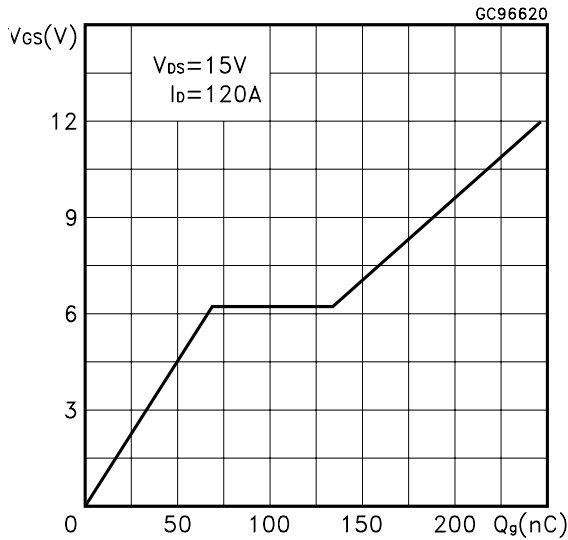
Transconductance



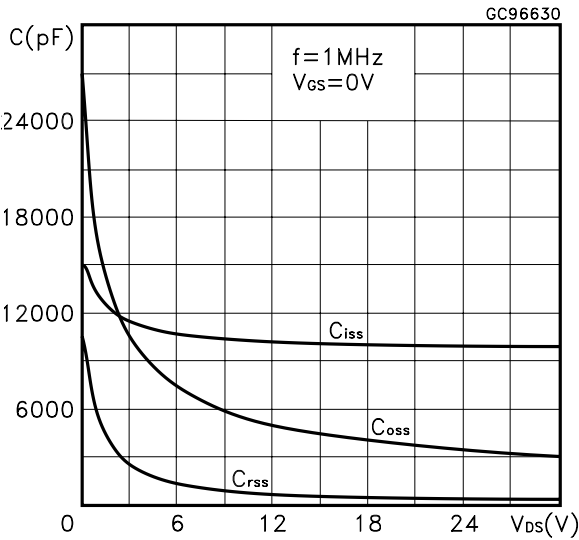
Static Drain-source On Resistance



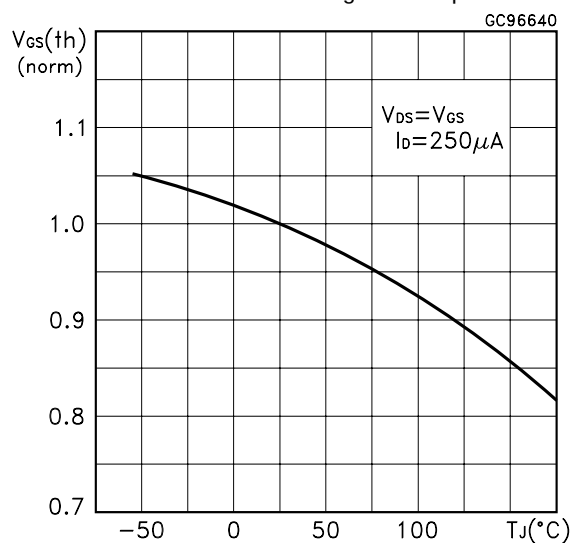
Gate Charge vs Gate-source Voltage



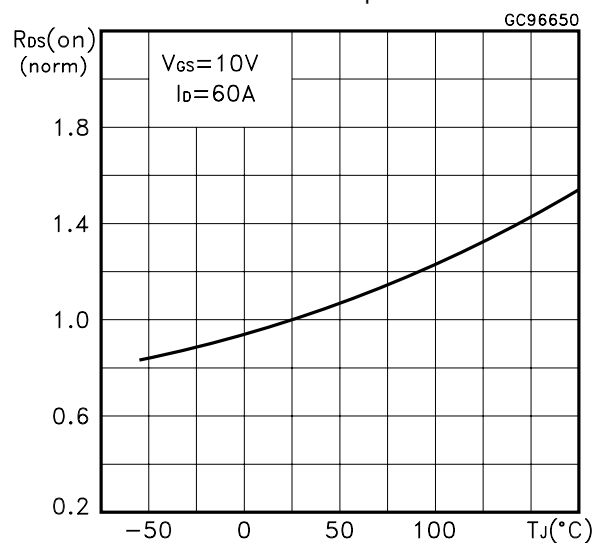
Capacitance Variations



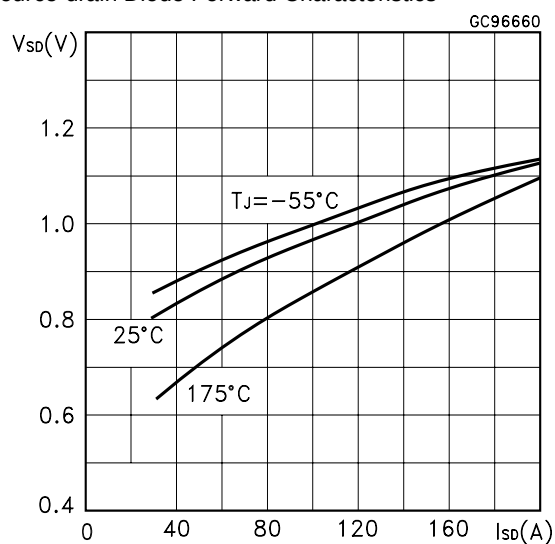
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature.

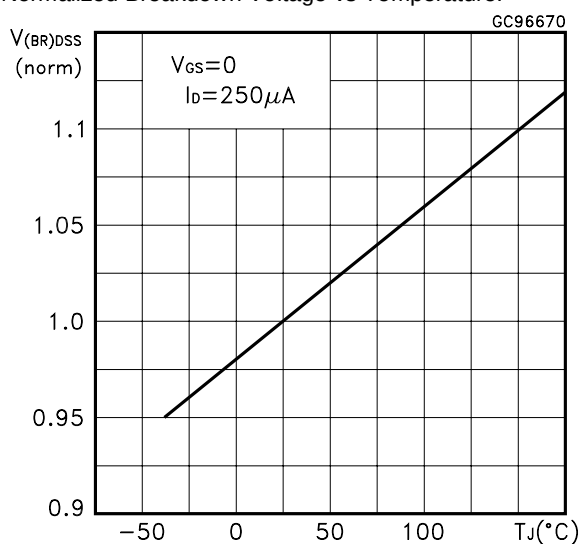


Fig. 1: Unclamped Inductive Load Test Circuit

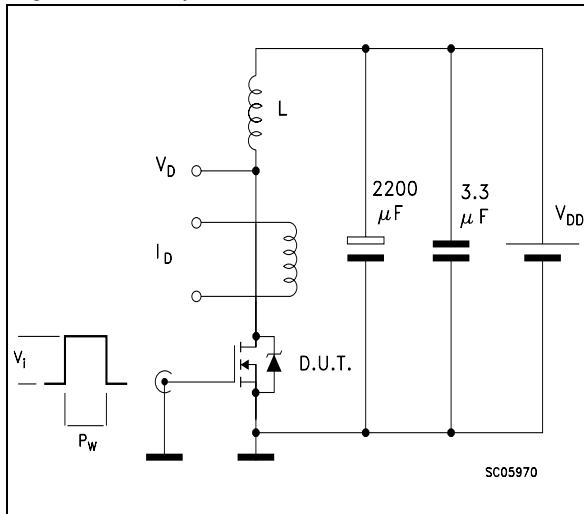


Fig. 2: Unclamped Inductive Waveform

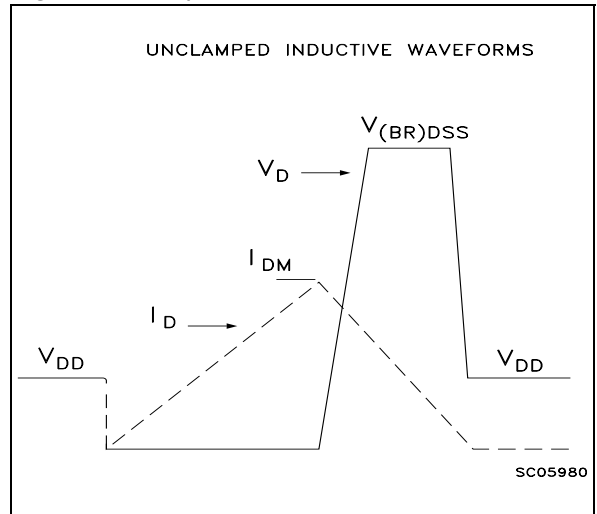


Fig. 3: Switching Times Test Circuits For Resistive Load

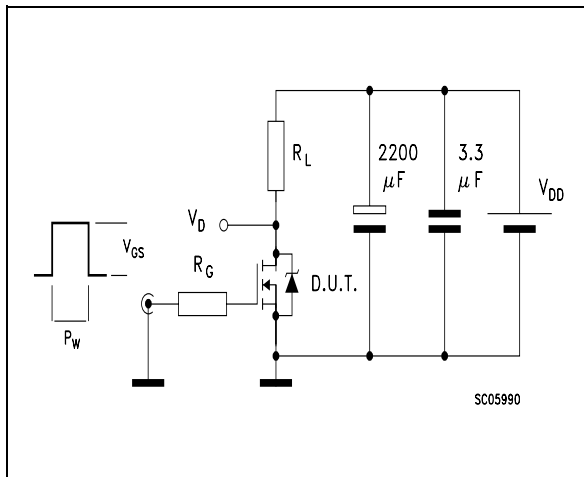


Fig. 4: Gate Charge test Circuit

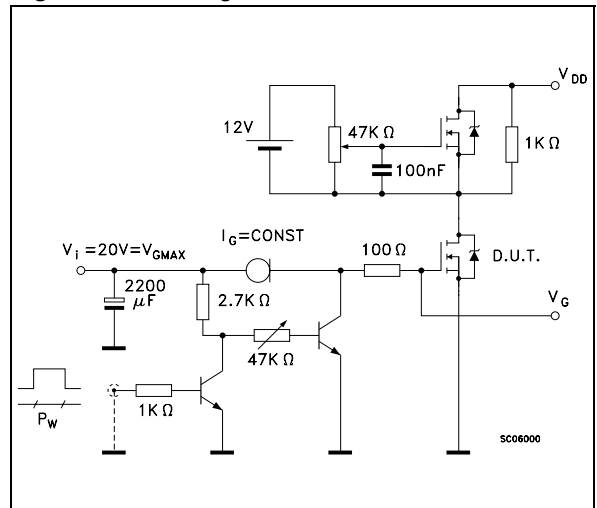
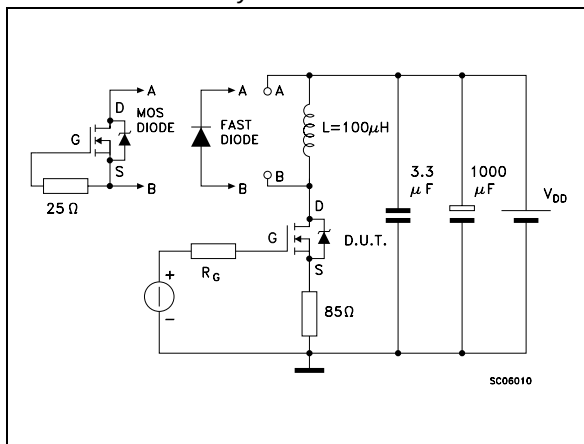
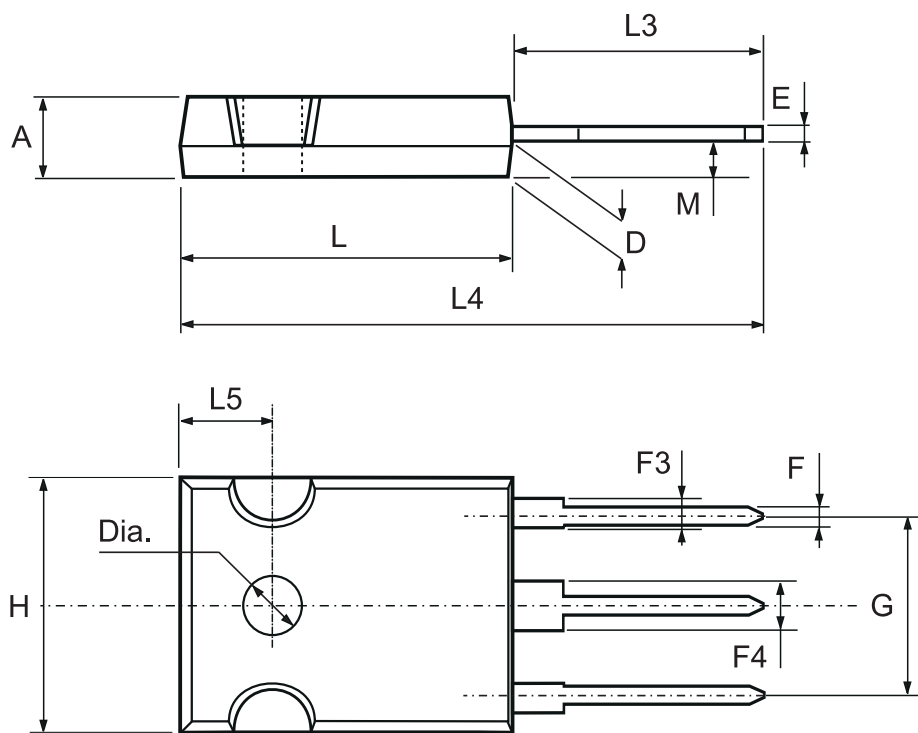


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118



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