M58LW032C

32 Mbit (2Mb x16, Uniform Block, Burst) 3V Supply Flash Memory

PRELIMINARY DATA

FEATURES SUMMARY

WIDE x16 DATA BUS for HIGH BANDWIDTH

SUPPLY VOLTAGE

– V_{DD} = 2.7 to 3.6V core supply voltage for Program, Erase and Read operations

– V_{DDQ} = 1.8 to V_{DD} for I/O Buffers

SYNCHRONOUS/ASYNCHRONOUS READ

– Synchronous Burst read

– Asynchronous Random Read

– Asynchronous Address Latch Controlled Read

– Page Read

ACCESS TIME

– Synchronous Burst Read up to 56MHz

– Asynchronous Page Mode Read 90/25ns, 110/25ns

– Random Read 90ns, 110ns

PROGRAMMING TIME

– 16 Word Write Buffer

– 12µs Word effective programming time

32 UNIFORM 64 KWord MEMORY BLOCKS

BLOCK PROTECTION/ UNPROTECTION

PROGRAM and ERASE SUSPEND

128bit PROTECTION REGISTER

COMMON FLASH INTERFACE

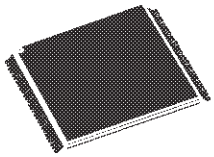
100,000 PROGRAM/ERASE CYCLES per BLOCK

ELECTRONIC SIGNATURE

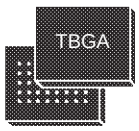
– Manufacturer Code: 0020h

– Device Code M58LW032C : 8822h

Figure 1. Packages



TSOP56 (N)
14 x 20 mm



TBGA64 (ZA)
10 x 13 mm

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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SUMMARY DESCRIPTION

M58LW032C is a 32 Mbit (2Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7V to 3.6V) core supply. On power-up the memory defaults to Read mode with an asynchronous bus where it can be read in the same way as a non-burst Flash memory.

The memory is divided into 32 blocks of 1Mbit that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The Write Buffer allows the microprocessor to program from 1 to 16 Words in parallel, both speeding up the programming and freeing up the microprocessor to perform other work. A Word Program command is available to program a single Word.

Erase can be suspended in order to perform either Read or Program in any other block and then resumed. Program can be suspended to Read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

Individual block protection against Program or Erase is provided for data security. All blocks are protected during power-up. The protection of the blocks is non-volatile; after power-up the protection status of each block is restored to the state when power was last removed. Software commands are provided to allow protection of some or all of the blocks and to cancel all block protection bits simultaneously. All Program or Erase operations are blocked when the Program Erase Enable input V_{PEN} is low.

The Reset/Power-Down pin is used to apply a Hardware Reset to the memory and to set the device in power-down mode.

The STS pin gives information about the memory status. It can be configured in two status: to output a static signal about the status of P/E C (when low P/E C is busy, when high P/E C is ready for a new operation) or to give a pulsing signal to indicate the end of programming or erasing blocks. In this last configuration it supplies a system interrupt signal useful for saving time.

In asynchronous mode Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. An Address Latch input can be used to latch addresses in Latch Controlled mode. Together they allow simple, yet powerful, connection to most microprocessors, often without additional logic.

In synchronous mode all Bus Read operations are synchronous with the Clock. Chip Enable and Output Enable select the Bus Read operation and the Latch Enable input is used to latch the address. The signals are compatible with most microprocessor burst interfaces.

The device includes a 128 bit Protection Register. The Protection Register is divided into two 64 bit segments: the first contains a unique device number written by ST, the second is user programmable. The user programmable segment can be protected.

The memory is available in TSOP56 (14 x 20 mm) and TBGA64 (10 x 13mm, 1mm pitch) packages.

Figure 2. Logic Diagram

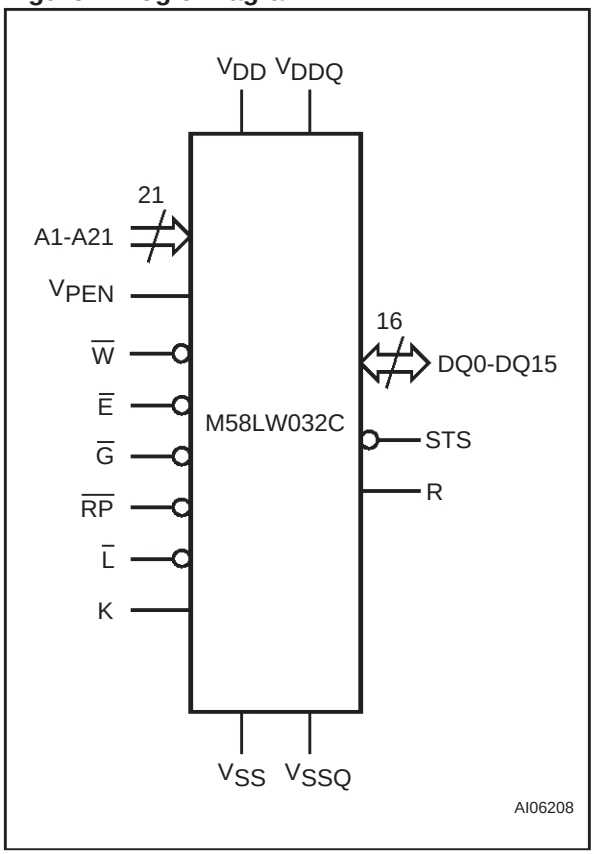


Table 1. Signal Names

A1-A21	Address inputs
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
K	Clock
$\overline{L}$	Latch Enable
R	Valid Data Ready
STS	Status/(Ready/Busy)
$\overline{RP}$	Reset/Power-Down
V_{PEN}	Program/Erase Enable
$\overline{W}$	Write Enable
V_{DD}	Supply Voltage
V_{DDQ}	Input/Output Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Ground
NC	Not Connected Internally

Figure 3. TSOP56 Connections

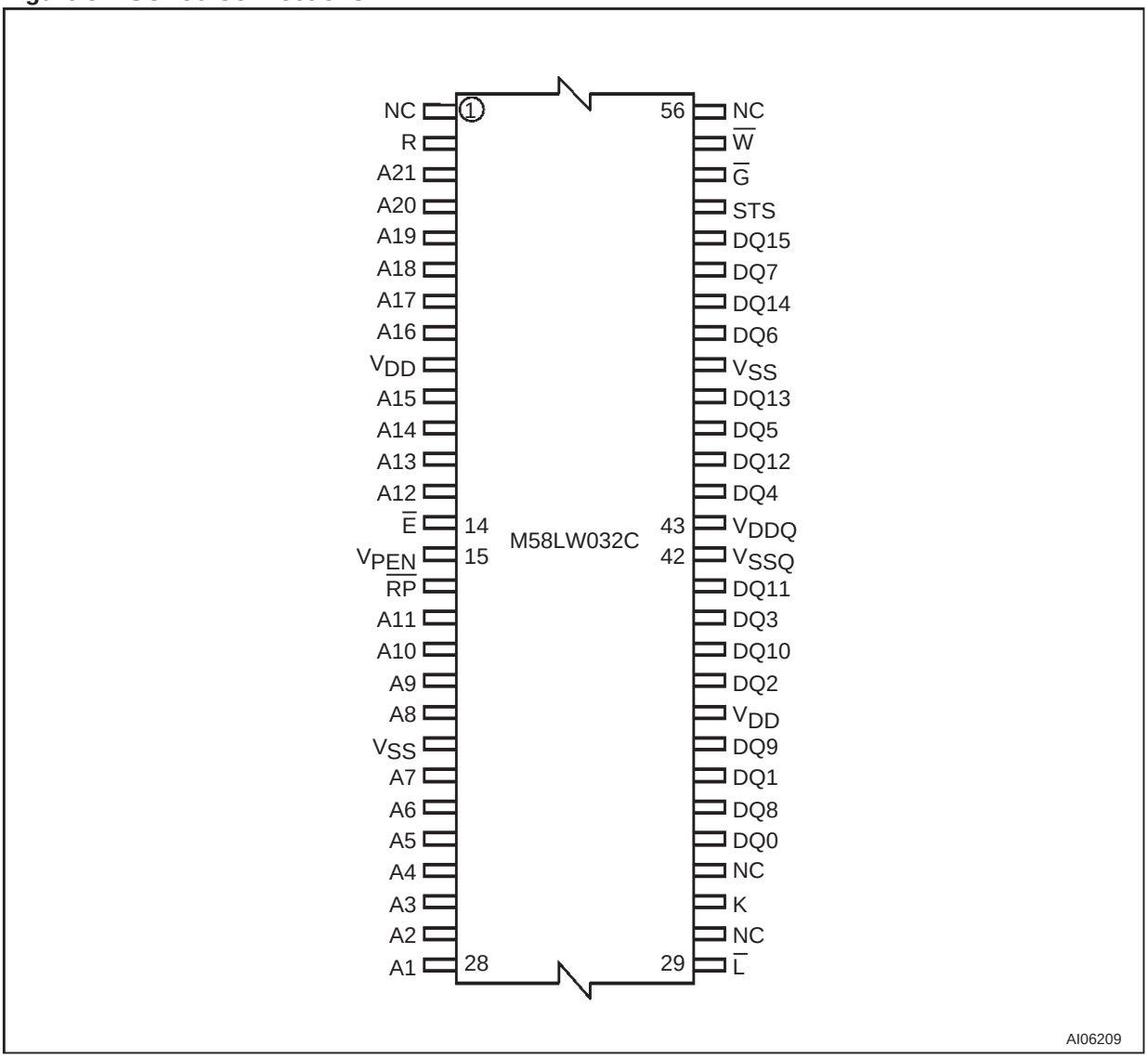


Figure 4. TBGA64 Connections (Top view through package)

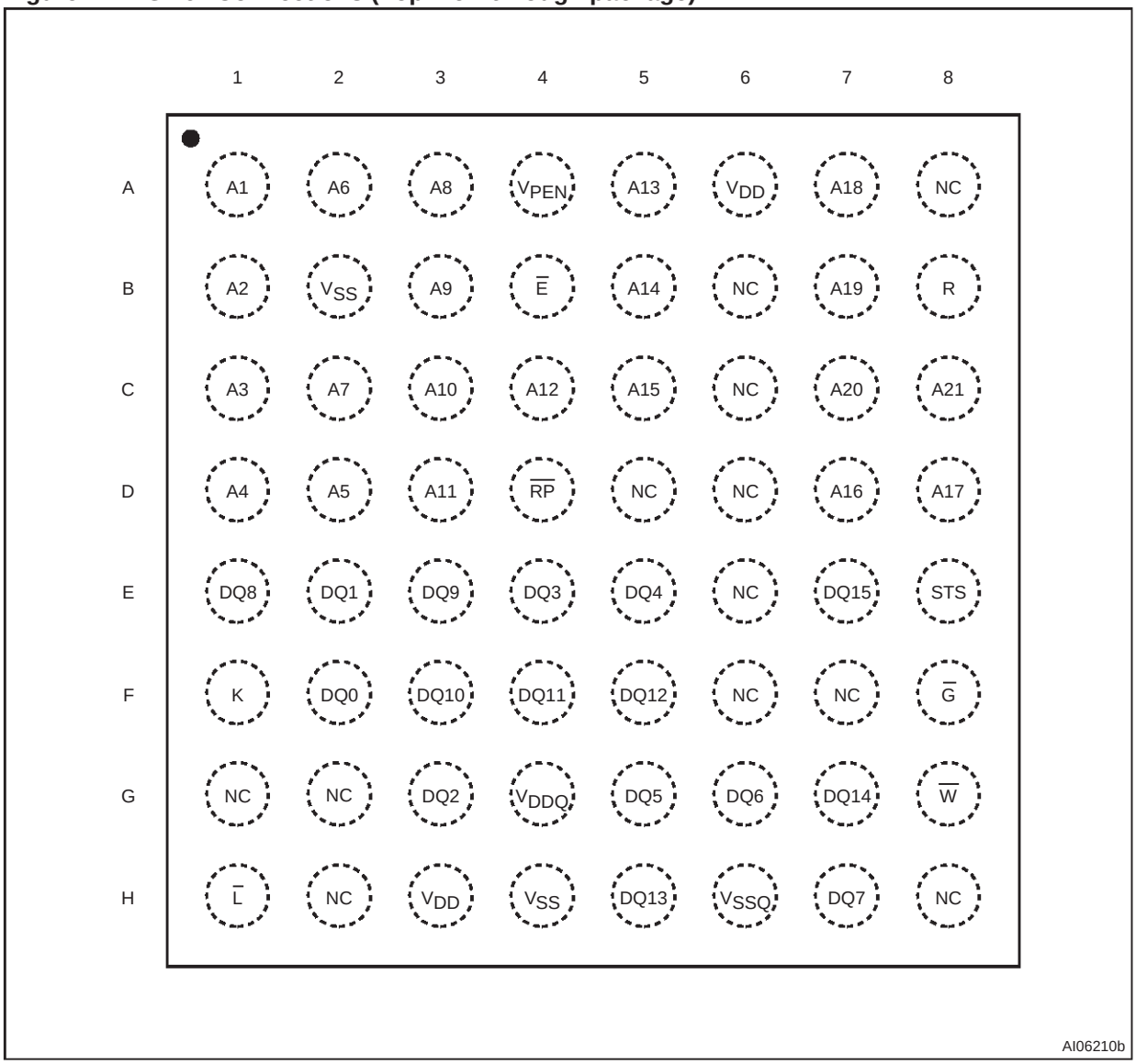
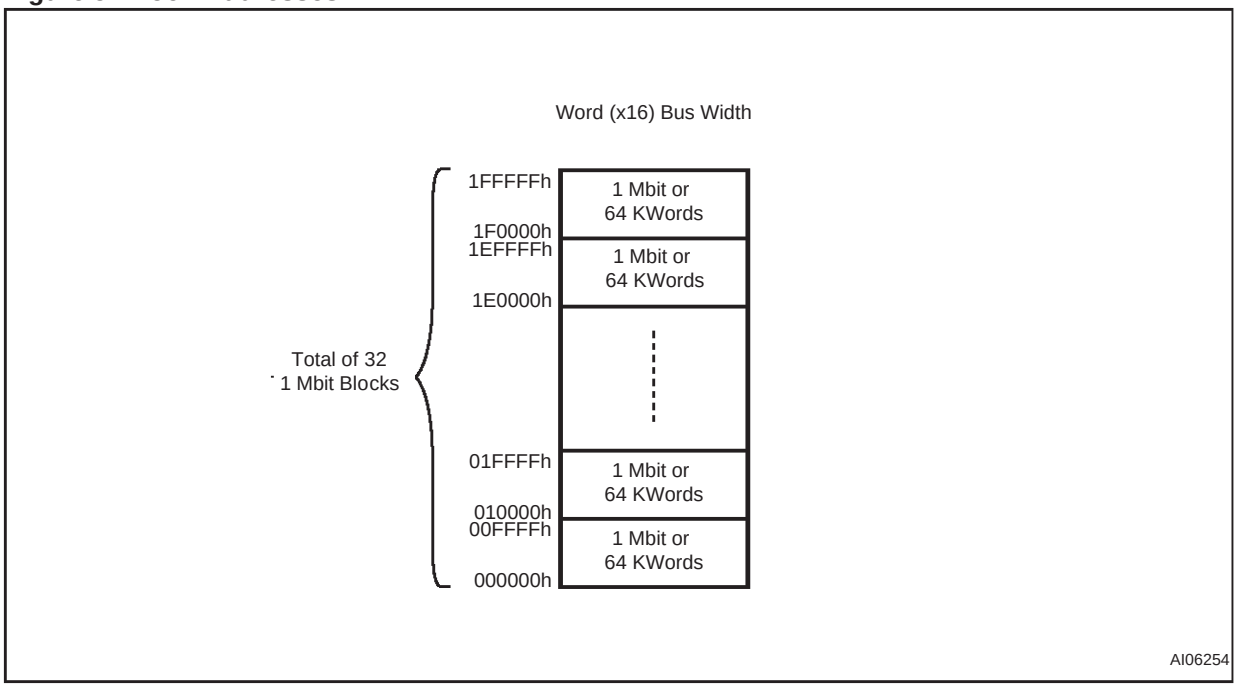


Figure 5. Block Addresses



Note: Also see Appendix A, Table 26 for a full listing of the Block Addresses.

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram and Table 11, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A1-A21). The Address Inputs are used to select the cells to access in the memory array during Bus Read operations either to read or to program data to. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. Chip Enable and Latch Enable must be low when selecting the addresses.

The address inputs are latched on the rising edge of Chip Enable, Write Enable or Latch Enable, whichever occurs first in a Write operation. The address latch is transparent when Latch Enable is low, V_{IL}. The address is internally latched in an Erase or Program operation.

Data Inputs/Outputs (DQ0-DQ15). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation, or are used to input the data during a program operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. When used to input data or Write commands they are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

When Chip Enable and Output Enable are both low, V_{IL}, the data bus outputs data from the memory array, the Electronic Signature, the Block Protection status, the CFI Information or the contents of the Status Register. The data bus is high impedance when the chip is deselected, Output Enable is high, V_{IH}, or the Reset/Power-Down signal is low, V_{IL}. When the Program/Erase Controller is active the Ready/Busy status is given on DQ7.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, input activates the memory control logic, input buffers, decoders and sense amplifiers. Chip Enable, $\overline{E}$, at V_{IH} deselects the memory and reduces the power consumption to the Standby level, I_{DD1}.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a read operation. When Output Enable, $\overline{G}$, is at V_{IH} the outputs are high impedance. Output Enable, $\overline{G}$, can be used to inhibit the data output during a burst read operation.

Write Enable ($\overline{W}$). The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data can be latched on the rising edge of Write Enable (also see Latch Enable, $\overline{L}$).

Reset/Power-Down ($\overline{RP}$). The Reset/Power-Down pin can be used to apply a Hardware Reset to the memory.

A Hardware Reset is achieved by holding Reset/Power-Down Low, V_{IL}, for at least t_{PLPH}. When Reset/Power-Down is Low, V_{IL}, the Status Register information is cleared and the power consumption is reduced to power-down level. The device is deselected and outputs are high impedance. If Reset/Power-Down goes low, V_{IL},during a Block Erase, a Write to Buffer and Program or a Block Protect/Unprotect the operation is aborted and the data may be corrupted. In this case the Ready/Busy pin stays low, V_{IL}, for a maximum timing of $t_{PLPH} + t_{PHRH}$, until the completion of the Reset/Power-Down pulse.

After Reset/Power-Down goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHQV}. Note that Ready/Busy does not fall during a reset, see Ready/Busy Output section.

In an application, it is recommended to associate Reset/Power-Down pin, $\overline{RP}$, with the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the memory is performing an Erase or Program operation, the memory may output the Status Register information instead of being initialized to the default Asynchronous Random Read.

Latch Enable ($\overline{L}$). The Bus Interface is configured to latch the Address Inputs on the rising edge of Latch Enable, $\overline{L}$. In synchronous bus operations the address is latched on the active edge of the Clock when Latch Enable is Low, V_{IL} or on the rising of Latch Enable, whichever occurs first. Once latched, the addresses may change without affecting the address used by the memory. When Latch Enable is Low, V_{IL}, the latch is transparent.

Clock (K). The Clock, K, is used to synchronize the memory with the external bus during Synchronous Bus Read operations. The Clock can be configured to have an active rising or falling edge. Bus signals are latched on the active edge of the Clock during synchronous bus operations. In Synchronous Burst Read mode the address is latched on the first active clock edge when Latch Enable is low, V_{IL}, or on the rising edge of Latch Enable, whichever occurs first.

During asynchronous bus operations the Clock is not used.

Valid Data Ready (R). The Valid Data Ready output, R, is an open drain output that can be used to identify if the memory is ready to output data or not. The Valid Data Ready output is only active during Synchronous Burst Read operations when the Burst Length is set to Continuous. The Valid Data Ready output can be configured to be active on the clock edge of the invalid data read cycle or one cycle before. Valid Data Ready Low, V_{OL}, in-

dicates that the data is not, or will not be valid. Valid Data Ready in a high-impedance state indicates that valid data is or will be available.

Unless Synchronous Burst Read has been selected, Valid Data Ready is high-impedance. It may be tied to other components with the same Valid Data Ready signal to create a unique System Ready signal.

The Valid Data Ready, R, output has an internal pull-up resistor of approximately 1 M powered from V_{DDQ}, designers should use an external pull-up resistor of the correct value to meet the external timing requirements for Valid Data Ready rising. Refer to Figure 19.

Status/(Ready/Busy) (STS). The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes:

Ready/Busy - the pin is Low, V_{OL}, during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation.

Status - the pin gives a pulsing signal to indicate the end of a Program or Block Erase operation.

After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured for Status mode using the Configure STS command.

When the Program/Erase Controller is idle, or suspended, STS can float High through a pull-up resistor. The use of an open-drain output allows the STS pins from several memories to be connected to a single pull-up resistor (a Low will indicate that one, or more, of the memories is busy).

STS is not Low during a reset unless the reset was applied when the Program/Erase controller was active. Ready/Busy can rise before Reset/Power-Down rises.

Program/Erase Enable (V_{PEN}). The Program/Erase Enable input, V_{PEN}, is used to protect all blocks, preventing Program and Erase operations from affecting their data.

Program/Erase Enable must be kept High during all Program/Erase Controller operations, otherwise the operations is not guaranteed to succeed and data may become corrupt.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

It is recommended to power-up and power-down V_{DD} and V_{DDQ} together to avoid any condition that would result in data corruption.

V_{SS} Ground. Ground, V_{SS}, is the reference for the core power supply. It must be connected to the system ground.

V_{SSQ} Ground. V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD} and V_{DDQ} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 10, AC Measurement Load Circuit.

BUS OPERATIONS

This section describes each of the bus operations that control the memory. Each of these is described in this section, see Tables 2 and 3, Bus Operations, for a summary. The bus operation is selected through the Burst Configuration Register; the bits in this register are described at the end of this section.

On Power-up or after a Hardware Reset the memory defaults to Asynchronous Latch Enable Controlled Read and Asynchronous Bus Write, no other bus operation can be performed until the Burst Control Register has been configured.

The Electronic Signature, CFI or Status Register must be read in asynchronous mode or single synchronous burst mode.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Asynchronous Bus Operations

For asynchronous bus operations refer to Table 3 together with the text below.

Asynchronous Bus Read. Asynchronous Bus Read operations read from the memory cells, or specific registers (Electronic Signature, Status Register, CFI and Block Protection Status) in the Command Interface. A valid bus operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable, Output Enable and Latch Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 11, Asynchronous Bus Read AC Waveforms, and Table 16, Asynchronous Bus Read AC Characteristics, for details of when the output becomes valid.

Asynchronous Latch Controlled Bus Read. Asynchronous Latch Controlled Bus Read operations read from the memory cells or specific registers in the Command Interface. The address is latched in the memory before the value is output on the data bus, allowing the address to change during the cycle without affecting the address that the memory uses.

A valid bus operation involves setting the desired address on the Address Inputs, setting Chip Enable and Latch Enable Low, V_{IL} and keeping Write Enable High, V_{IH}; the address is latched on the rising edge of Address Latch. Once latched, the Address Inputs can change. Set Output Enable Low, V_{IL}, to read the data on the Data Inputs/Outputs; see Figure 12, Asynchronous Latch Controlled Bus Read AC Waveforms and Table 17, Asynchronous Latch Controlled Bus Read AC Characteristics for details on when the output becomes valid.

Note that, since the Latch Enable input is transparent when set Low, V_{IL}, Asynchronous Bus Read operations can be performed by holding Latch Enable Low, V_{IL} throughout the bus operation.

Asynchronous Page Read. Asynchronous Page Read operations are used to read from several addresses within the same memory page. Each memory page is 4 Words and has the same A3-A21, only A1 and A2 may change.

Valid bus operations are the same as Asynchronous Bus Read operations but with different timings. The first read operation within the page has identical timings, subsequent reads within the same page have much shorter access times. If the page changes then the normal, longer timings apply again. See Figure 13, Asynchronous Page Read AC Waveforms and Table 18, Asynchronous Page Read AC Characteristics for details on when the outputs become valid.

Asynchronous Bus Write. Asynchronous Bus Write operations write to the Command Interface in order to send commands to the memory or to latch addresses and input data to program. Bus Write operations are asynchronous, the clock, K, is don't care during Bus Write operations.

A valid Asynchronous Bus Write operation begins by setting the desired address on the Address Inputs and setting Latch Enable Low, V_{IL}. The Address Inputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Asynchronous Bus Write operation. See Figures 14, and 16, Asynchronous Write AC Waveforms, and Tables 19 and 20, Asynchronous Write and Latch Controlled Write AC Characteristics, for details of the timing requirements.

Asynchronous Latch Controlled Bus Write. Asynchronous Latch Controlled Bus Write operations write to the Command Interface in order to send commands to the memory or to latch addresses and input data to program. Bus Write operations are asynchronous, the clock, K, is don't care during Bus Write operations.

A valid Asynchronous Latch Controlled Bus Write operation begins by setting the desired address on the Address Inputs and pulsing Latch Enable Low, V_{IL}. The Address Inputs are latched by the Command Interface on the rising edge of Latch Enable, Chip Enable or Write Enable, whichever occurs first. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Out-

put Enable must remain High, V_{IH}, during the whole Asynchronous Bus Write operation. See Figures 15 and 17 Asynchronous Latch Controlled Write AC Waveforms, and Tables 19 and 20, Asynchronous Write and Latch Controlled Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when the Output Enable is High.

Standby. When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high impedance state regardless of Output Enable or Write Enable. The Supply Current is reduced to the Standby Supply Current, I_{DD1}.

During Program or Erase operations the memory will continue to use the Program/Erase Supply Current, I_{DD3}, for Program or Erase operations until the operation completes.

Automatic Low Power. If there is no change in the state of the bus for a short period of time during Asynchronous Bus Read operations the memory enters Auto Low Power mode where the internal Supply Current is reduced to the Auto-Standby Supply Current, I_{DD5}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Automatic Low Power is only available in Asynchronous Read modes.

Power-Down. The memory is in Power-Down mode when Reset/Power-Down, $\overline{RP}$, is Low. The power consumption is reduced to the Power-Down level, I_{DD2}, and the outputs are high impedance, independent of Chip Enable, Output Enable or Write Enable.

Table 2. Asynchronous Bus Operations

Bus Operation	Step	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{L}$	A1-A21	DQ0-DQ15
Asynchronous Bus Read		V_{IL}	V_{IL}	V_{IH}	High	V_{IL}	Address	Data Output
Asynchronous Latch Controlled Bus Read	Address Latch	V_{IL}	V_{IL}	V_{IH}	High	V_{IL}	Address	High Z
	Read	V_{IL}	V_{IL}	V_{IH}	High	V_{IH}	X	Data Output
Asynchronous Page Read		V_{IL}	V_{IL}	V_{IH}	High	V_{IL}	Address	Data Output
Asynchronous Bus Write		V_{IL}	V_{IH}	V_{IL}	High	V_{IL}	Address	Data Input
Asynchronous Latch Controlled Bus Write	Address Latch	V_{IL}	V_{IH}	V_{IL}	High	V_{IL}	Address	Data Input
Output Disable		V_{IL}	V_{IH}	V_{IH}	High	X	X	High Z
Standby		V_{IH}	X	X	High	X	X	High Z
Power-Down		X	X	X	V_{IL}	X	X	High Z

Note: 1. X = Don't Care V_{IL} or V_{IH}. High = V_{IH} or V_{HH}.

Synchronous Bus Operations

For synchronous bus operations refer to Table 3 together with the text below.

Synchronous Burst Read. Synchronous Burst Read operations are used to read from the memory at specific times synchronized to an external reference clock. The burst type, length and latency can be configured. The different configurations for Synchronous Burst Read operations are described in the Burst Configuration Register section.

A valid Synchronous Burst Read operation begins when the address is set on the Address Inputs, Write Enable is High, V_{IH}, and Chip Enable and Latch Enable are Low, V_{IL}, during the active edge of the Clock. The address is latched on the first active clock edge when Latch Enable is low, or on the rising edge of Latch Enable, whichever occurs first. The data becomes available for output after the X-latency specified in the Burst Control Register has expired. The output buffers are activated by setting Output Enable Low, V_{IL}. See Figures 6 and 7 for examples of Synchronous Burst Read operations.

In Continuous Burst mode one Burst Read operation can access the entire memory sequentially. If the starting address is not associated with a page (4 Word) boundary the Valid Data Ready, R, output goes Low, V_{IL}, to indicate that the data will not be ready in time and additional wait-states are required. The Valid Data Ready output timing (bit M8) can be changed in the Burst Configuration Register.

The Synchronous Burst Read timing diagrams and AC Characteristics are described in the AC and DC Parameters section. See Figures 18, 19 and Table 21.

Table 3. Synchronous Burst Read Bus Operations

Bus Operation	Step	$\overline{E}$	$\overline{G}$	$\overline{RP}$	K(3)	$\overline{L}$	A1-A21 DQ0-DQ15
Synchronous Burst Read	Address Latch	V_{IL}	X	V_{IH}	T	V_{IL}	Address Input
	Read	V_{IL}	V_{IL}	V_{IH}	T	X	Data Output
	Read Abort	V_{IH}	X	V_{IH}	X	X	High Z

Note: 1. X = Don't Care, V_{IL} or V_{IH}.
2. M15 = 0, Bit M15 is in the Burst Configuration Register.
3. T = transition, see M6 in the Burst Configuration Register for details on the active edge of K.

Burst Configuration Register

The Burst Configuration Register is used to configure the type of bus access that the memory will perform. The Burst Configuration Register bits are described in Table 4. They specify the selection of the burst length, burst type, burst X and Y latencies and the Read operation. See figures 6 and 7 for examples of Synchronous Burst Read configurations.

The Burst Configuration Register is set through the Command Interface and will retain its information until it is re-configured, the device is reset, or the device goes into Reset/Power-Down mode. The Burst Configuration Register is read using the Read Electronic Signature Command at address 05h.

Read Select Bit (M15). The Read Select bit, M15, is used to switch between asynchronous and synchronous Bus Read operations. When the Read Select bit is set to '1', Bus Read operations are asynchronous; when the Read Select but is set to '0', Bus Read operations are synchronous.

On reset or power-up the Read Select bit is set to '1' for asynchronous access.

X-Latency Bits (M13-M11). The X-Latency bits are used during Synchronous Bus Read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in Table 4, Burst Configuration Register.

Internal Clock Divider Bit (M10). The Internal Clock Divider Bit is used to divide the internal clock by two. When M10 is set to '1' the internal clock is divided by two, which effectively means that the X and Y-Latency values are multiplied by two, that is the number of clock cycles between the address being latched and the first data becoming available will be twice the value set in M13-M11, and the number of clock cycles between consecutive reads will be twice the value set in M9. For example 8-1-1-1 will become 16-2-2-2. When M10 is set to '0' the internal clock runs normally and the X and Y-Latency values are those set in M13-M11 and M9.

Y-Latency Bit (M9). The Y-Latency bit is used during Synchronous Bus Read operations to set the number of clock cycles between consecutive reads. The Y-Latency value depends on both the X-Latency value and the setting in M9.

When the Y-Latency is 1 the data changes each clock cycle; when the Y-Latency is 2 the data changes every second clock cycle. See Table 4, Burst Configuration Register for valid combinations of the Y-Latency, the X-Latency and the Clock frequency.

Valid Data Ready Bit (M8). The Valid Data Ready bit controls the timing of the Valid Data Ready output pin, R. When the Valid Data Ready bit is '0' the Valid Data Ready output pin is driven Low for the active clock edge when invalid data is output on the bus. When the Valid Data Ready bit is '1' the Valid Data Ready output pin is driven Low one clock cycle prior to invalid data being output on the bus.

Burst Type Bit (M7). The Burst Type bit is used to configure the sequence of addresses read as sequential or interleaved. When the Burst Type bit is '0' the memory outputs from interleaved addresses; when the Burst Type bit is '1' the memory outputs from sequential addresses. See Tables 5, Burst Type Definition, for the sequence of addresses output from a given starting address in each mode.

Valid Clock Edge Bit (M6). The Valid Clock Edge bit, M6, is used to configure the active edge of the Clock, K, during Synchronous Burst Read operations. When the Valid Clock Edge bit is '0' the falling edge of the Clock is the active edge; when the Valid Clock Edge bit is '1' the rising edge of the Clock is active.

Burst Length Bit (M2-M0). The Burst Length bits set the maximum number of Words that can be output during a Synchronous Burst Read operation.

Table 4, Burst Configuration Register gives the valid combinations of the Burst Length bits that the memory accepts; Tables 5, Burst Type Definition, give the sequence of addresses output from a given starting address for each length.

M5 M4 and M3 are reserved for future use.

Table 4. Burst Configuration Register

Address Bit	Mnemonic	Bit Name	Reset Value	Value	Description
16	M15	Read Select	1	0	Synchronous Burst Read
				1	Asynchronous Bus Read (default at power-up)
15	M14	Reserved			
14 to 12	M13-M11	X-Latency(2)	XXX	001	Reserved
				010	X-Latency = 4, 4-1-1-1 (use only with Y-Latency = 1)(1)
				011	X-Latency = 5, 5-1-1-1, 5-2-2-2
				100	X-Latency = 6, 6-1-1-1, 6-2-2-2
				101	X-Latency = 7, 7-1-1-1, 7-2-2-2
				110	X-Latency = 8, 8-1-1-1, 8-2-2-2
11	M10	Internal Clock Divider	X	0	X and Y-Latencies remains as set in M13-M11 and M9
				1	Divides internal clock, X and Y-Latencies multiplied by 2
10	M9	Y-Latency(3)	X	0	Y-Latency = 1
				1	Y-Latency = 2
9	M8	Valid Data Ready	X	0	R valid Low during valid Clock edge
				1	R valid Low one cycle before valid Clock edge
8	M7	Burst Type	X	0	Interleaved
				1	Sequential
7	M6	Valid Clock Edge	X	0	Falling Clock edge
				1	Rising Clock edge
6 to 4	M5-M3	Reserved			
3 to 1	M2-M0	Burst Length	XXX	001	4 Words
				010	8 Words
				111	Continuous

Note: 1. 4 - 2 - 2 - 2 (represents X-Y-Y-Y) is not allowed.
2. X latencies can be calculated as: $(t_{AVQV} - t_{LLKH} + t_{QVKH}) + t_{SYSTEM\ MARGIN} < (X - 1)\ t_{K.}$ (X is an integer number from 4 to 8 and t_K is the clock period).
3. Y latencies can be calculated as: $t_{KHQV} + t_{SYSTEM\ MARGIN} + t_{QVKH} < Y\ t_{K.}$
4. $t_{SYSTEM\ MARGIN}$ is the time margin required for the calculation.

Table 5. Burst Type Definition

Starting Address	x4 Sequential	x4 Interleaved	x8 Sequential	x8 Interleaved	Continuous
0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10..
1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7-8-9-10-11..
2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8-9-10-11-12..
3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9-10-11-12-13..
4	–	–	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-2-13-14..
5	–	–	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7-8-9-10-11-12-13-14..
6	–	–	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8-9-10-11-12-13-14-15..
7	–	–	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13-14-15-16..
8	–	–	–	–	8-9-10-11-12-13-14-15-16-17..

Figure 6. Burst Configuration X-1-1-1

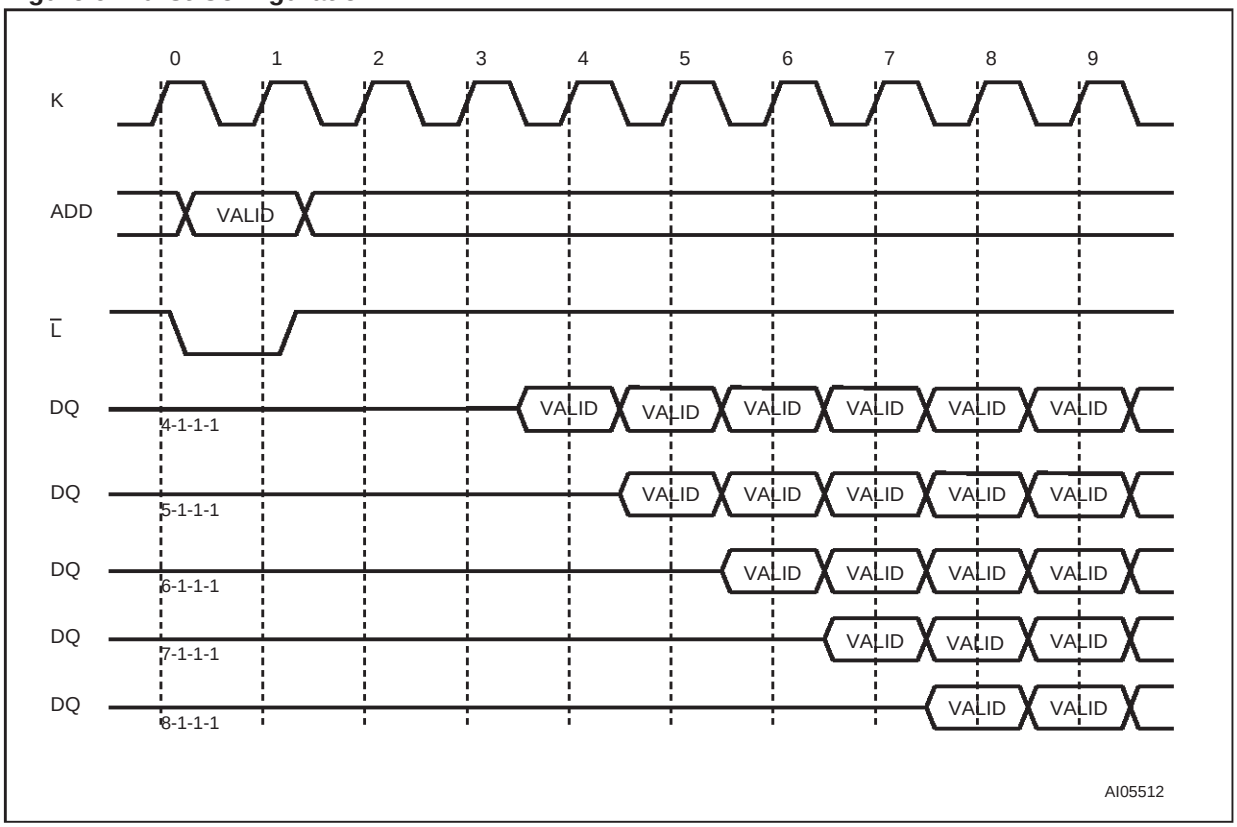
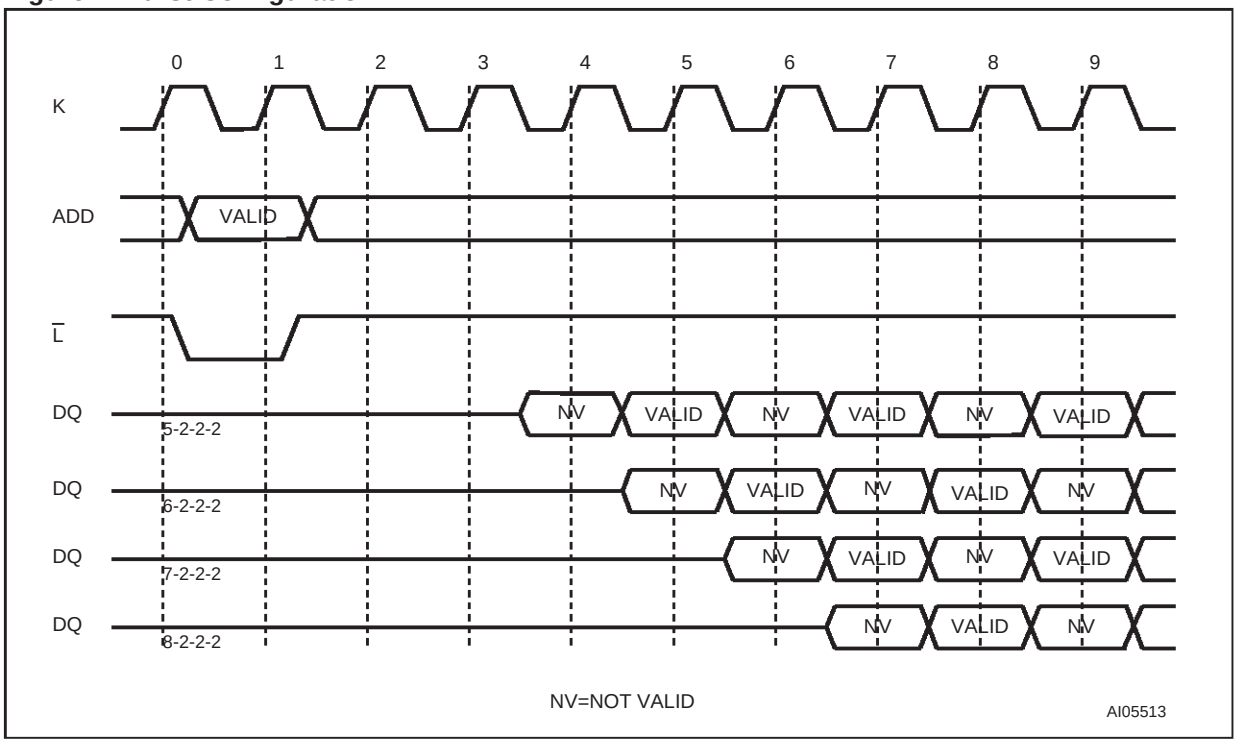


Figure 7. Burst Configuration X-2-2-2



COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. The Commands are summarized in Table 6, Commands. Refer to Table 6 in conjunction with the text descriptions below.

After power-up or a Reset operation the memory enters Read mode.

Synchronous Read operations and Latch Controlled Bus Read operations can only be used to read the memory array. The Electronic Signature, CFI or Status Register will be read in asynchronous mode or single synchronous burst mode. Once the memory returns to Read Memory Array mode the bus will resume the setting in the Burst Configuration Register automatically.

Read Memory Array Command. The Read Memory Array command returns the memory to Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Once the command is issued the memory remains in Read mode until another command is issued. From Read mode Bus Read commands will access the memory array.

While the Program/Erase Controller is executing a Program, Erase, Block Protect, Blocks Unprotect or Protection Register Program operation the memory will not accept the Read Memory Array command until the operation completes.

Read Electronic Signature Command. The Read Electronic Signature command is used to read the Manufacturer Code, the Device Code, the Block Protection Status, the Burst Configuration Register and the Protection Register. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code, the Device Code, the Block Protection Status, the Burst Configuration Register or the Protection Register until another command is issued. Refer to Table 8, Read Electronic Signature, Table 9, Read Protection Register and Figure 8, Protection Register Memory Map for information on the addresses.

Read Query Command. The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See Appendix B, Tables 27, 28, 29, 30, 31 and 32 for details on the information contained in the Common Flash Interface (CFI) memory area.

Read Status Register Command. The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued.

The Status Register information is present on the output data bus (DQ1-DQ7) when both Chip Enable and Output Enable are low, V_{IL}.

See the section on the Status Register and Table 11 for details on the definitions of the Status Register bits

Clear Status Register Command. The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command.

The bits in the Status Register are sticky and do not automatically return to '0' when a new Write to Buffer and Program, Erase, Block Protect, Block Unprotect or Protection Register Program command is issued. If any error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program, Erase or Resume command.

Block Erase Command. The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Erase times are given in Table 10.

See Appendix C, Figure 25, Block Erase Flowchart and Pseudo Code, for a suggested flowchart on using the Block Erase command.

Word Program Command. The Word Program command is used to program a single word in the memory array. Two Bus Write operations are required to issue the command; the first write cycle sets up the Word Program command, the second write cycle latches the address and data to be programmed in the internal state machine and starts the Program/Erase Controller.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

Write to Buffer and Program Command. The Write to Buffer and Program command is used to program the memory array.

Up to 16 Words can be loaded into the Write Buffer and programmed into the memory. Each Write Buffer has the same A5-A21 addresses.

Four successive steps are required to issue the command.

1. One Bus Write operation is required to set up the Write to Buffer and Program Command. Issue the set up command with the selected memory Block Address where the program operation should occur (any address in the block where the values will be programmed can be used). Any Bus Read operations will start to output the Status Register after the 1st cycle.
2. Use one Bus Write operation to write the same block address along with the value N on the Data Inputs/Output, where N+1 is the number of Words to be programmed.
3. Use N+1 Bus Write operations to load the address and data for each Word into the Write Buffer. See the constraints on the address combinations listed below. The addresses must have the same A5-A21.
4. Finally, use one Bus Write operation to issue the final cycle to confirm the command and start the Program operation.

Invalid address combinations or failing to follow the correct sequence of Bus Write cycles will set an error in the Status Register and abort the operation without affecting the data in the memory array. The Status Register should be cleared before re-issuing the command.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

See Appendix C, Figure 23, Write to Buffer and Program Flowchart and Pseudo Code, for a suggested flowchart on using the Write to Buffer and Program command.

Program/Erase Suspend Command. The Program/Erase Suspend command is used to pause a Word Program, Write to Buffer and Program or Erase operation. The command will only be accepted during a Program or an Erase operation. It can be issued at any time during an Erase operation but will only be accepted during a Word Program or Write to Buffer and Program command if the Program/Erase Controller is running.

One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit (bit 7) to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing it is possible for the operation to complete. Once the Program/Erase Controller Status bit (bit 7) indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit (bit 2) or the Erase Suspend Status bit (bit 6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see Table 10.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Erase then the Write to Buffer and Program, and the Program Suspend commands will also be accepted. When a program operation is completed inside a Block Erase Suspend the Read Memory Array command must be issued to reset the device in Read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

See Appendix C, Figure 24, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 26, Erase Suspend & Resume Flowchart and Pseudo Code, for suggested flowcharts on using the Program/Erase Suspend command.

Program/Erase Resume Command. The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. Once the command is issued subsequent Bus Read operations read the Status Register.

Set Burst Configuration Register Command.

The Set Burst Configuration Register command is used to write a new value to the Burst Configuration Control Register which defines the burst length, type, X and Y latencies, Synchronous/

Asynchronous Read mode and the valid Clock edge configuration.

Two Bus Write cycles are required to issue the Set Burst Configuration Register command. Once the command is issued the memory returns to Read mode as if a Read Memory Array command had been issued.

The value for the Burst Configuration Register is presented on A1-A16. M0 is on A1, M1 on A2, etc.; the other address bits are ignored.

Block Protect Command. The Block Protect command is used to protect a block and prevent Program or Erase operations from changing the data in it. Two Bus Write cycles are required to issue the Block Protect command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Protect operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in Table 10.

The Block Protection bits are non-volatile, once set they remain set through reset and power-down/power-up. They are cleared by a Blocks Unprotect command.

See Appendix C, Figure 27, Block Protect Flowchart and Pseudo Code, for a suggested flowchart on using the Block Protect command.

Blocks Unprotect Command. The Blocks Unprotect command is used to unprotect all of the blocks. Two Bus Write cycles are required to issue the Blocks Unprotect command; the second Bus Write cycle starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Unprotect operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in Table 10.

See Appendix C, Figure 28, Block Unprotect Flowchart and Pseudo Code, for a suggested flowchart on using the Block Unprotect command.

Protection Register Program Command. The Protection Register Program command is used to Program the 64 bit user segment of the Protection Register. The segment is programmed 16 bits at a time. Two write cycles are required to issue the Protection Register Program command.

The first bus cycle sets up the Protection Register Program command.

The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The user-programmable segment can be locked by programming bit 1 of the Protection Register Lock location to '0' (see Table 9). Bit 0 of the Protection Register Lock location locks the factory programmed segment and is programmed to '0' in the factory. The locking of the Protection Register is not reversible, once the lock bits are programmed no further changes can be made to the values stored in the Protection Register, see Figure 8, Protection Register Memory Map. Attempting to program a previously protected Protection Register will result in a Status Register error.

The Protection Register Program cannot be suspended. See Appendix C, Figure 29, Protection Register Program Flowchart and Pseudo Code, for the flowchart for using the Protection Register Program command.

Configure STS Command.

The Configure STS command is used to configure the Status/(Ready/Busy) pin. After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured in Status mode using the Configure STS command (refer to Status/(Ready/Busy) section for more details.

Two write cycles are required to issue the Configure STS command.

The first bus cycle sets up the Configure STS command.

The second specifies one of the four possible configurations (refer to Table 7, Configuration Codes):

– Ready/Busy mode

– Pulse on Erase complete mode

– Pulse on Program complete mode

– Pulse on Erase or Program complete mode

The device will not accept the Configure STS command while the Program/Erase controller is busy or during Program/Erase Suspend. When STS pin is pulsing it remains Low for a typical time of 250ns. Any invalid Configuration Code will set an error in the Status Register.

Table 6. Commands

Command	Cycles	Bus Operations											
		1st Cycle			2nd Cycle			Subsequent			Final		
		Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data
Read Memory Array	≥ 2	Write	X	FFh	Read	RA	RD						
Read Electronic Signature	≥ 2	Write	X	90h	Read	IDA(3)	IDD(3)						
Read Status Register	2	Write	X	70h	Read	X	SRD						
Read Query	≥ 2	Write	X	98h	Read	QA(4)	QD(4)						
Clear Status Register	1	Write	X	50h									
Block Erase	2	Write	X	20h	Write	BA	D0						
Word Program	2	Write	X	40h 10h	Write	PA	PD						
Write to Buffer and Program	4 + N	Write	BA	E8h	Write	BA	N	Write	PA	PD	Write	X	D0h
Program/Erase Suspend	1	Write	X	B0h									
Program/Erase Resume	1	Write	X	D0h									
Set Burst Configuration Register	2	Write	X	60h	Write	BCR	03h						
Block Protect	2	Write	X	60h	Write	BA	01h						
Blocks Unprotect	2	Write	X	60h	Write	X	D0h						
Protection Register Program	2	Write	X	C0h	Write	PRA	PRD						
Configure STS command	2	Write	X	B8h	Write	X	CC						

Note: 1. X Don't Care; RA Read Address, RD Read Data, IDA Identifier Address, IDD Identifier Data, SRD Status Register Data, PA Program Address; PD Program Data, QA Query Address, QD Query Data, BA Any address in the Block, BCR Burst Configuration Register value, CC Configuration Code.
2. Base Address, refer to Figure 8 and Table 9 for more information.
3. For Identifier addresses and data refer to table 8, Read Electronic Signature.
4. For Query Address and Data refer to Appendix B, CFI.

Table 7. Configuration Codes

Configuration Code	DQ1	DQ2	Mode	STS Pin	Description
00h	0	0	Ready/Busy	V_{OL} during P/E operations Hi-Z when the memory is ready	The STS pin is Low during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation.
01h	0	1	Pulse on Erase complete	Pulse Low then High when operation completed(2)	Supplies a system interrupt pulse at the end of a Block Erase operation.
02h	1	0	Pulse on Program complete		Supplies a system interrupt pulse at the end of a Program operation.
03h	1	1	Pulse on Erase or Program complete		Supplies a system interrupt pulse at the end of a Block Erase or Program operation.

Note: 1. DQ2-DQ7 are reserved
2. When STS pin is pulsing it remains Low for a typical time of 250ns.

Table 8. Read Electronic Signature

Code	Address (A21-A1)	Data (DQ15-DQ0)
Manufacturer Code	000000h	0020h
Device Code	000001h	8822h
Block Protection Status	SBA+02h	0000h (Block Unprotected) 0001h (Block Protected)
Burst Configuration Register	000005h	BCR
Protection Register	000080h(2)	PRD

Note: 1. SBA is the Start Base Address of each block, BCR is Burst Configuration Register data, PRD is Protection Register Data.
2. Base Address, refer to Figure 8 and Table 9 for more information.

Table 9. Read Protection Register

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
Lock	Factory, User	1	0	0	0	0	0	0	0
0	Factory (Unique ID)	1	0	0	0	0	0	0	1
1	Factory (Unique ID)	1	0	0	0	0	0	1	0
2	Factory (Unique ID)	1	0	0	0	0	0	1	1
3	Factory (Unique ID)	1	0	0	0	0	1	0	0
4	User	1	0	0	0	0	1	0	1
5	User	1	0	0	0	0	1	1	0
6	User	1	0	0	0	0	1	1	1
7	User	1	0	0	0	1	0	0	0

Figure 8. Protection Register Memory Map

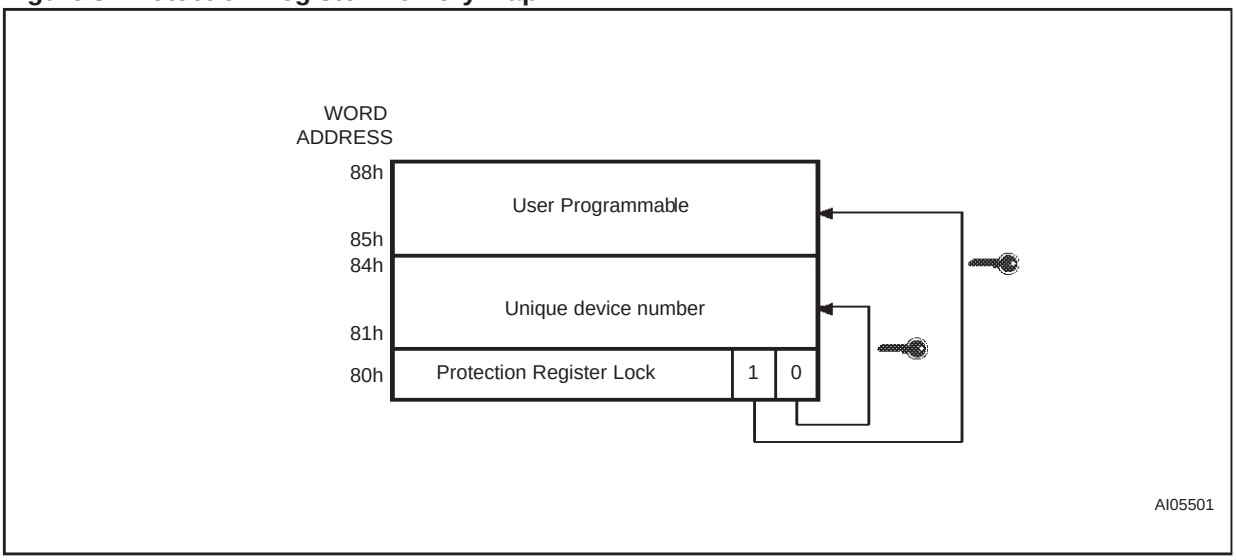


Table 10. Program, Erase Times and Program Erase Endurance Cycles

Parameters	M58LW032C			Unit
	Min	Typ(1,2)	Max(2)	
Block (1Mb) Erase		1.2	4.8(4)	s
Chip Program (Write to Buffer)		24	72(4)	s
Chip Erase Time		37	110 (4)	s
Program Write Buffer		192 (3)	576 (4)	µs
Word/Byte Program Time (Word/Byte Program command)		16	48 (4)	µs
Program Suspend Latency Time		1	20 (5)	µs
Erase Suspend Latency Time		1	25 (5)	µs
Block Protect Time		18	30 (5)	µs
Blocks Unprotect Time		0.75	1.2 (5)	s
Program/Erase Cycles (per block)	100,000			cycles
Data Retention	20			years

Note: 1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Effective byte programming time 6µs, effective word programming time 12µs.
4. Maximum value measured at worst case conditions for both temperature and V_{DD} after 100,000 program/erase cycles.
5. Maximum value measured at worst case conditions for both temperature and V_{DD}.

STATUS REGISTER

The Status Register provides information on the current or previous Program, Erase, Block Protect or Blocks Unprotect operation. The various bits in the Status Register convey information and errors on the operation. They are output on DQ7-DQ0.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase, Block Protect, Blocks Unprotect and Program/Erase Resume commands. The Status Register can be read from any address.

The Status Register can only be read using Asynchronous Bus Read operations. Once the memory returns to Read Memory Array mode the bus will resume the setting in the Burst Configuration Register automatically.

The contents of the Status Register can be updated during an Erase or Program operation by toggling the Output Enable pin or by dis-activating (Chip Enable, V_{IH}) and then reactivating (Chip Enable and Output Enable, V_{IL}) the device.

Status Register bits 5, 4, 3 and 1 are associated with various error conditions and can only be reset with the Clear Status Register command. The Status Register bits are summarized in Table 11, Status Register Bits. Refer to Table 11 in conjunction with the following text descriptions.

Program/Erase Controller Status (Bit 7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is Low, V_{OL}, the Program/Erase Controller is active and all other Status Register bits are High Impedance; when the bit is High, V_{OH}, the Program/Erase Controller is inactive.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

During Program, Erase, Block Protect and Blocks Unprotect operations the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status and Block Protection Status bits should be tested for errors.

Erase Suspend Status (Bit 6). The Erase Suspend Status bit indicates that an Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is Low, V_{OL}, the Program/Erase Controller is active or has completed its operation; when the bit is High, V_{OH}, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status (Bit 5). The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly or that all blocks have been unprotected successfully. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Erase Status bit is Low, V_{OL}, the memory has successfully verified that the block has erased correctly or all blocks have been unprotected successfully. When the Erase Status bit is High, V_{OH}, the erase operation has failed. Depending on the cause of the failure other Status Register bits may also be set to High, V_{OH}.

If only the Erase Status bit (bit 5) is set High, V_{OH}, then the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly or that all the blocks have been unprotected successfully.

If the failure is due to an erase or blocks unprotect with V_{PEN} low, V_{OL}, then V_{PEN} Status bit (bit 3) is also set High, V_{OH}.

If the failure is due to an erase on a protected block then Block Protection Status bit (bit 1) is also set High, V_{OH}.

If the failure is due to a program or erase incorrect command sequence then Program Status bit (bit 4) is also set High, V_{OH}.

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status (Bit 4). The Program Status bit is used to identify a Program or Block Protect failure. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Program Status bit is Low, V_{OL}, the memory has successfully verified that the Write Buffer has programmed correctly or the block is protected. When the Program Status bit is High, V_{OH}, the program or block protect operation has

failed. Depending on the cause of the failure other Status Register bits may also be set to High, V_{OH}.

If only the Program Status bit (bit 4) is set High, V_{OH}, then the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that the Write Buffer has programmed correctly or that the Block is protected.

If the failure is due to a program or block protect with V_{PEN} low, V_{OL}, then V_{PEN} Status bit (bit 3) is also set High, V_{OH}.

If the failure is due to a program on a protected block then Block Protection Status bit (bit 1) is also set High, V_{OH}.

If the failure is due to a program or erase incorrect command sequence then Erase Status bit (bit 5) is also set High, V_{OH}.

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

V_{PEN} Status (Bit 3). The V_{PEN} Status bit can be used to identify if a Program, Erase, Block Protection or Block Unprotection operation has been attempted when V_{PEN} is Low, V_{IL}.

When the V_{PEN} Status bit is Low, V_{OL}, no Program, Erase, Block Protection or Block Unprotection operations have been attempted with V_{PEN} Low, V_{IL}, since the last Clear Status Register command, or hardware reset. When the V_{PEN} Status bit is High, V_{OH}, a Program, Erase, Block Protection or Block Unprotection operation has been attempted with V_{PEN} Low, V_{IL}.

Once set High, the V_{PEN} Status bit can only be reset by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program, Erase, Block Protection or Block Unprotection command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2). The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is Low, V_{OL}, the Program/Erase Controller is active or has completed its operation; when the bit is High, V_{OH}, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status (Bit 1). The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a protected block.

When the Block Protection Status bit is Low, V_{OL}, no Program or Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the Block Protection Status bit is High, V_{OH}, a Program (Program Status bit 4 set High) or Erase (Erase Status bit 5 set High) operation has been attempted on a protected block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Reserved (Bit 0). Bit 0 of the Status Register is reserved. Its value should be masked.

Table 11. Status Register Bits

OPERATION	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	$R\overline{B}$	Result (Hex)
Program/Erase Controller active	0	Hi-Z						V_{OL}	N/A
Write Buffer not ready	0	Hi-Z						V_{OL}	N/A
Write Buffer ready	1	0	0	0	0	0	0	Hi-Z	80h
Write Buffer ready in Erase Suspend	1	1	0	0	0	0	0	Hi-Z	C0h
Program suspended	1	0	0	0	0	1	0	Hi-Z	84h
Program suspended in Erase Suspend	1	1	0	0	0	1	0	Hi-Z	C4h
Program/Block Protect completed successfully	1	0	0	0	0	0	0	Hi-Z	80h
Program completed successfully in Erase Suspend	1	1	0	0	0	0	0	Hi-Z	C0h
Program/Block protect failure due to incorrect command sequence	1	0	1	1	0	0	0	Hi-Z	B0h
Program failure due to incorrect command sequence in Erase Suspend	1	1	1	1	0	0	0	Hi-Z	F0h
Program/Block Protect failure due to V_{PEN} error	1	0	0	1	1	0	0	Hi-Z	98h
Program failure due to V_{PEN} error in Erase Suspend	1	1	0	1	1	0	0	Hi-Z	D8h
Program failure due to Block Protection	1	0	0	1	0	0	1	Hi-Z	92h
Program failure due to Block Protection in Erase Suspend	1	1	0	1	0	0	1	Hi-Z	D2h
Program/Block Protect failure due to cell failure	1	0	0	1	0	0	0	Hi-Z	90h
Program failure due to cell failure in Erase Suspend	1	1	0	1	0	0	0	Hi-Z	D0h
Erase Suspended	1	1	0	0	0	0	0	Hi-Z	C0h
Erase/Blocks Unprotect completed successfully	1	0	0	0	0	0	0	Hi-Z	80h
Erase/Blocks Unprotect failure due to incorrect command sequence	1	0	1	1	0	0	0	Hi-Z	B0h
Erase/Blocks Unprotect failure due to V_{PEN} error	1	0	1	0	1	0	0	Hi-Z	A8h
Erase failure due to Block Protection	1	0	1	0	0	0	1	Hi-Z	A2h
Erase/Blocks Unprotect failure due to failed cells in Block	1	0	1	0	0	0	0	Hi-Z	A0h

MAXIMUM RATING

Stressing the device above the ratings listed in Table 12, Absolute Maximum Ratings, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–55	150	°C
V_{IO}	Input or Output Voltage	–0.6	V_{DDQ} +0.6	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.6	5.0	V

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 13, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 13. Operating and AC Measurement Conditions

Parameter		M58LW032C		Units
		90 - 110		
		Min	Max	
Supply Voltage (V_{DD})		2.7	3.6	V
Input/Output Supply Voltage (V_{DDQ})		1.8	V_{DD}	V
Ambient Temperature (T_A)	Grade 1	0	70	°C
	Grade 6	–40	85	°C
Load Capacitance (C_L)		30		pF
Clock Rise and Fall Times			3	ns
Input Rise and Fall Times			4	ns
Input Pulses Voltages		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages		0.5 V_{DDQ}		V

Figure 9. AC Measurement Input Output Waveform

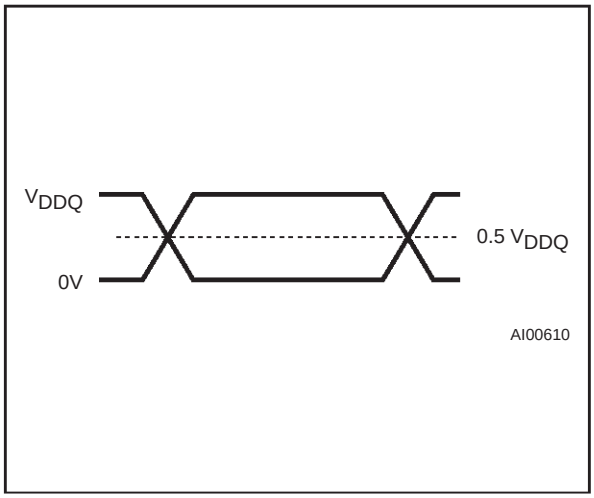


Figure 10. AC Measurement Load Circuit

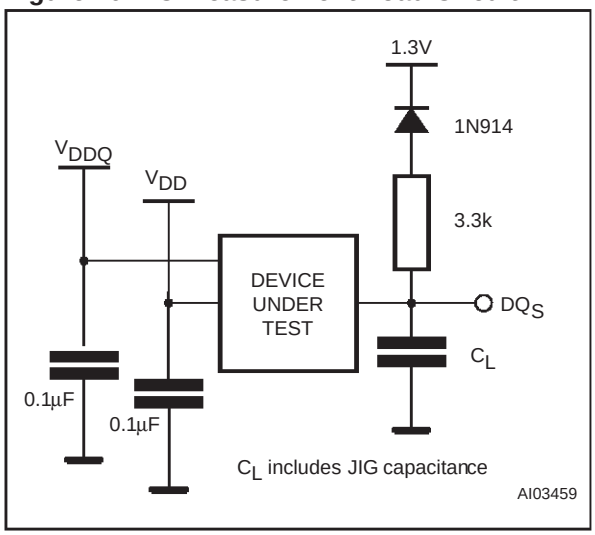


Table 14. Capacitance

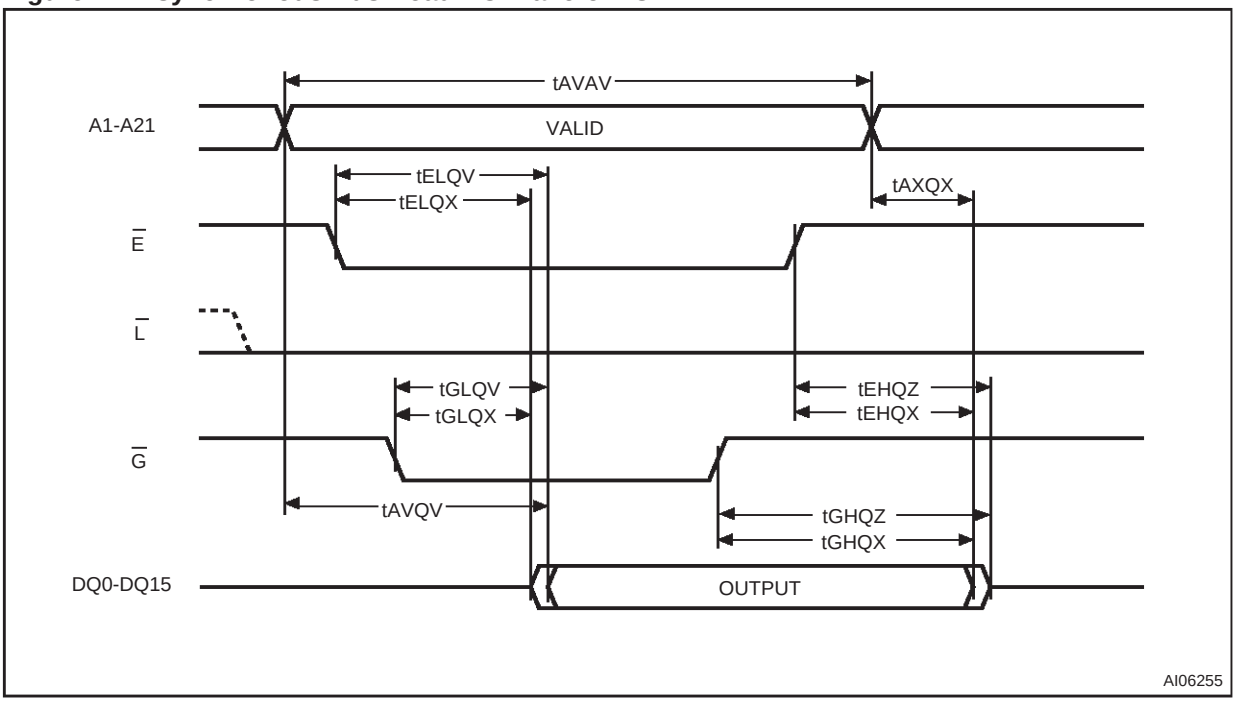
Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Note: 1. T_A = 25°C, f = 1 MHz
2. Sampled only, not 100% tested.

Table 15. DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$		±5	µA
I_{DD}	Supply Current (Random Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{add} = 6MHz		20	mA
I_{DDB}	Supply Current (Burst Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{clock} = 50MHz		30	mA
I_{DD1}	Supply Current (Standby)	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		40	A
I_{DD5}	Supply Current (Auto Low-Power)	$\overline{E} = V_{IL}$, $\overline{RP} = V_{IH}$		40	A
I_{DD2}	Supply Current (Reset/Power-Down)	$\overline{RP} = V_{IL}$		40	µA
I_{DD3}	Supply Current (Program or Erase, Block Protect, Block Unprotect)	Program or Erase operation in progress		30	mA
I_{DD4}	Supply Current (Erase/Program Suspend)	$\overline{E} = V_{IH}$		40	µA
V_{IL}	Input Low Voltage		–0.5	V_{DDQ} x 0.3	V
V_{IH}	Input High Voltage		V_{DDQ} x 0.7	V_{DDQ} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQ} –0.2		V
V_{LKO}	V_{DD} Supply Voltage (Erase and Program lockout)			2	V

Figure 11. Asynchronous Bus Read AC Waveforms

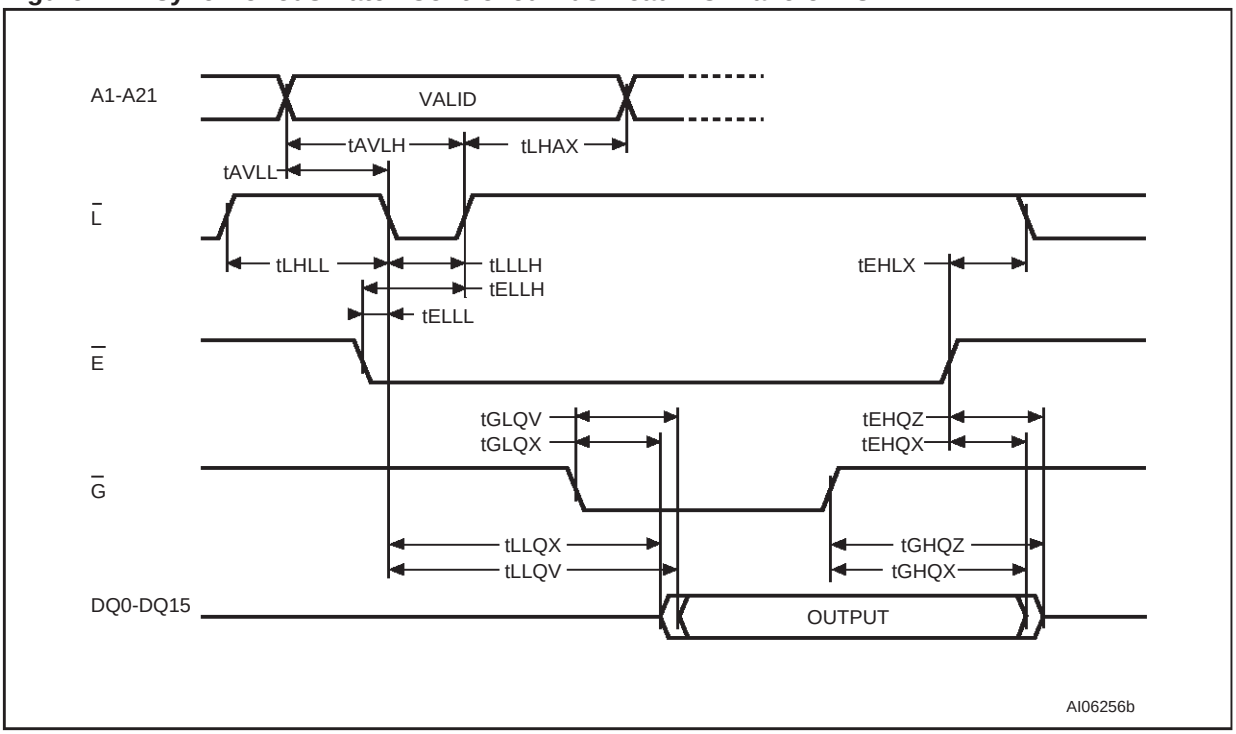


Note: Asynchronous Read M15 = 1

Table 16. Asynchronous Bus Read AC Characteristics.

Symbol	Parameter	Test Condition		M58LW032C		Unit
				90	110	
t_{AVAV}	Address Valid to Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	90	110	ns
t_{AVQV}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	90	110	ns
t_{ELQX}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{ELQV}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	90	110	ns
t_{GLQX}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	25	25	ns
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	25	25	ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	20	20	ns

Figure 12. Asynchronous Latch Controlled Bus Read AC Waveforms



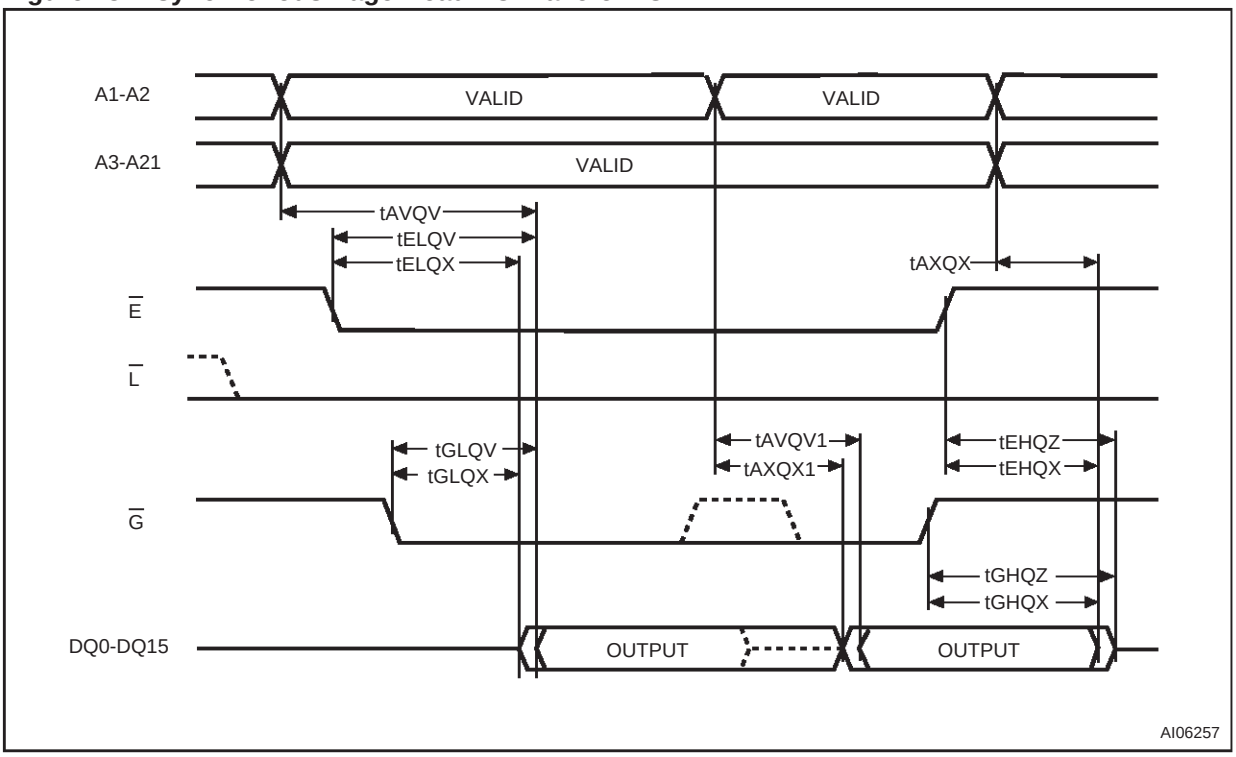
Note: Asynchronous Read M15 = 1

Table 17. Asynchronous Latch Controlled Bus Read AC Characteristics

Symbol	Parameter	Test Condition		M58LW032C		Unit
				90	110	
t_{AVLL}	Address Valid to Latch Enable Low	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{AVLH}	Address Valid to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{LHLL}	Latch Enable High to Latch Enable Low		Min	10	10	ns
t_{LLLH}	Latch Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		Min	0	0	ns
t_{ELLH}	Chip Enable Low to Latch Enable High		Min	10	10	ns
t_{LLQX}	Latch Enable Low to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns
t_{LLQV}	Latch Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	90	110	ns
t_{LHAX}	Latch Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	6	6	ns
t_{GLQX}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	25	25	ns
t_{EHLX}	Chip Enable High to Latch Enable Transition		Min	0	0	ns

Note: For other timings see Table 16, Asynchronous Bus Read Characteristics.

Figure 13. Asynchronous Page Read AC Waveforms



Note: Asynchronous Read M15 = 1

Table 18. Asynchronous Page Read AC Characteristics

Symbol	Parameter	Test Condition		M58LW032C	Unit
				90 - 110	
t_{AXQX1}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	6	ns
t_{AVQV1}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	25	ns

Note: For other timings see Table 16, Asynchronous Bus Read Characteristics.

Figure 14. Asynchronous Write AC Waveform, Write Enable Controlled

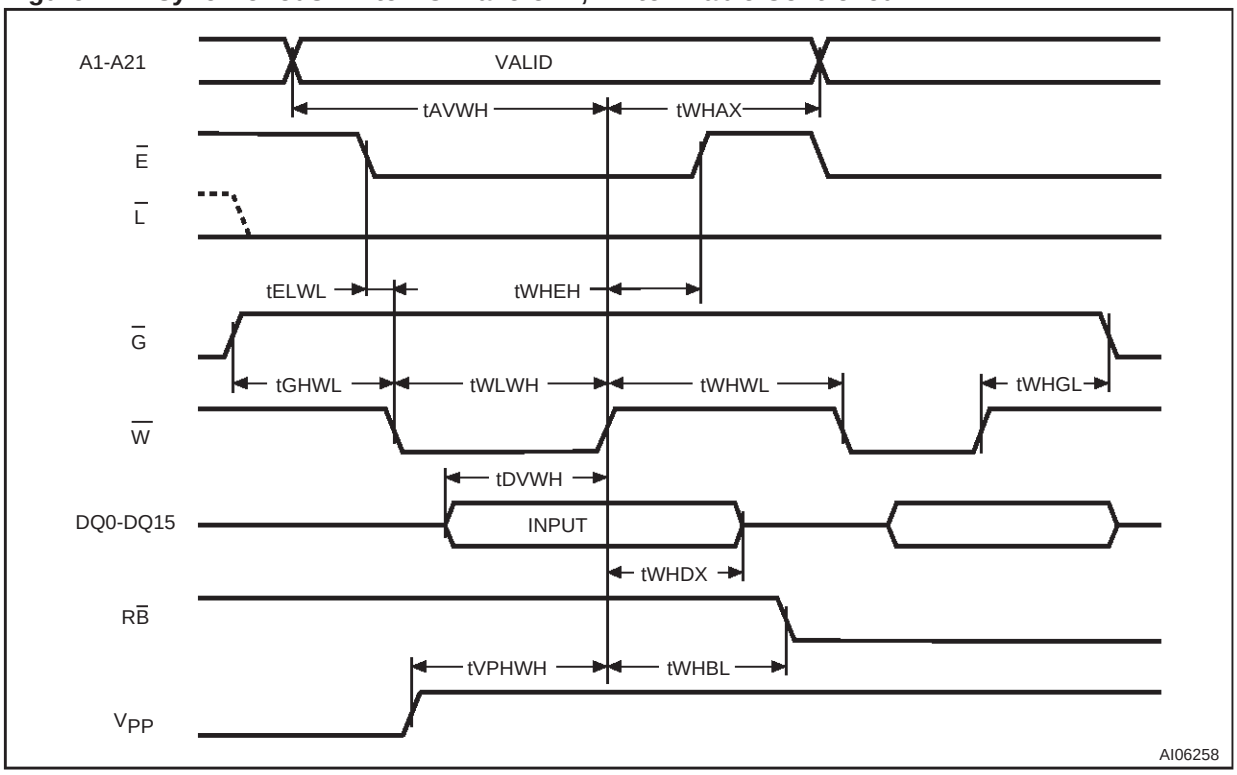


Figure 15. Asynchronous Latch Controlled Write AC Waveform, Write Enable Controlled

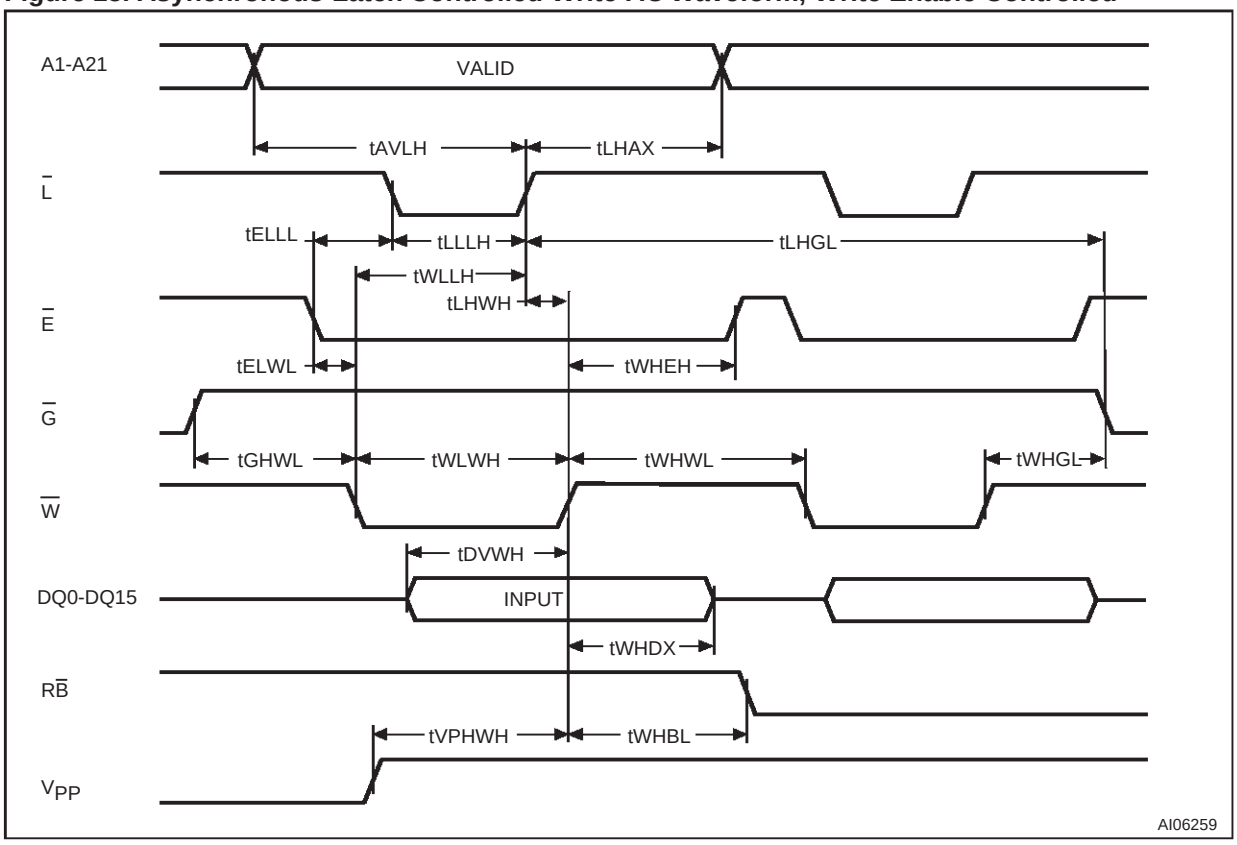


Table 19. Asynchronous Write and Latch Controlled Write AC Characteristics, Write Enable Controlled.

Symbol	Parameter	Test Condition		M58LW032C	Unit
				90 - 110	
t_{AVLH}	Address Valid to Latch Enable High		Min	10	ns
t_{AVWH}	Address Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	ns
t_{DVWH}	Data Input Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	ns
t_{ELWL}	Chip Enable Low to Write Enable Low		Min	0	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		Min	0	ns
t_{LHAX}	Latch Enable High to Address Transition		Min	6	ns
t_{LHGL}	Latch Enable High to Output Enable Low		Min	95	ns
t_{LHWH}	Latch Enable High to Write Enable High		Min	0	ns
t_{LLLH}	Latch Enable low to Latch Enable High		Min	10	ns
t_{LLWH}	Latch Enable Low to Write Enable High		Min	50	ns
t_{VPHWH}	Program/Erase Enable High to Write Enable High		Min	0	ns
t_{WHAX}	Write Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	0	ns
t_{WHBL}	Write Enable High to Ready/Busy low		Max	500	ns
t_{WHDX}	Write Enable High to Input Transition	$\overline{E} = V_{IL}$	Min	0	ns
t_{WHEH}	Write Enable High to Chip Enable High		Min	0	ns
t_{GHWL}	Output Enable High to Write Enable Low		Min	20	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	35	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	30	ns
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{E} = V_{IL}$	Min	70	ns
t_{WLLH}	Write Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	ns

Figure 16. Asynchronous Write AC Waveforms, Chip Enable Controlled

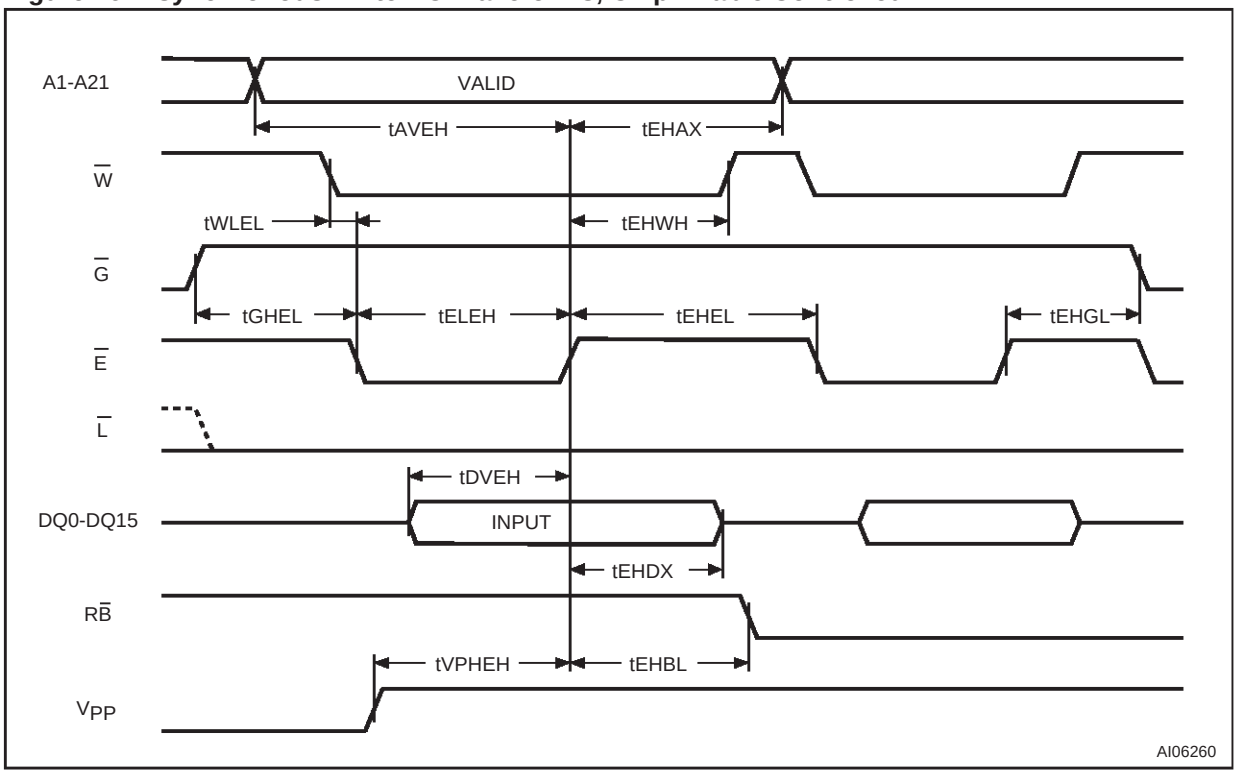


Figure 17. Asynchronous Latch Controlled Write AC Waveforms, Chip Enable Controlled

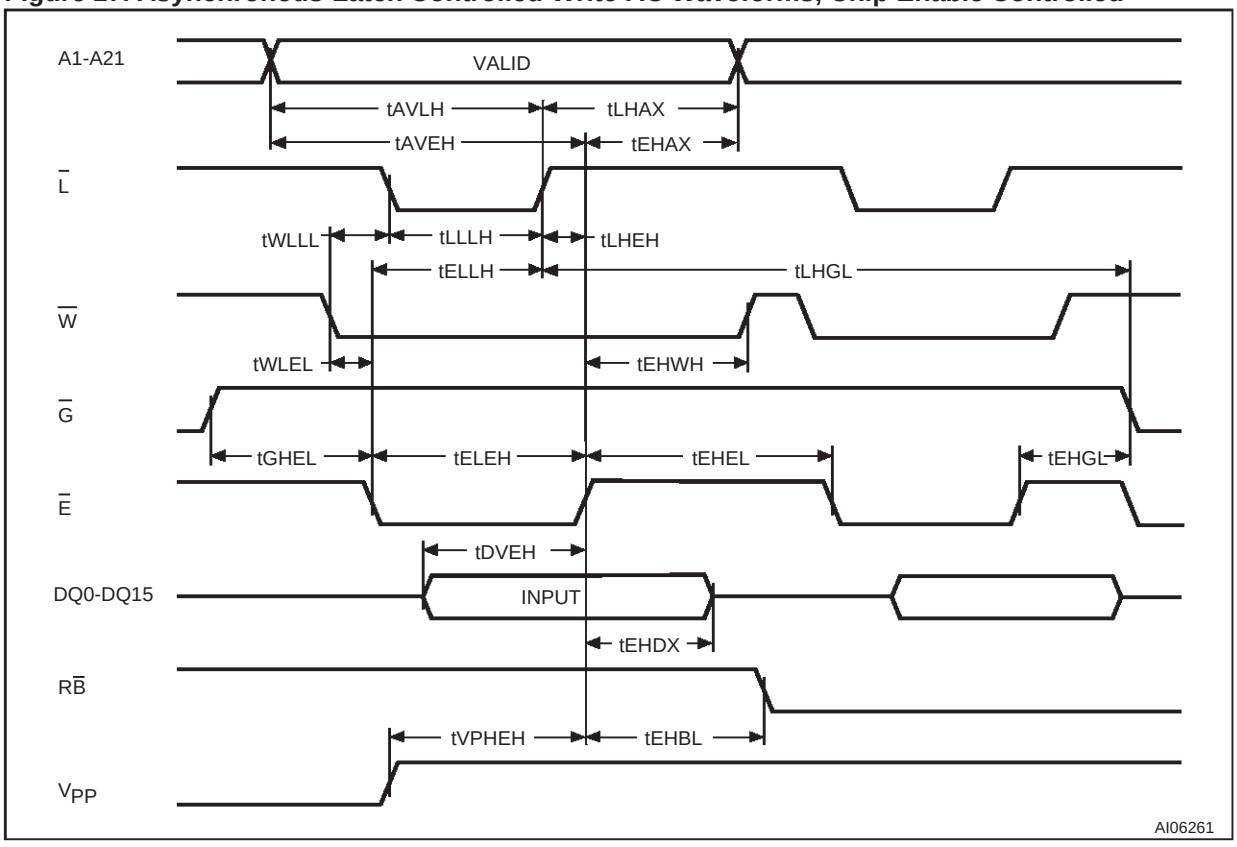
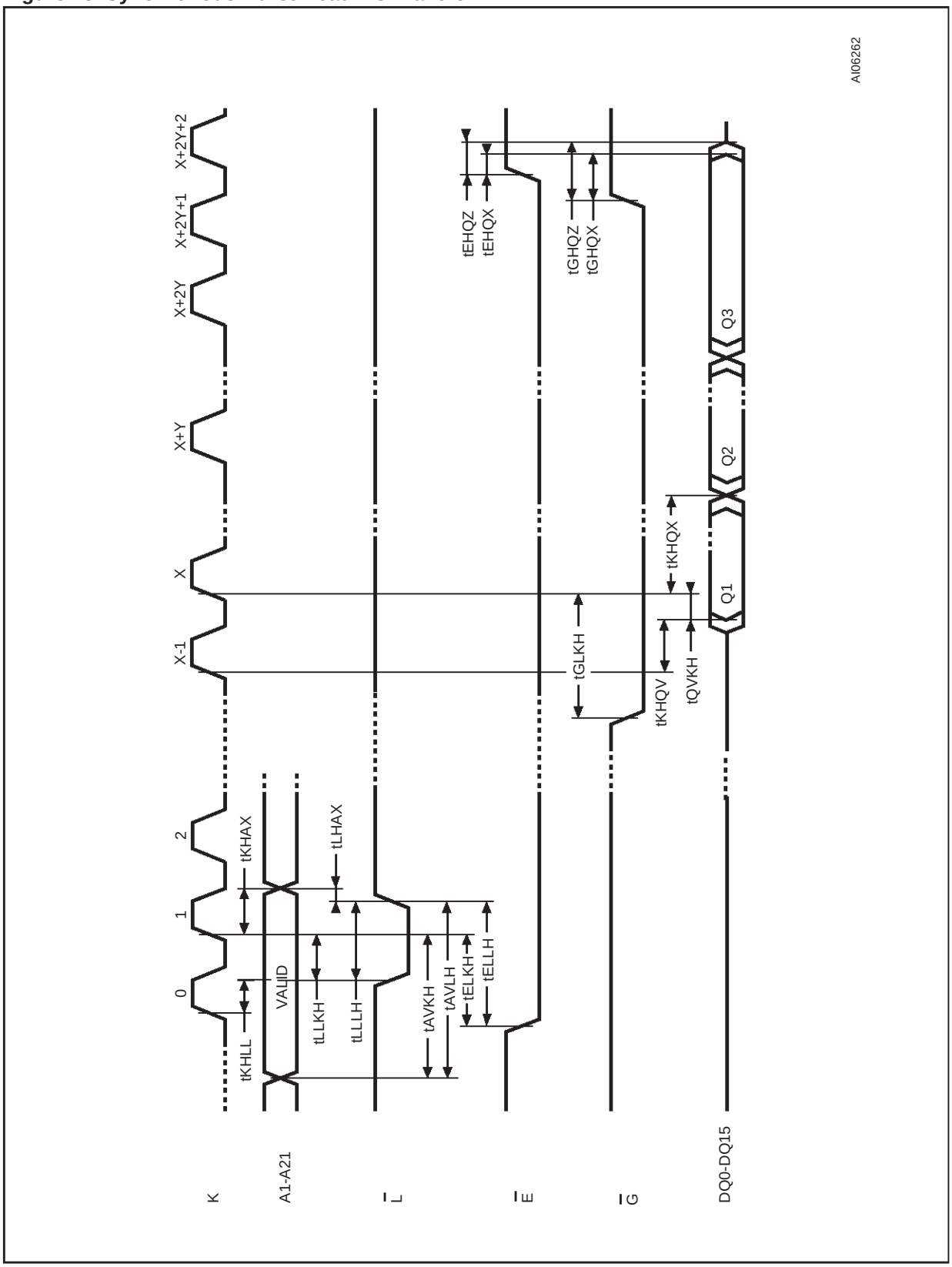


Table 20. Asynchronous Write and Latch Controlled Write AC Characteristics, Chip Enable Controlled

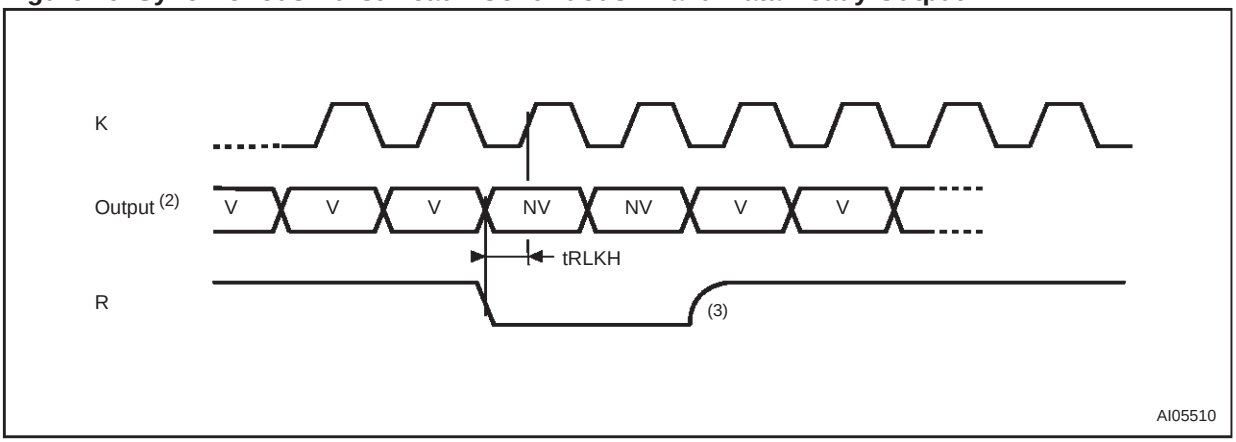
Symbol	Parameter	Test Condition		M58LW032C	Unit
				90 - 110	
t_{AVLH}	Address Valid to Latch Enable High		Min	10	ns
t_{AVEH}	Address Valid to Chip Enable High	$\overline{W} = V_{IL}$	Min	50	ns
t_{DVEH}	Data Input Valid to Chip Enable High	$\overline{W} = V_{IL}$	Min	50	ns
t_{EHAX}	Chip Enable High to Address Transition	$\overline{W} = V_{IL}$	Min	0	ns
t_{EHBL}	Chip Enable High to Ready/Busy low		Max	500	ns
t_{EHDX}	Chip Enable High to Input Transition	$\overline{W} = V_{IL}$	Min	0	ns
t_{EHWH}	Chip Enable High to Write Enable High		Min	0	ns
t_{EHGL}	Chip Enable High to Output Enable Low		Min	35	ns
t_{EHEL}	Chip Enable High to Chip Enable Low		Min	30	ns
t_{ELEH}	Chip Enable Low to Chip Enable High	$\overline{W} = V_{IL}$	Min	70	ns
t_{ELLH}	Chip Enable Low to Latch Enable High	$\overline{W} = V_{IL}$	Min	10	ns
t_{GHEL}	Output Enable High to Chip Enable Low		Min	20	ns
t_{LHAX}	Latch Enable High to Address Transition		Min	6	ns
t_{LHGL}	Latch Enable High to Output Enable Low		Min	35	ns
t_{LHEH}	Latch Enable High to Chip Enable High		Min	0	ns
t_{LLLH}	Latch Enable low to Latch Enable High		Min	10	ns
t_{LLEH}	Latch Enable Low to Chip Enable High		Min	50	ns
t_{VPHEH}	Program/Erase Enable High to Chip Enable High		Min	0	ns
t_{WLEL}	Write Enable Low to Chip Enable Low		Min	0	ns
t_{WLLL}	Write Enable Low to Latch Enable Low		Min	0	ns

Figure 18. Synchronous Burst Read AC Waveform



Note: Valid Clock Edge = Rising (M6 = 1)

Figure 19. Synchronous Burst Read - Continuous - Valid Data Ready Output



Note: 1. Valid Data Ready = Valid Low during valid clock edge (M8 = 0)
2. V= Valid output, NV= Not Valid output.
3. R is an open drain output with an internal pull up resistor of 1M . Depending on the Valid Data Ready pin capacitance load an external pull up resistor must be chosen according to the system clock period.

Table 21. Synchronous Burst Read AC Characteristics

Symbol	Parameter	Test Condition		M58LW032C	Unit
				90 - 110	
t_{AVKH}	Address Valid to Active Clock Edge	$\overline{E} = V_{IL}$	Min	7	ns
t_{AVLH}	Address Valid to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	ns
t_{ELKH}	Chip Enable Low to Active Clock Edge	$\overline{E} = V_{IL}$	Min	10	ns
t_{ELLH}	Chip Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	ns
t_{GLKH}	Output Enable Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{L} = V_{IH}$	Min	20	ns
t_{KHAX}	Valid Clock Edge to Address Transition	$\overline{E} = V_{IL}$	Min	5	ns
t_{KHLL}	Valid Clock Edge to Latch Enable Low	$\overline{E} = V_{IL}$	Min	0	ns
t_{KHLH}	Valid Clock Edge to Latch Enable High	$\overline{E} = V_{IL}$	Min	0	ns
t_{KHQX}	Valid Clock Edge to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	3	ns
t_{LLKH}	Latch Enable Low to Valid Clock Edge	$\overline{E} = V_{IL}$	Min	6	ns
t_{LLLH}	Latch Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	7	ns
t_{KHQV}	Valid Clock Edge to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Max	15	ns
t_{QVKH}	Output Valid to Active Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	5	ns
t_{RLKH}	Valid Data Ready Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	5	ns

Note: For other timings see Table 16, Asynchronous Bus Read Characteristics.

Figure 20. Reset, Power-Down and Power-up AC Waveform

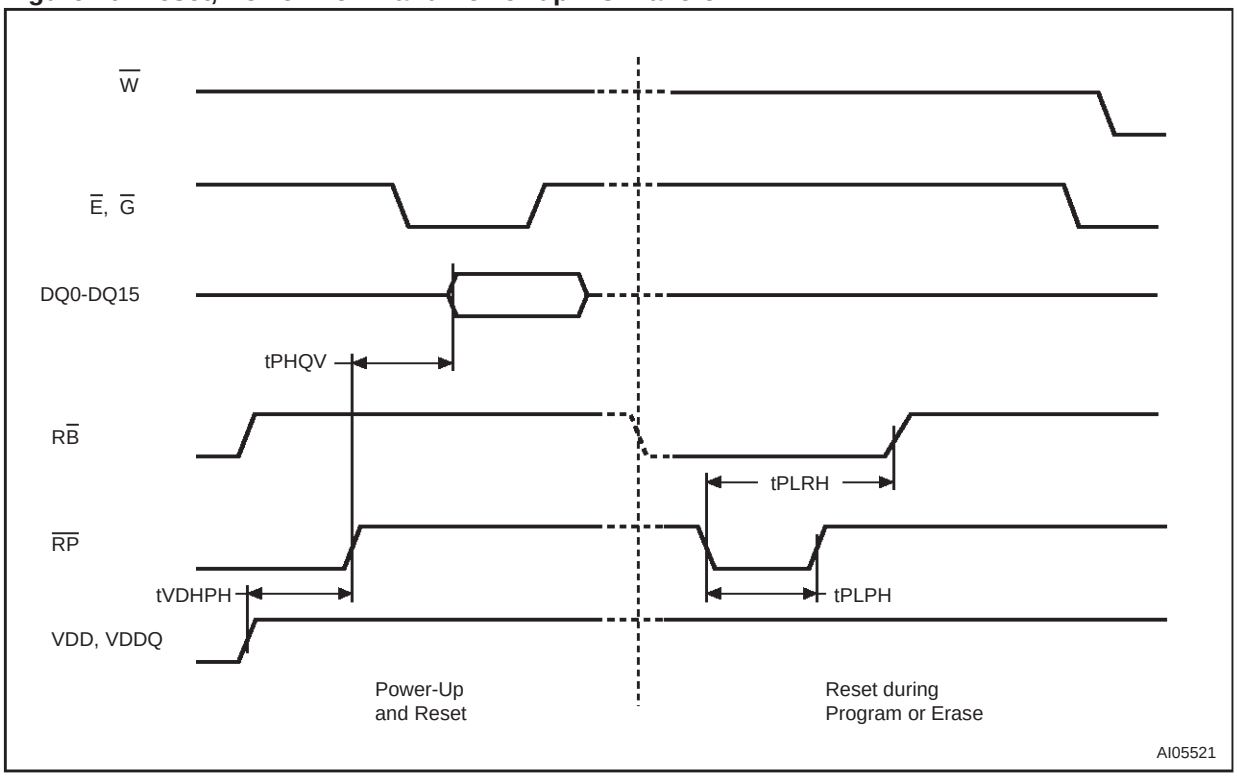
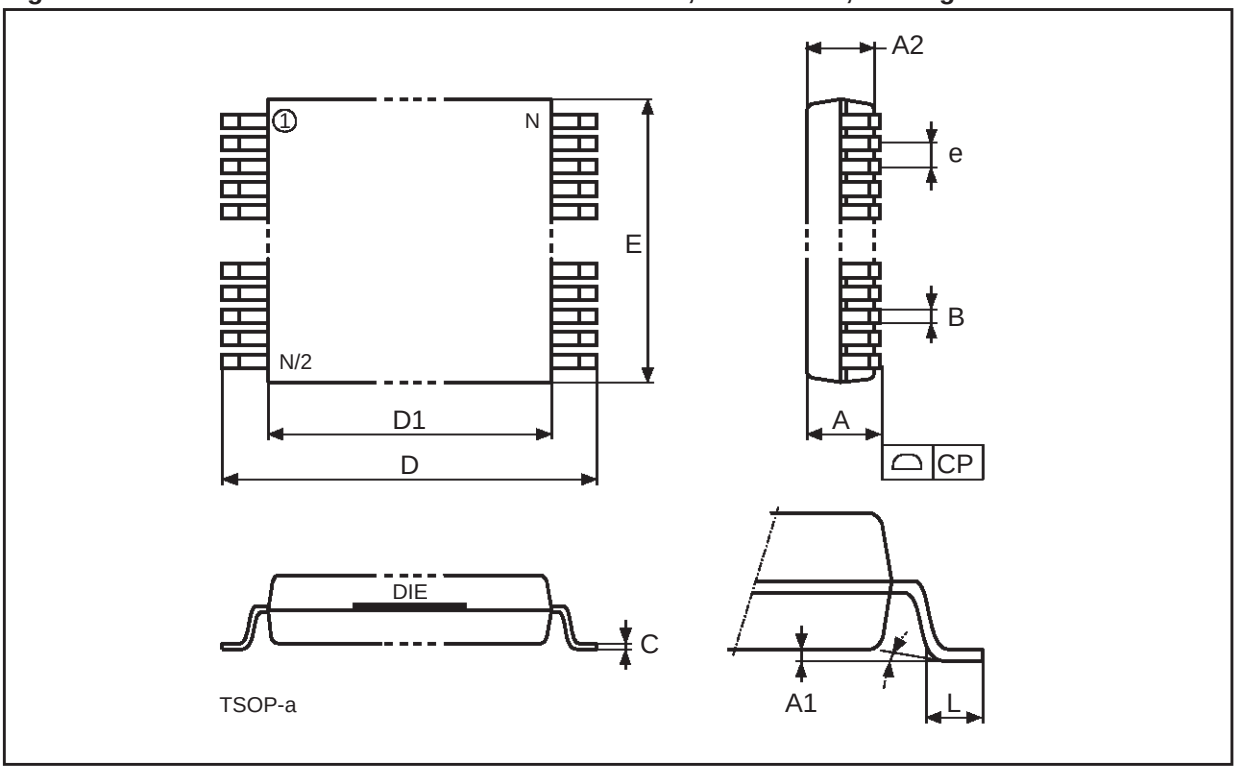


Table 22. Reset, Power-Down and Power-up AC Characteristics

Symbol	Parameter		M58LW032C		Unit
			90	110	
t_{PHQV}	Reset/Power-Down High to Data Valid	Max	130	150	ns
t_{PLPH}	Reset/Power-Down Low to Reset/Power-Down High	Min	100	100	ns
t_{PLRH}	Reset/Power-Down Low to Ready High	Max	30	30	µs
t_{VDHPH}	Supply Voltages High to Reset/Power-Down High	Min	0	0	µs

PACKAGE MECHANICAL

Figure 21. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Outline

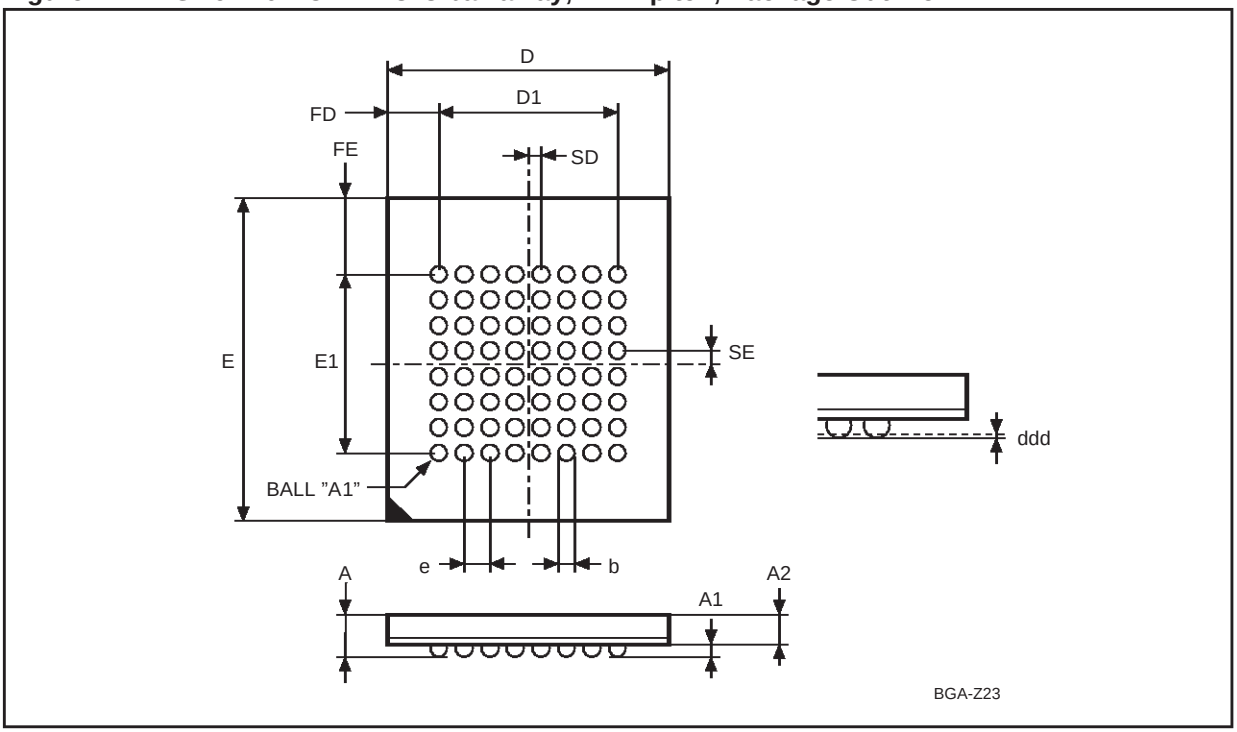


Note: Drawing is not to scale.

Table 23. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		13.90	14.10		0.5472	0.5551
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0276
		0°	5°		0°	5°
N	56			56		
CP			0.10			0.0039

Figure 22. TBGA64 10x13mm - 8x8 ball array, 1mm pitch, Package Outline



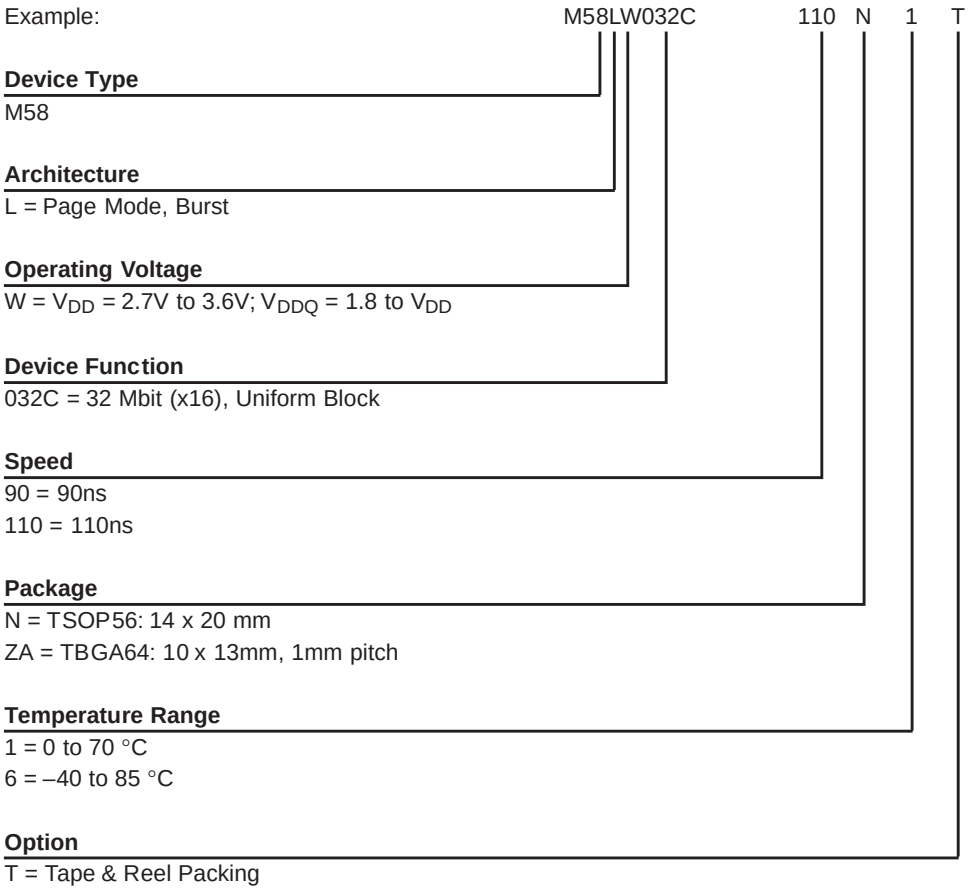
Note: Drawing is not to scale.

Table 24. TBGA64 10x13mm - 8x8 ball array, 1mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.300	0.200	0.350	0.0118	0.0079	0.0138
A2			0.850			0.0335
b		0.400	0.500		0.0157	0.0197
D	10.000	9.900	10.100	0.3937	0.3898	0.3976
D1	7.000	–	–	0.2756	–	–
ddd			0.100			0.0039
e	1.000	–	–	0.0394	–	–
E	13.000	12.900	13.100	0.5118	0.5079	0.5157
E1	7.000	–	–	0.2756	–	–
FD	1.500	–	–	0.0591	–	–
FE	3.000	–	–	0.1181	–	–
SD	0.500	–	–	0.0197	–	–
SE	0.500	–	–	0.0197	–	–

PART NUMBERING

Table 25. Ordering Information Scheme



Note: Devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

APPENDIX A. BLOCK ADDRESS TABLE

Table 26. Block Addresses

Block Number	Address Range (x16 Bus Width)
32	1F0000h-1FFFFFh
31	1E0000h-1EFFFFh
30	1D0000h-1DFFFFh
29	1C0000h-1CFFFFh
28	1B0000h-1BFFFFh
27	1A0000h-1AFFFFh
26	190000h-19FFFFh
25	180000h-18FFFFh
24	170000h-17FFFFh
23	160000h-16FFFFh
22	150000h-15FFFFh
21	140000h-14FFFFh
20	130000h-13FFFFh
19	120000h-12FFFFh
18	110000h-11FFFFh
17	100000h-10FFFFh
16	0F0000h-0FFFFFh
15	0E0000h-0EFFFFh
14	0D0000h-0DFFFFh
13	0C0000h-0CFFFFh
12	0B0000h-0BFFFFh
11	0A0000h-0AFFFFh
10	090000h-09FFFFh
9	080000h-08FFFFh
8	070000h-07FFFFh
7	060000h-06FFFFh
6	050000h-05FFFFh
5	040000h-04FFFFh
4	030000h-03FFFFh
3	020000h-02FFFFh
2	010000h-01FFFFh
1	000000h-00FFFFh

APPENDIX B. COMMON FLASH INTERFACE - CFI

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 27, 28, 29, 30, 31 and 32 show the addresses used to retrieve the data.

Table 27. Query Structure Overview

Offset	Sub-section Name	Description
00h		Manufacturer Code
01h		Device Code
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing and voltage information
27h	Device Geometry Definition	Flash memory layout
P(h)(1)	Primary Algorithm-specific Extended Query Table	Additional information specific to the Primary Algorithm (optional)
A(h)(2)	Alternate Algorithm-specific Extended Query Table	Additional information specific to the Alternate Algorithm (optional)
(SBA+02)h	Block Status Register	Block-related Information

Note: 1. Offset 15h defines P which points to the Primary Algorithm Extended Query Address Table.
2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.
3. SBA is the Start Base Address for each block.

Table 28. CFI - Query Address and Data Output

Address A21-A1	Data		Instruction
10h	51h	"Q"	Query ASCII String 51h; "Q" 52h; "R" 59h; "Y"
11h	52h	"R"	
12h	59h	"Y"	
13h	01h		Primary Vendor: Command Set and Control Interface ID Code
14h	00h		
15h	31h		Primary algorithm extended Query Address Table: P(h)
16h	00h		
17h	00h		Alternate Vendor: Command Set and Control Interface ID Code
18h	00h		
19h	00h		Alternate Algorithm Extended Query address Table
1Ah(2)	00h		

Note: 1. Query Data are always presented on DQ7-DQ0. DQ15-DQ8 are set to '0'.
2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.

Table 29. CFI - Device Voltage and Timing Specification

Address A21-A1	Data	Description
1Bh	27h (1)	V_{DD} Min, 2.7V
1Ch	36h (1)	V_{DD} max, 3.6V
1Dh	00h (2)	V_{PP} min – Not Available
1Eh	00h (2)	V_{PP} max – Not Available
1Fh	04h	2^n µs typical time-out for Word, DWord prog – Not Available
20h	08h	2^n µs, typical time-out for max buffer write
21h	0Ah	2^n ms, typical time-out for Erase Block
22h	00h (3)	2^n ms, typical time-out for chip erase – Not Available
23h	04h	2^n x typical for Word Dword time-out max – Not Available
24h	04h	2^n x typical for buffer write time-out max
25h	04h	2^n x typical for individual block erase time-out maximum
26h	00h (3)	2^n x typical for chip erase max time-out – Not Available

Note: 1. Bits are coded in Binary Code Decimal, bit7 to bit4 are scaled in Volts and bit3 to bit0 in mV.
2. Bit7 to bit4 are coded in Hexadecimal and scaled in Volts while bit3 to bit0 are in Binary Code Decimal and scaled in 100mV.
3. Not supported.

Table 30. Device Geometry Definition

Address A21-A1	Data	Description
27h	16h	n where 2^n is number of bytes memory Size
28h	01h	Device Interface
29h	00h	Organization Sync./Async.
2Ah	05h	Maximum number of bytes in Write Buffer, 2^n
2Bh	00h	
2Ch	01h	Bit7-0 = number of Erase Block Regions in device
2Dh	1Fh	Number (n-1) of Erase Blocks of identical size; n=64
2Eh	00h	
2Fh	00h	Erase Block Region Information x 256 bytes per Erase block (128K bytes)
30h	02h	

Table 31. Block Status Register

Address A21-A1	Data		Selected Block Information
(BA+2)h[1]	bit0	0	Block UnProtected
		1	Block Protected
	bit1	0	Last erase operation ended successfully [2]
		1	Last erase operation not ended successfully [2]
	bit7-2	0	Reserved for future features

Note: 1. BA specifies the block address location, A21-A17.
2. Not Supported.

Table 32. Extended Query information

Address offset	Address A21-A2	Data (Hex) x16 Bus Width		Description
(P)h	31h	50h	"P"	Query ASCII string - Extended Table
(P+1)h	32h	52h	"R"	
(P+2)h	33h	49h	"Y"	
(P+3)h	34h	31h		Major version number
(P+4)h	35h	31h		Minor version number
(P+5)h	36h	CEh		Optional Feature: (1=yes, 0=no) bit0, Chip Erase Supported (0=no) bit1, Suspend Erase Supported (1=yes) bit2, Suspend Program Supported (1=yes) bit3, Protect/UnProtect Supported (1=yes) bit4, Queue Erase Supported (0=no) bit5, Instant Individual Block locking (0=no) bit6, Protection bits supported (1=yes) bit7, Page Read supported (1=yes) bit8, Synchronous Read supported (1=yes) bits 9 to 31 reserved for future use
(P+6)h	37h	01h		
(P+7)h	38h	00h		
(P+8)h	39h	00h		
(P+9)h	3Ah	01h		Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h	3Bh	01h		Block Status Register bit0, Block Protect Bit status active (1=yes) bit1, Block Lock-Down Bit status active (not available) bits 2 to 15 reserved for future use
(P+B)h	3Ch	00h		
(P+C)h	3Dh	33h		V_{DD} OPTIMUM Program/Erase voltage conditions
(P+D)h	3Eh	00h		V_{PP} OPTIMUM Program/Erase voltage conditions
(P+E)h	3Fh	01h		OTP protection: No. of protection register fields
(P+F)h	40h	80h		Protection Register's start address, least significant bits
(P+10)h	41h	00h		Protection Register's start address, most significant bits
(P+11)h	42h	03h		n where 2^n is number of factory reprogrammed bytes
(P+12)h	43h	03h		n where 2^n is number user programmable bytes
(P+13)h	44h	03h		Page Read: 2^n Bytes (n = bits 0-7)
(P+14)h	45h	03h		Synchronous mode configuration fields
(P+15)h	46h	01h		n where 2^{n+1} is the number of Words for the burst Length = 4
(P+16)h	47h	02h		n where 2^{n+1} is the number of Words for the burst Length = 8
(P+17)h	48h	07h		Burst Continuous

Note: 1. Bit7 to bit4 are coded in Hexadecimal and scaled in Volt while bit3 to bit0 are in Binary Code Decimal and scaled in mV.

APPENDIX C. FLOW CHARTS

Figure 23. Write to Buffer and Program Flowchart and Pseudo Code

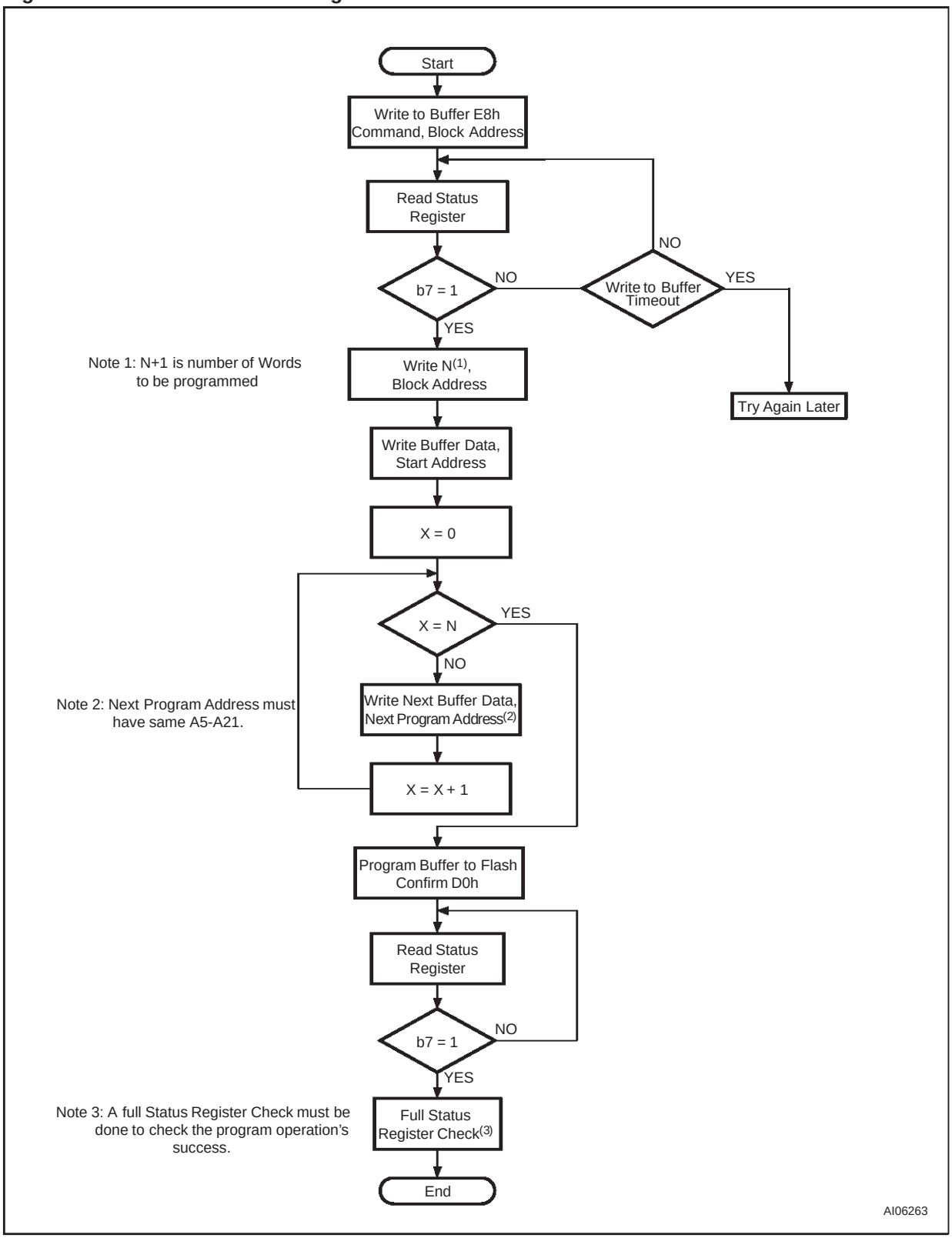
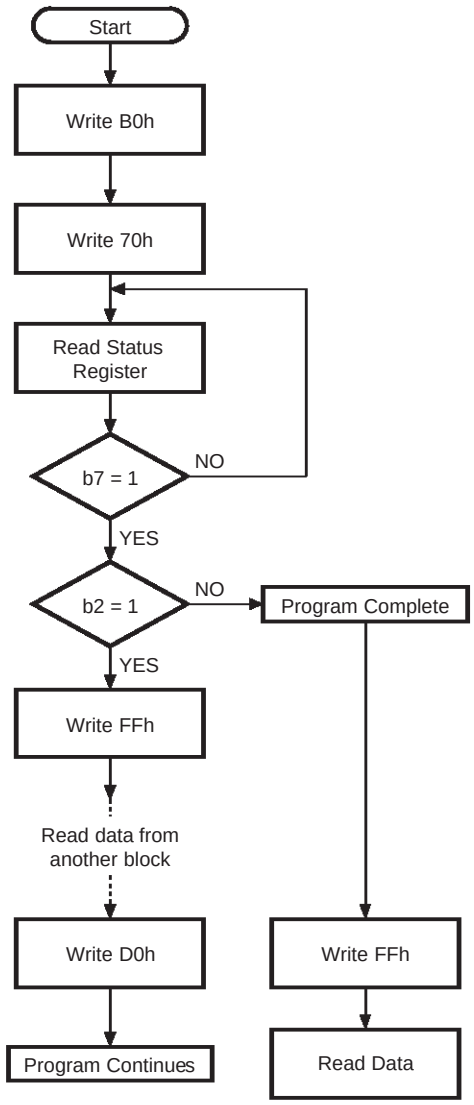


Figure 24. Program Suspend & Resume Flowchart and Pseudo Code



Program/Erase Suspend Command:
– write B0h
– write 70h

do:
– read status register

while b7 = 1

If b2 = 0, Program completed

Read Memory Array instruction:
– write FFh
– one or more data reads from other blocks

Program Erase Resume Command:
– write D0h to resume erasure
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase Suspend command was not issued).

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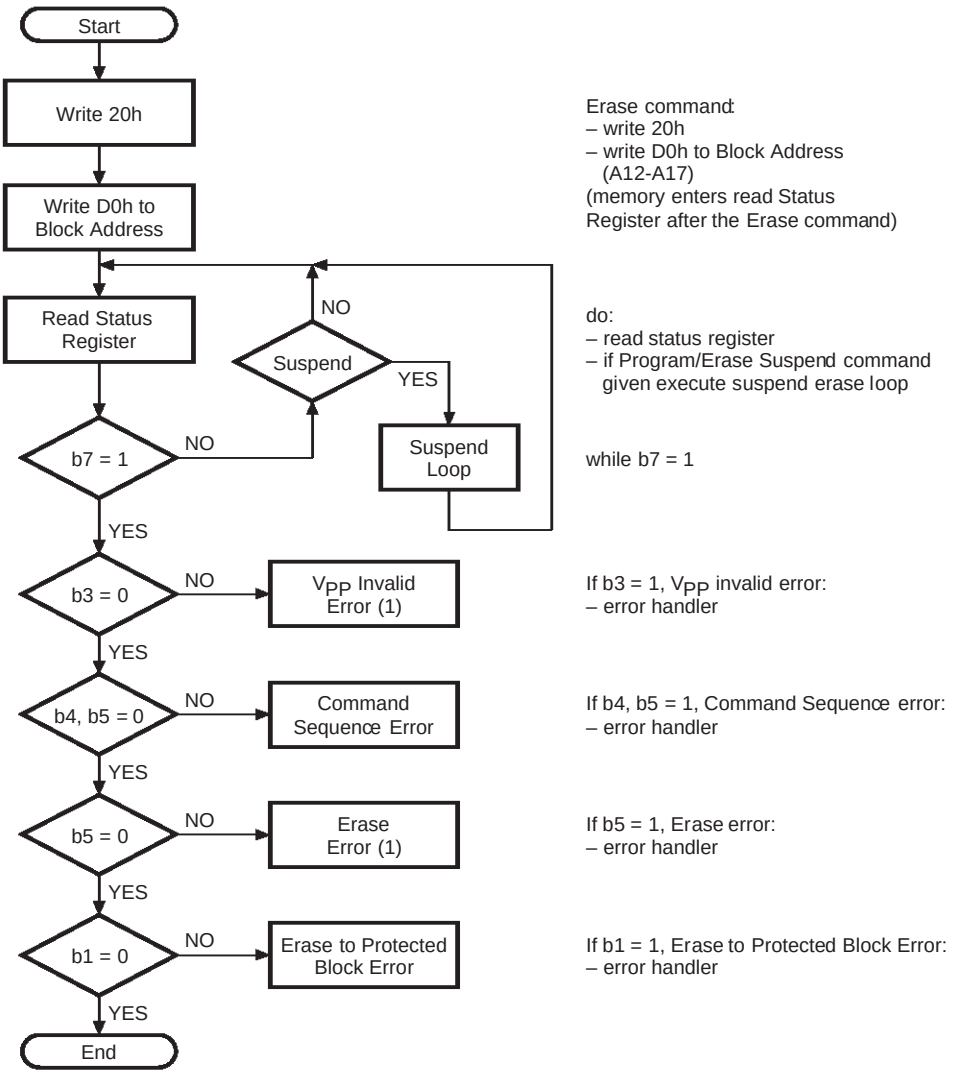
Figure 25. Erase Flowchart and Pseudo Code



Note: 1. If an error is found, the Status Register must be cleared (Clear Status Register Command) before further Program or Erase operations.

Figure 26. Erase Suspend & Resume Flowchart and Pseudo Code

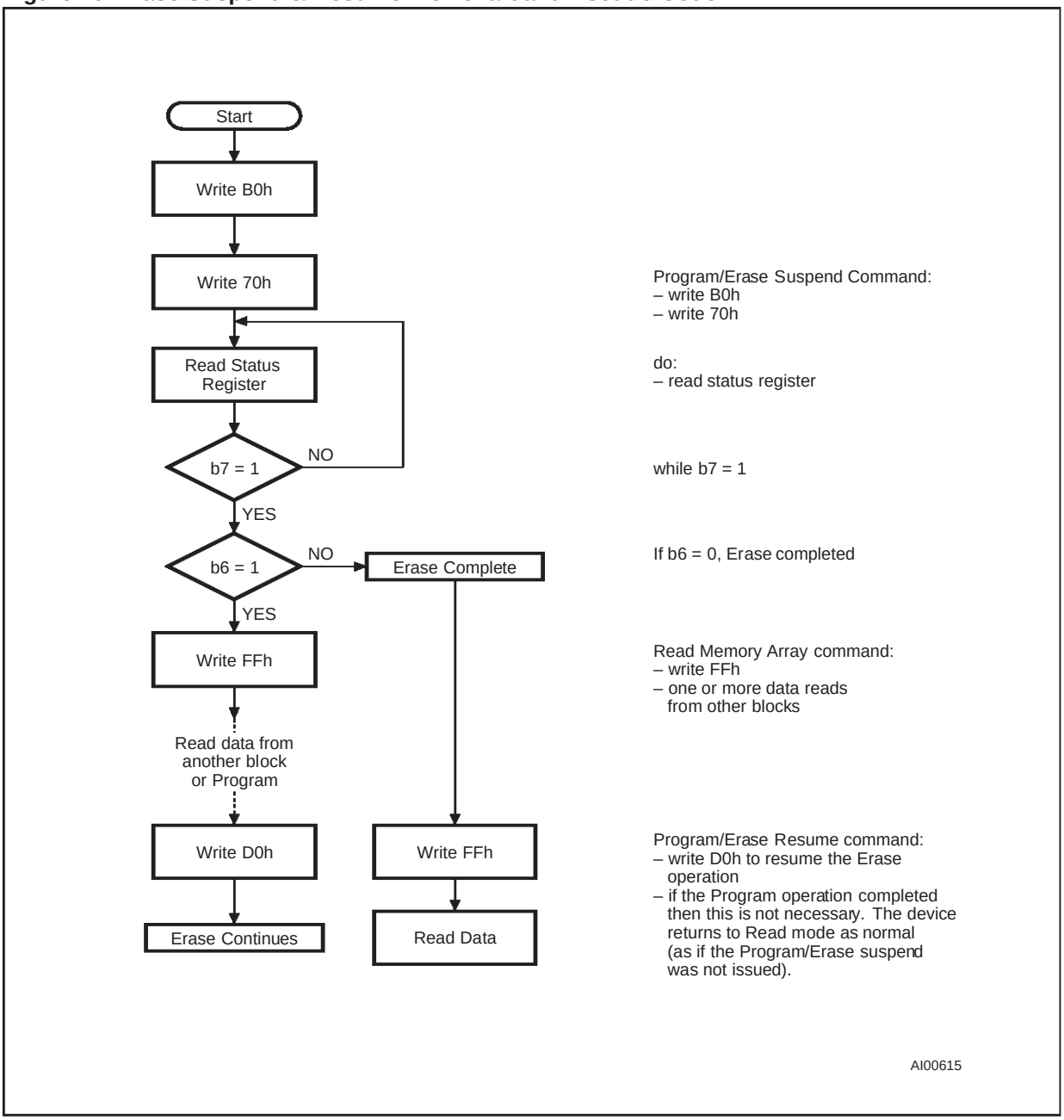
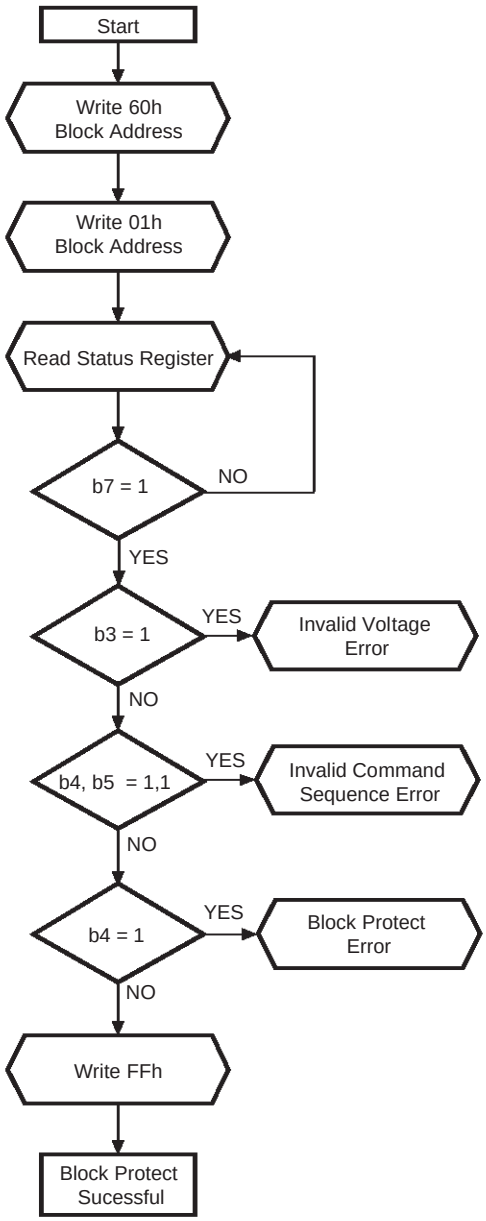


Figure 27. Block Protect Flowchart and Pseudo Code



Block Protect Command
– write 60h, Block Adress
– write 01h, Block Adress

do:
– read status register

while b7 = 1

If b3 = 1, Invalid Voltage Error

If b4 = 1, b5 = 1 Invalid Command Sequence Error

If b4 = 1, Block Protect Error

Read Memory Array Command:
– write FFh

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Figure 28. Block Unprotect Flowchart and Pseudo Code

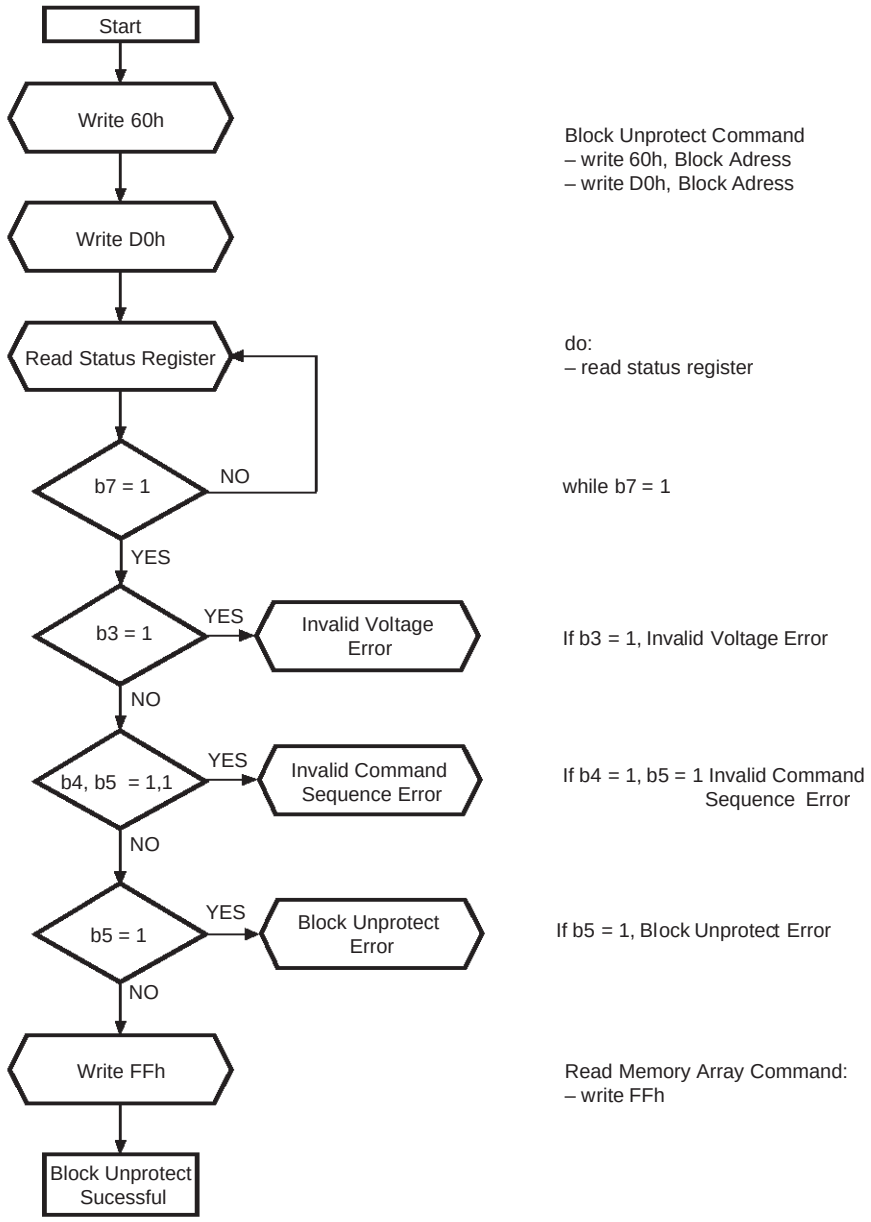
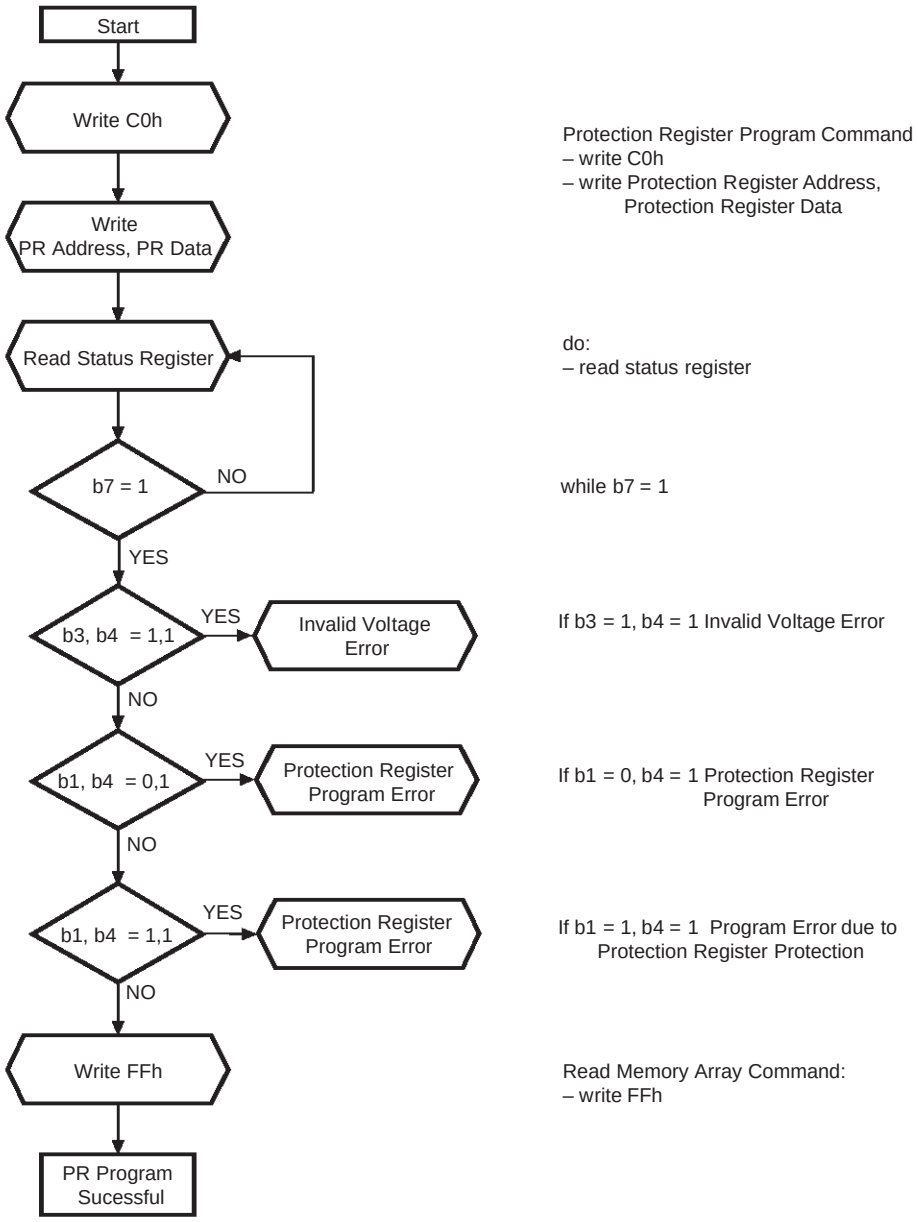


Figure 29. Protection Register Program Flowchart and Pseudo Code



Note: PR = Protection Register

Figure 30. Command Interface and Program Erase Controller Flowchart (a)

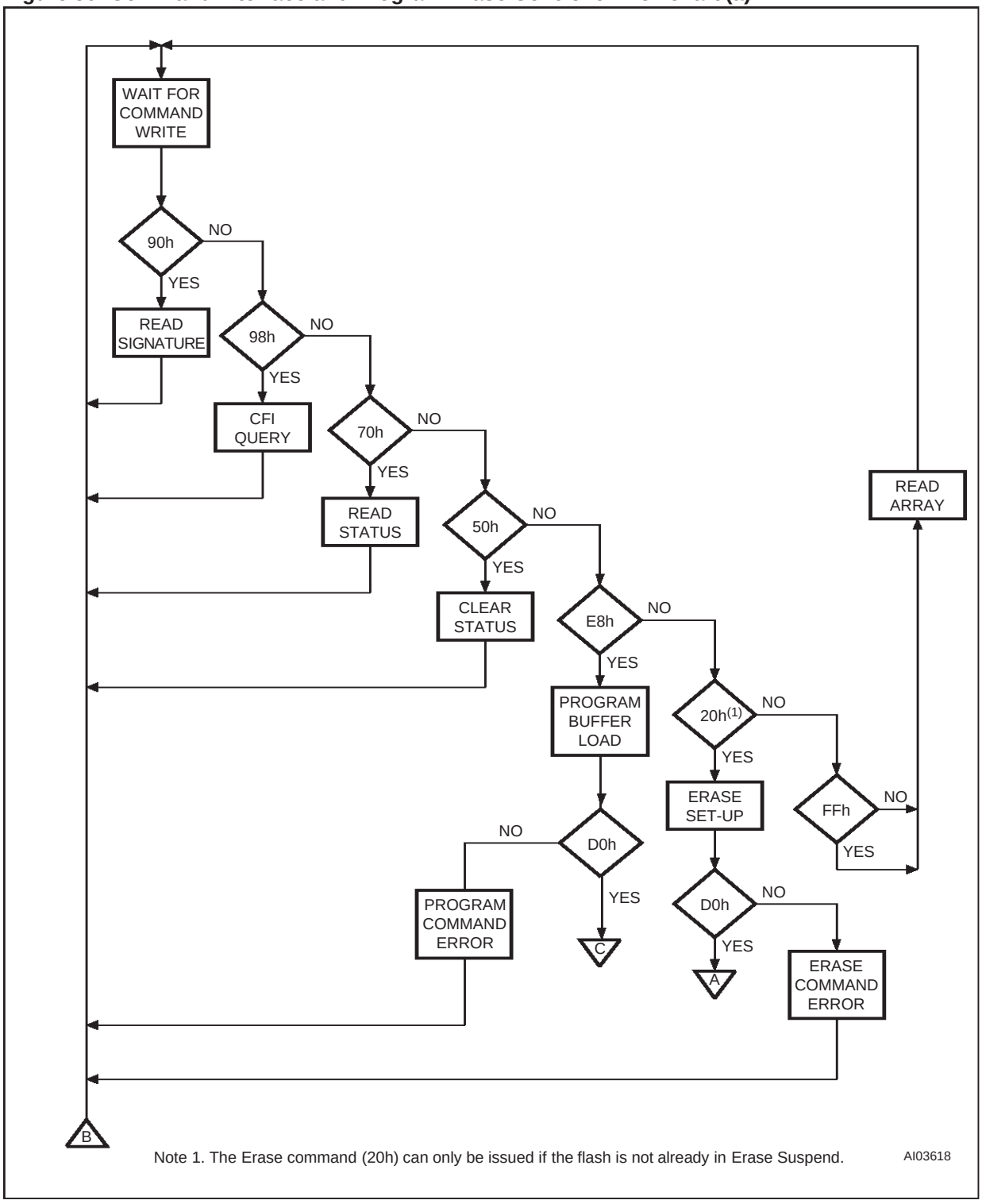


Figure 31. Command Interface and Program Erase Controller Flowchart (b)

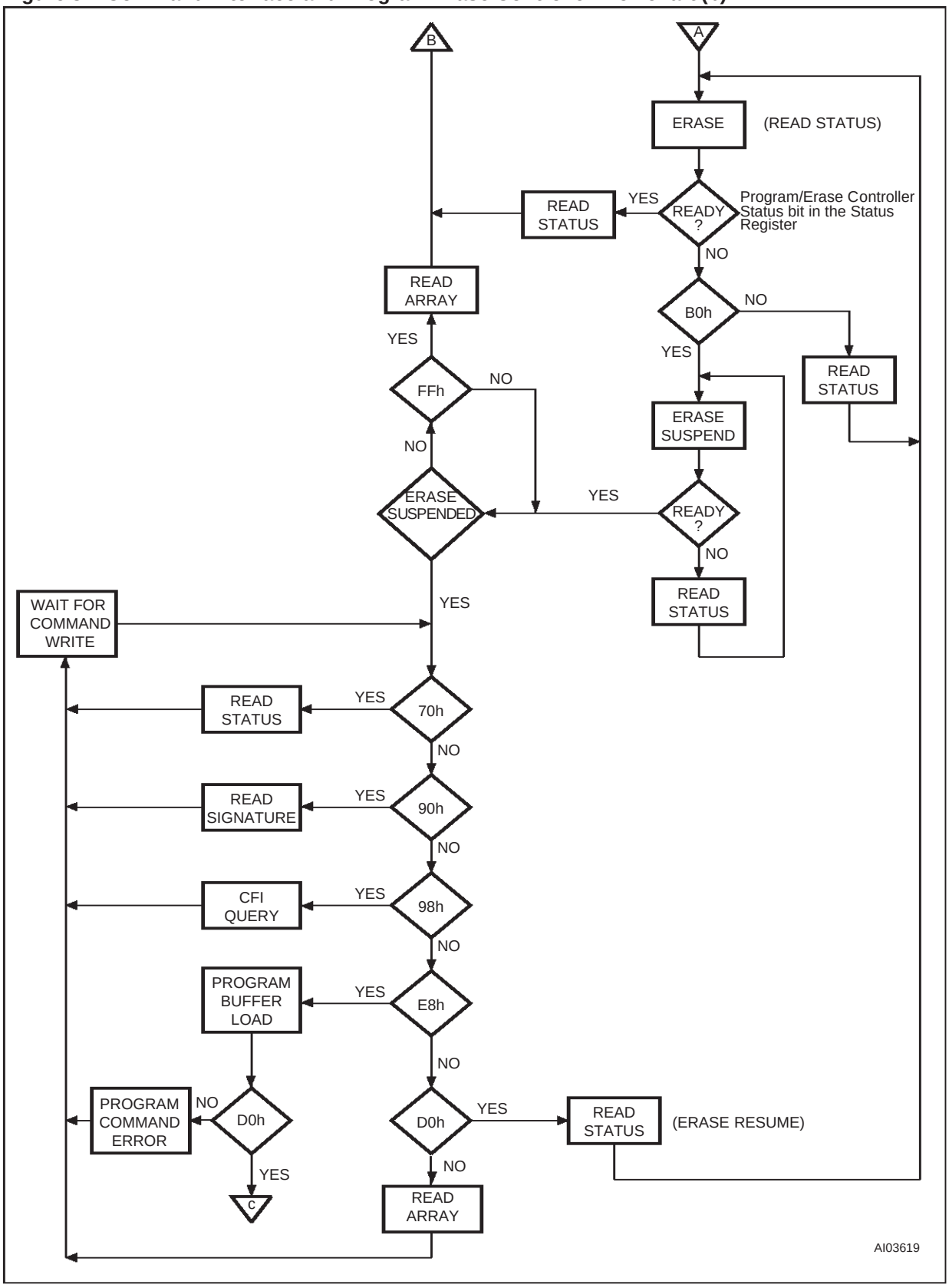
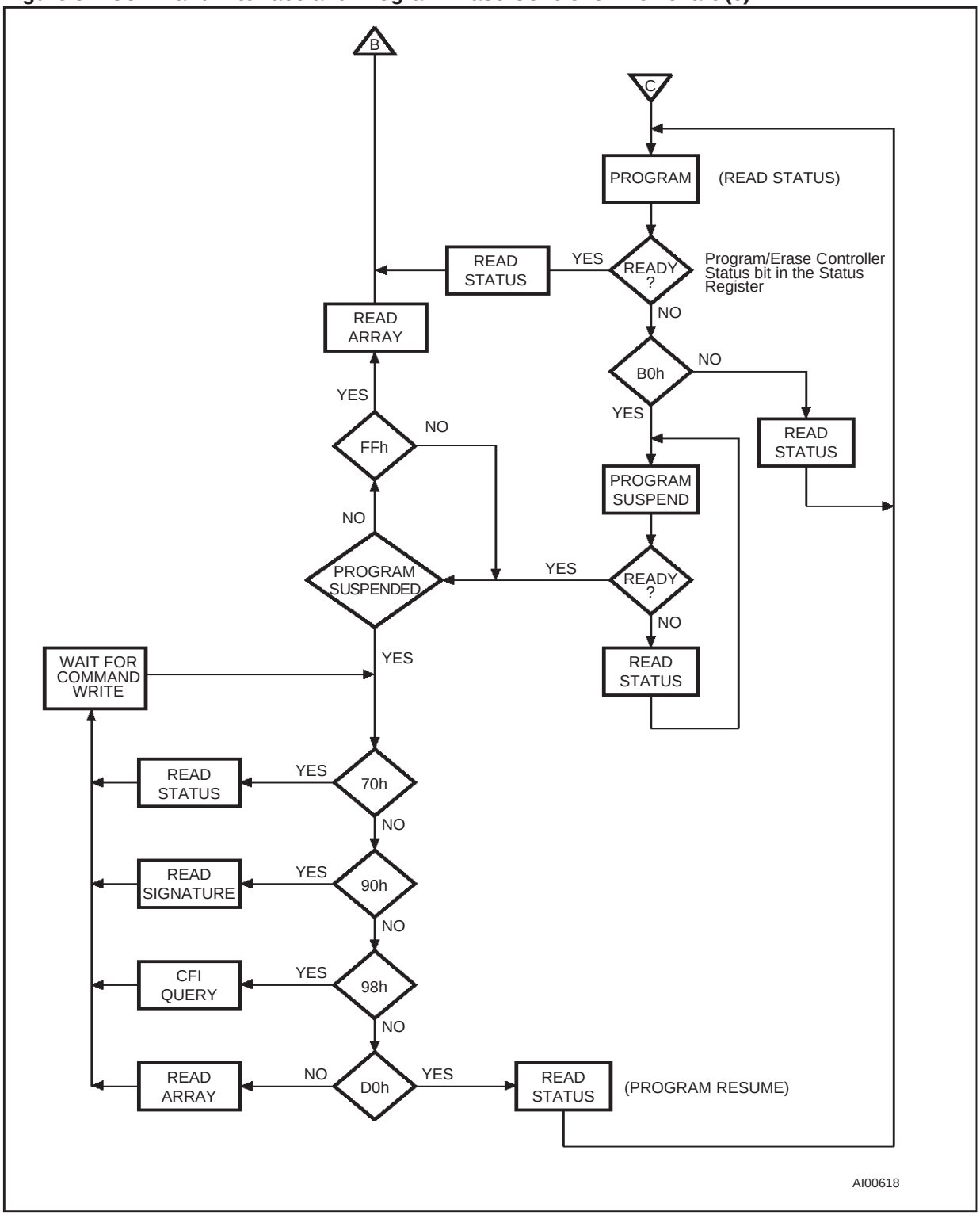


Figure 32. Command Interface and Program Erase Controller Flowchart (c).



REVISION HISTORY

Table 33. Document Revision History

Date	Version	Revision Details
11-Mar-2002	-01	First Issue (Data Brief)
10-Jul-2002	-02	Document expanded to full Product Preview
06-Aug-2002	2.1	Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 02 equals 2.0). Word Effective Programming Time modified. Program Write Buffer and Block Erase Time parameters modified in Table 10. Speed Class 90ns added. V_{DD}, V_{DDQ}, V_{SS} and V_{SSQ} signal descriptions modified.
02-Sep-2002	2.2	Figure 12, Asynchronous Latch Controlled Bus Read AC Waveforms**,** modified.
16-Dec-2002	2.3	REVISION HISTORY moved to after the appendices. Table 10, Program, Erase Times and Program Erase Endurance Cycles table modified. All DU connections changed to NC in Table 4, TBGA64 Connections (Top view through package). V_{IL} max and V_{IH} min modified in Table 15, DC Characteristics. Block Protect setup command address modified in Table 6, Commands. Data and Descriptions clarified in CFI Table 32, Extended Query information.

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