

STSJ20NM20N

N-CHANNEL 200V - 0.11Ω - 20A PowerSO-8™ ULTRA LOW GATE CHARGE MDmesh™II MOSFET

TARGET DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STSJ20NM20N	200 V	< 0.13 Ω	20 A

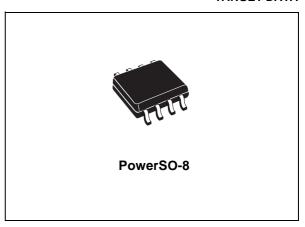
- WORLDWIDE LOWEST GATE CHARGE
- TYPICAL $R_{DS}(on) = 0.11 \Omega$
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- LOW INPUT CAPACITANCE
- LOW GATE RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTORING YIELDS

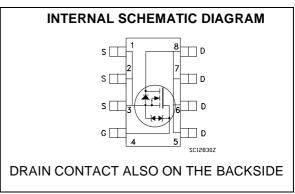
DESCRIPTION

This 200V MOSFET with a new advanced layout brings all unique advantages of MDmesh technology to lower voltages. The device exhibits worldwide lowest gate charge for any given on-resistance. Its use is therefore ideal as primary switch in isolated DC-DC converters for Telecom and Computer applications. Used in combination with secondary-side low-voltage STripFETTM products, it contributes to reducing losses and boosting efficiency. The exposed slug reduced the Rthj-c improving the current capability

APPLICATIONS

The MDmesh[™] family is very suitable for increasing power density allowing system miniaturization and higher efficiencies.





ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STSJ20NM20N	SJ20NM20N	PowerSO-8	TAPE & REEL

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	200	V
V _{GS}	Gate-source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C Drain Current (continuous) at T _C = 100°C	20 12.5	A A
I _{DM} (2)	Drain Current (pulsed)	80	Α
P_{TOT} Total Dissipation at $T_C = 25^{\circ}C$ P_{TOT} Total Dissipation at $T_C = 25^{\circ}C$ (1)		70 3	W W
dv/dt (3)	Peak Diode Recovery voltage slope	10	V/ns

THERMAL DATA

Rthj-c	Thermal Resistance Junction-case Max	1.8	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max (1)	42	°C/W
Tj	Max. Operating Junction Temperature	150	°C
T _{stg}	Storage Temperature	- 55 to 150	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	TBD	А
E _{AS} Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 35 V)		TBD	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	200			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_{C} = 125 °C			1 10	μA μA
IGSS	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 30V			100	nA
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	3.5	4.2	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 2 A		0.11	0.13	Ω

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ELECTRICAL CHARACTERISTICS (CONTINUED)

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (4)	Forward Transconductance	V _{DS} = 15 V _, I _D = 2 A		1.4		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		670 180 12		pF pF pF
Coss eq. (*)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 400V		TBD		pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		TBD		Ω

^(*) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V_{DD} = 100 V, I_{D} = 2 A R_{G} = 4.7 Ω V _{GS} = 10 V (see test circuit, Figure 3)		TBD TBD		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 160 \text{ V}, I_D = 4 \text{ A},$ $V_{GS} = 10 \text{ V}$		19 3.5 11		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{r(Voff)}	Off-Voltage Rise Time	$V_{DD} = 100 \text{ V}, I_D = 2 \text{ A},$		TBD		ns
`t _f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$		TBD		ns
t _c	Cross-Over Time	(see test circuit, Figure 3)		TBD		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				20 80	A A
V _{SD} (4)	Forward On Voltage	I _{SD} = 2 A, V _{GS} = 0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 2 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 25°C (see test circuit, Figure 5)		89 300 6.5		ns nC A
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 2 A, di/dt = 100 A/ μ s, V_{DD} = 100 V, T_j = 150°C (see test circuit, Figure 5)		TBD TBD TBD		ns nC A

Note: 1. When mounted on FR4 Board with 1inch² pad, 2oz of Cu, $t \le 10$ sec.

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 Pulse width limited by safe operating area
 I_{SD} ≤ 20A, di/dt ≤ 400A/µs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ T_{JMAX}
 Pulsed: Pulse duration = 400 µs, duty cycle 1.5 %

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Fig. 1: Unclamped Inductive Load Test Circuit

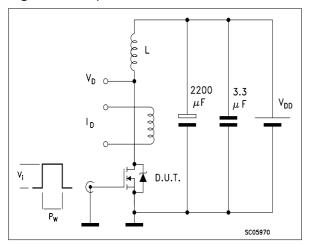


Fig. 3: Switching Times Test Circuit For Resistive Load

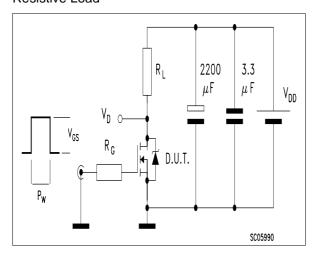


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

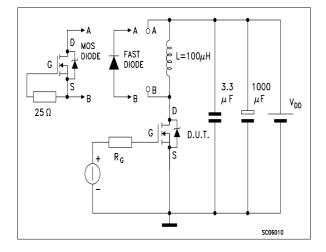


Fig. 2: Unclamped Inductive Waveform

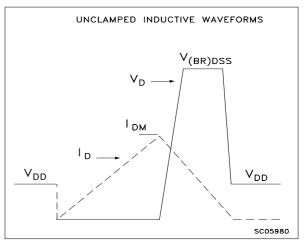
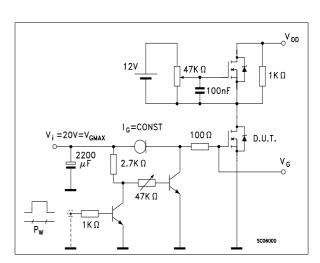


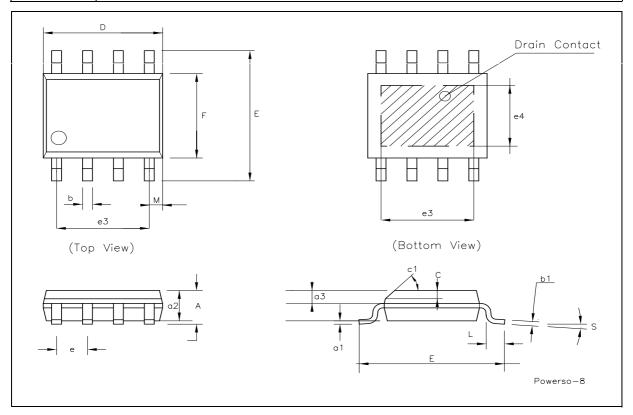
Fig. 4: Gate Charge test Circuit



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PowerSO-8™ MECHANICAL DATA

DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
а3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45°	(typ.)		
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S			8° (max.)		



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