



STL27N15

N-CHANNEL 150V - 0.045 Ω - 27A PowerFLAT™ LOW GATE CHARGE STripFET™ MOSFET

TARGET DATA

TYPE	V _{DS}	R _{DS(on)}	I _D
STL15N15	150 V	<0.060 Ω	27 A ⁽¹⁾

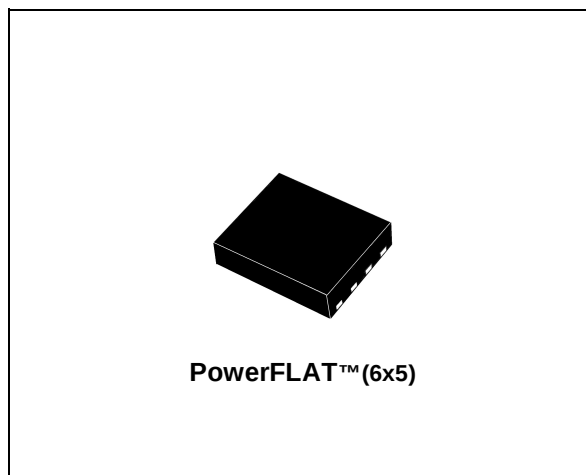
- TYPICAL R_{DS(on)} = 0.045 Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- VERY LOW GATE CHARGE

DESCRIPTION

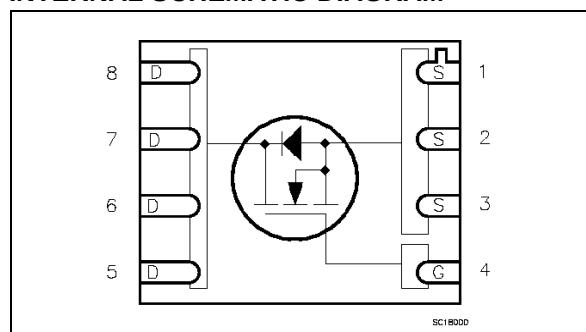
This MOSFET series realized with STMicroelectronics unique "STripFET™" process has specifically been designed to minimize input capacitance and gate charge. It's therefore suitable as primary switch in advanced high efficiency, high frequency isolated DC-DC converter for telecom and computer application. The new PowerFLAT™ package allows a significant reduction in a board space without compromising performance.

APPLICATIONS

- HIGH-EFFICIENCY ISOLATED DC-DC CONVERTERS
- TELECOM AND BATTERY CHARGER ADAPTOR
- SYNCHRONOUS RECTIFICATION



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STL27N15	L27N15	PowerFLAT	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	150	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	150	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C (Steady State)	6	A
I _D	Drain Current (continuous) at T _C = 100°C	4	A
I _{DM} ⁽³⁾	Drain Current (pulsed)	24	A
P _{tot} ⁽²⁾	Total Dissipation at T _C = 25°C (Steady State)	4	W
P _{tot} ⁽¹⁾	Total Dissipation at T _C = 25°C	80	W
	Derating Factor	0.03	W/°C
dv/dt ⁽⁵⁾	Peak Diode Recovery voltage slope	TBD	V/ns
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Operating Junction Temperature		

June 2003

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This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice

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THERMAL DATA

Rthj-F	Thermal Resistance Junction-Foot (Drain)	1.56	°C/W
Rthj-pcb(2)	Thermal Operating Junction-pcb	31.2	°C/W

ELECTRICAL CHARACTERISTICS ($T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{\text{GS}} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{\text{GS}} = 0$)	$V_{\text{DS}} = \text{Max Rating}$ $V_{\text{DS}} = \text{Max Rating}$ $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{\text{DS}} = 0$)	$V_{\text{GS}} = \pm 20\text{ V}$			± 100	nA

ON (6)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$ $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{\text{DS(on)}}$	Static Drain-source On Resistance	$V_{\text{GS}} = 10\text{ V}$ $I_D = 3\text{ A}$		0.045	0.060	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (6)	Forward Transconductance	$V_{\text{DS}} = 50\text{ V}$ $I_D = 5\text{ A}$		TBD		S
C_{iSS} C_{oSS} C_{rSS}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0$		TBD TBD TBD		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 50\text{ V}$ $I_D = 3\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		TBD TBD		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 50\text{ V}$ $I_D = 6\text{ A}$ $V_{GS} = 10\text{ V}$		TBD TBD TBD	28	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 50\text{ V}$ $I_D = 3\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		TBD TBD		ns ns

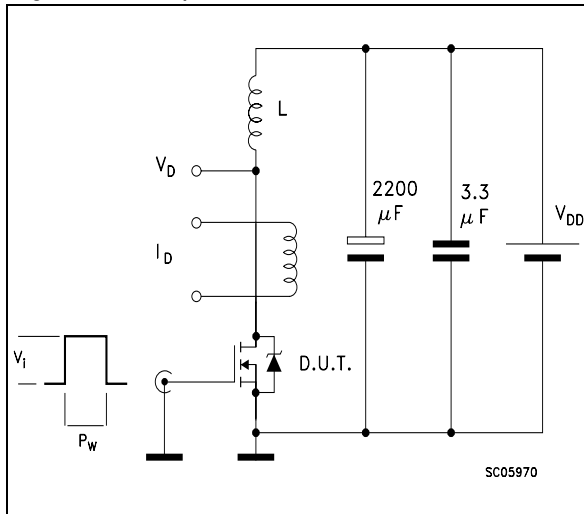
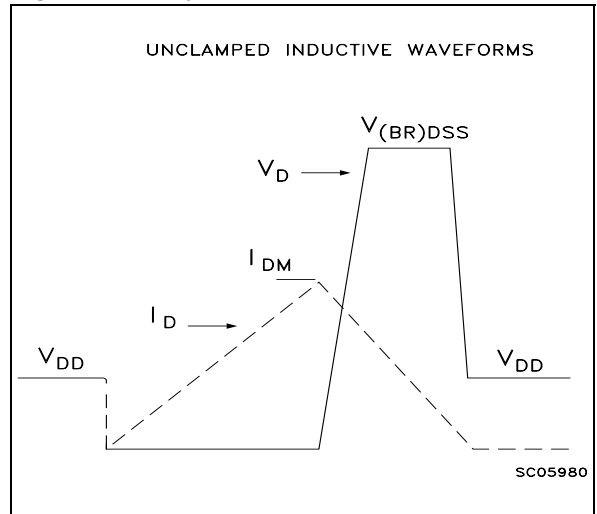
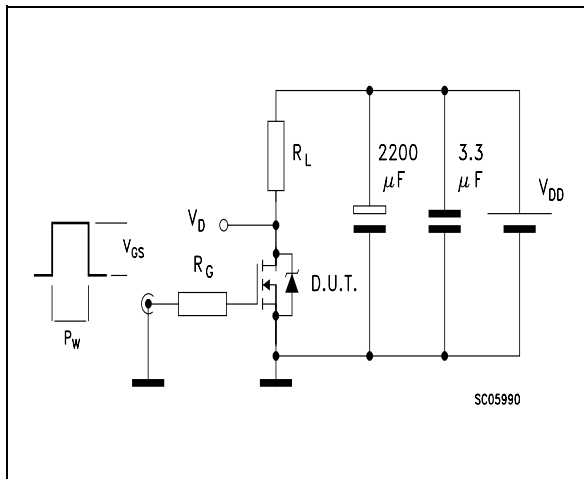
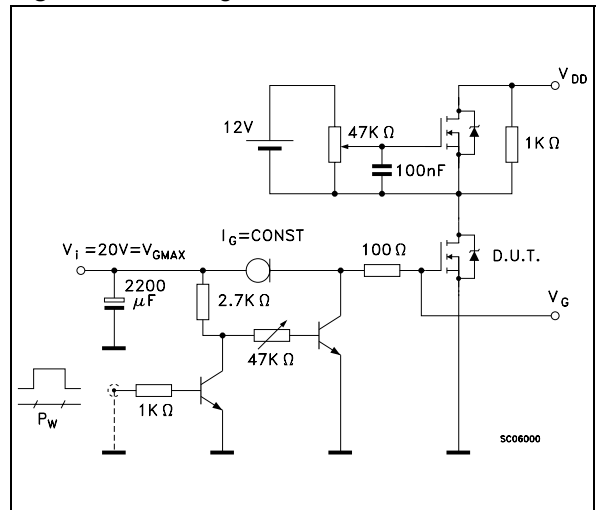
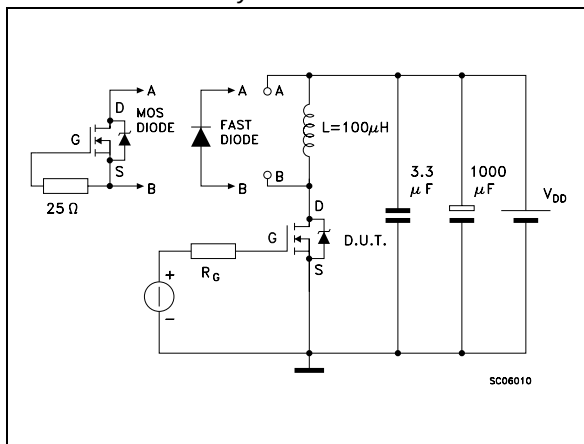
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(3)}$	Source-drain Current Source-drain Current (pulsed)				6 24	A A
$V_{SD}^{(6)}$	Forward On Voltage	$I_{SD} = 3\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 6\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		TBD TBD TBD		ns nC A

(1) The value is rated according R_{thj-F} .(2) When Mounted on FR-4 board of 1 inch², 2oz Cu

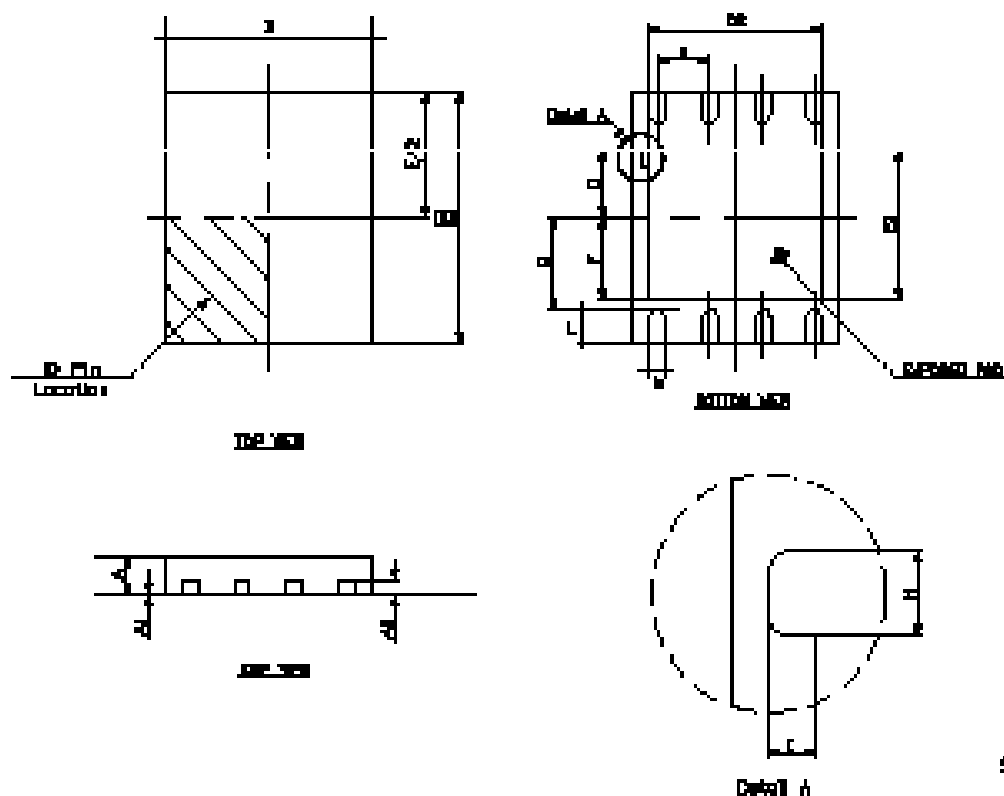
(3) Pulse width limited by safe operating area.

(5) $I_{SD} \leq 6\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.(6) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Fig. 1: Unclamped Inductive Load Test Circuit**Fig. 2: Unclamped Inductive Waveform****Fig. 3: Switching Times Test Circuits For Resistive Load****Fig. 4: Gate Charge test Circuit****Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**

PowerFLAT™(6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80		1.00	0.031		0.039
A1		0.02			0.001	
b	0.35		0.47	0.014		0.018
C		1.61			0.063	
D		5.00			0.197	
D2	4.15		4.25	0.163		0.167
E		6.00			0.236	
E2	3.55		3.65	0.140		0.144
e		1.27			0.049	
F		1.99			0.078	
G		2.20			0.086	
H		0.40			0.015	
I		0.219			0.0086	
L	0.70		0.90	0.028		0.035



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