256-Position One-Time Programmable Dual-Channel I²C Digital Potentiometer

Preliminary Technical Data — AD5172/AD5173

FEATURES

2-Channel, 256-position
OTP(One-Time Programmable) Set-and-Forget Resistance Setting — low cost alternative over EEMEM
Unlimited adjustments prior to OTP activation
OTP overwriting function allows temporary adjustments[1]
End-to-end resistance 2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Compact MSOP-10 (3 mm × 4.9 mm) Package
Low tempco 5 ppm/°C in potentiometer mode
Low tempco 35 ppm/°C in rheostat mode
Fast Settling Time: t_S = 5µs Typ in Power-Up
Full read/write of wiper register
Power-on preset to midscale[1]
Extra package address decode pins AD0 and AD1(AD5173)
Computer Software Replaces µC in Factory Programming Applications
6 V one-time programming voltage
Single supply 2.7 V to 5.5 V
Low power, I_{DD} = 5 µA
Wide operating temperature –40°C to +125°C

APPLICATIONS

Systems Calibrations
Mechanical Potentiometers and Trimmers® Replacements
Transducer adjustment
RF amplifier biasing
Automotive electronics adjustment
Gain control and offset adjustment
Electronics Level Settings

GENERAL OVERVIEW

The AD5172/73 are dual channel 256-position, one-time programmable (OTP) digital potentiometers[2], which employ fuse link technology to achieve the memory retention of resistance setting function. OTP is a cost-effective alternative over the EEMEM approach for users who do not need to program the digital potentiometer setting in memory for more than once. These devices perform the same electronic adjustment functions like most mechanical trimmers and variable resistors do but offer enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

The AD5172/73 are programmed using a 2-wire I²C compatible digital control. They allow unlimited adjustments before permanently setting the resistance value. During the OTP activation, a permanent fuse blown command is sent after the final value is determined; therefore freezing the wiper position at a given setting (analogous to placing epoxy on a mechanical trimmer). Unlike other OTP digital potentiometers in the same family, AD5172/73 have unique temporary OTP overwriting feature that new adjustments if desired but the OTP setting is restored during subsequent power up conditions. To verify the success of permanent programming, Analog Devices patterned the OTP validation such that the fuse status can be discerned from two validation bits in read mode.

For applications that program AD5172/73 in the factories, Analog Devices offers a device programming software, which operates across Windows® 95 to XP® platforms including Windows NT®. This software application effectively replaces the need for external I²C controllers or host processors and therefore significantly reduces users' development time.

An AD5172/73 evaluation kit is available, which include the software, connector, and cable that can be converted for the factory programming applications.

The AD5172/73 are available in a MSOP-10 package. All parts are guaranteed to operate over the automotive temperature range of –40°C to +125°C. Besides their unique OTP features, the AD5172/73 lend themselves well to other general-purpose digital potentiometer applications due to their programmable preset, superior temperature stability, and small form factor.

FUNCTIONAL BLOCK DIAGRAMS

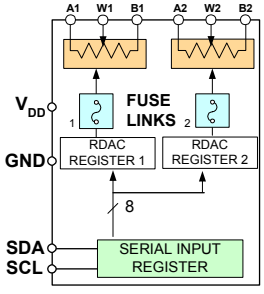

Figure 1. AD5172

Rev. PrF 8/14/03

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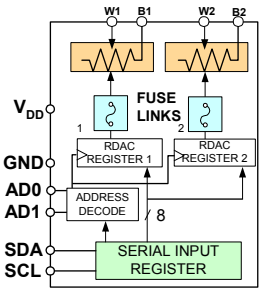

Figure 2. AD5173

Note:
1. New adjustments are allowed even after OTP is achieved but the permanent setting will always be restored during subsequent power up cycles. This feature allows users to use these digital potentiometers as volatile pots with programmable preset.
2. The terms *digital potentiometer*, *VR*, and *RDAC* are used interchangeably.

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REVISION HISTORY

Revision Pr F: Initial Version

ELECTRICAL CHARACTERISTICS—2.5 kΩ VERSION

(V_{DD} = 5 V ± 10%, or 3 V ± 10%; V_A = +V_{DD}; V_B = 0 V; –40°C < T_A < +125°C; unless otherwise noted.)

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	–1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	–4	±0.75	+4	LSB
Nominal Resistor Tolerance[3]	$\Delta R_{AB}/R_{AB}$	T_A = 25°C	–30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	V_{AB} = V_{DD}, Wiper = no connect		35		ppm/°C
Wiper Resistance	R_W			50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all RDACs)						
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		–1.5	±0.1	+1.5	LSB
Integral Nonlinearity[4]	INL		–1.5	±0.6	+1.5	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	–6	–2.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+2	+6	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Normal Operating Supply Voltage	V_{DD}		2.7		5.5	V
OTP Supply Voltage[8]	V_{DD_OTP}	T_A = 25°C				
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	5	µA
OTP Supply Current[9]	I_{DD_OTP}	V_{DD_OTP}=6V, T_A = 25°C	100			mA
Power Dissipation[10]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, Code = Midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 10, 11]						
Bandwidth –3dB	BW_2.5K	R_{AB} = 2.5 kΩ, Code = 0x80		2.4		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A= 5 V, V_B = 0 V, ±1 LSB error band, R_{WB} = 2.5 kΩ		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 2.5 kΩ, RS = 0		4.5		nV/√Hz

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; –40°C < T_A < +125°C; unless otherwise noted.)

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, A = no connect	–1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, A = no connect	–2	±0.25	+2	LSB
Nominal Resistor Tolerance[3]	$\Delta R_{AB}/R_{AB}$	T_A = 25°C	–30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, Wiper = no connect		35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V		50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL	R_{WB}, A = no connect	–1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL	R_{WB}, A = no connect	–1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	–3	–1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+1	+3	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Normal Operating Supply Voltage	V_{DD}		2.7		5.5	V
OTP Supply Voltage[8]	V_{DD_OTP}	T_A = 25°C	6		6.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	5	µA
OTP Supply Current[9]	I_{DD_OTP}	V_{DD_OTP}=6V, T_A = 25°C	100			mA
Power Dissipation[10]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, Code = Midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 10, 11]						
Bandwidth –3dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, Code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band, R_{WB} = 5 kΩ		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, RS = 0		9		nV/√Hz

TIMING CHARACTERISTICS—2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = +5V ± 10%, or +3V ± 10%; $V_A = V_{DD}$; V_B = 0 V; –40°C < T_A < +125°C; unless otherwise noted.)

Table 3.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
I²C INTERFACE TIMING CHARACTERISTICS[6, 11] (Specifications Apply to All Parts)						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated START)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for Repeated START Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

NOTES
[1] Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, Wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. VA = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[8]Different from operating power supply, power supply for OTP is used one-time only.
[9]Different from operating current, supply current for OTP lasts approximately 400 ms for one-time needed only.
[10]Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value result in the minimum overall power consumption.
[11]All dynamic characteristics use V_{DD} = 5 V.
[12]Different from settling time after fuse is blown. The OTP settling time occurs once only

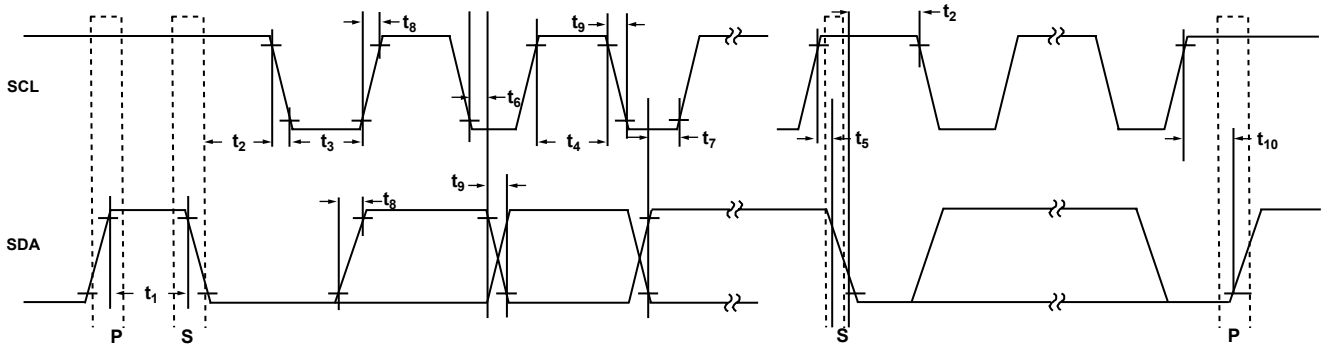

Figure 3. I²C Interface Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C, unless otherwise noted.)

Table 4.

Parameter	Value
V_{DD} to GND	–0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
I_{MAX}[1]	±20 mA
Digital Inputs and Output Voltage to GND	0 V to +7 V
Operating Temperature Range	–40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2] θ_{JA}: MSOP-10	230°C/W

NOTES

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = $(T_{JMAX} – T_A)/\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

PIN CONFIGURATION

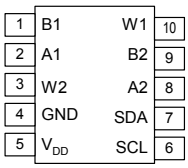

Figure 4.- AD5172 Pin Configuration

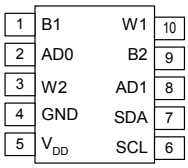

Figure 5. – AD5173 Pin Configuration

PIN FUNCTION DESCRIPTIONS

Table 5.

Pin	Name	Description
1	B1	B1 Terminal. GND ≤ V_{B1} ≤ V_{DD}
2	A1	A1 Terminal. GND ≤ V_{A1} ≤ V_{DD}
3	W2	W2 Terminal. GND ≤ V_{W2} ≤ V_{DD}
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, V_{DD} needs to be a minimum of 6 V and 100 mA driving capability.
6	SCL	Serial Clock Input. Positive edge triggered. Requires pull-up resistor
7	SDA	Serial Data Input/Output. Requires pull-up resistor
8	A2	A2 Terminal. GND ≤ V_{A2} ≤ V_{DD}
9	B2	B2 Terminal. GND ≤ V_{B2} ≤ V_{DD}
10	W1	W1 Terminal. GND ≤ V_{W1} ≤ V_{DD}

Table 6.

Pin	Name	Description
1	B1	B1 Terminal. GND ≤ V_{B1} ≤ V_{DD}
2	AD0	Programmable address bit 0 for multiple package decoding. AD0 and AD1 allow maximum of four AD5173s to be addressed
3	W2	W2 Terminal. GND ≤ V_{W2} ≤ V_{DD}
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, V_{DD} needs to be a minimum of 6 V and 100 mA driving capability.
6	SCL	Serial Clock Input. Positive edge triggered. Requires pull-up resistor
7	SDA	Serial Data Input/Output. Requires pull-up resistor
8	AD1	Programmable address bit 1 for multiple package decoding. AD0 and AD1 allow maximum of four AD5173s to be addressed
9	B2	B2 Terminal. GND ≤ V_{B2} ≤ V_{DD}
10	W1	W1 Terminal. GND ≤ V_{W1} ≤ V_{DD}

TYPICAL PERFORMANCE CHARACTERISTICS

Figures 6 to 25

THEORY OF OPERATION

The AD5172/73 allow unlimited 8-bit adjustments, except for one-time programmable, set-and-forget resistance setting. OTP technology is a proven cost-effective alternative over EEMEM in one-time memory programming applications. AD5172/73 employ fuse link technology to achieve the memory retention of the resistance setting function. It comprises eight data fuses, which control the address decoder for programming the RDAC, one user mode test fuse for checking setup error, and one programming lock fuse for disabling any further programming once the data fuses are blown.

ONE-TIME PROGRAMMING (OTP)

Prior to OTP activation, the AD5172/73 preset to midscale during power on. After the wiper is set at the desired position, the resistance can be permanently set by programming the T bit to high along with the proper coding (Tables 10 and 11).

The device control circuit has two validation bits, E1 and E0, that can be read back in the read mode for checking the programming status as shown in Table 7.

Table 7. Validation Status

E1	E0	Status
0	0	Ready for Programming
0	1	Test Fuse Not Blown Successfully. (For factory setup checking purpose only. Users should not see these combinations.)
1	0	Error. Some fuses are not blown. Try again.
1	1	Successful. No further programming is possible.

When the OTP T bit is set, the internal clock is enabled. The program will attempt to blow a test fuse. The operation stops if this fuse is not blown properly. The validation Bits E1 and E0 show 01, and the users should check the setup. If the test fuse is blown successfully, the data fuses will be programmed next. The eight data fuses will be programmed in eight clock cycles. The output of the fuses is compared with the code stored in the DAC register. If they do not match, E1 and E0 = 10 is issued as a error and the operation stops. Users may retry with the same codes. If the output and stored code match, the programming lock fuse will be blown so that no further programming is possible. In the meantime, E1 and E0 will issue 11 indicating the lock fuse is blown successfully. All the fuse latches are enabled at power-on and therefore the output corresponds to the stored setting from this point on. Figure26 shows a detailed functional block diagram.

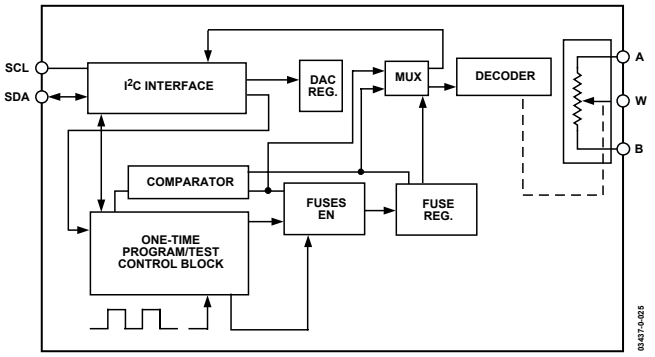

Figure26. Detailed Functional Block Diagram

DETERMINING THE VARIABLE RESISTANCE AND VOLTAGE

Rheostat Mode Operation

If only the W-to-B or W-to-A (AD5172 only) terminals are used as variable resistors, the unused terminal can be opened or shorted with W. This operation is called rheostat mode (Figure27).

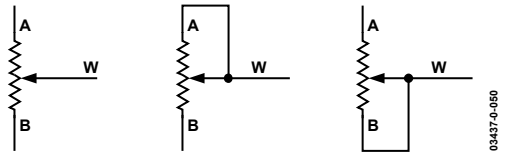

Figure27. Rheostat Mode Configuration

The nominal resistance (R_{AB}) of the RDAC has 256 contact points accessed by the wiper terminal, plus the B terminal contact if R_{WB} is considered. The 8-bit data in the RDAC latch is decoded to select one of the 256 settings. Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Such connection yields a minimum of 60 Ω resistance between terminals W and B because of the 60 Ω wiper contact resistance. The second connection is the first tap point, which corresponds to 219 Ω ($R_{WB} = (1) \times R_{AB}/256 + R_W$) for data 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10060 Ω ($(256) \times R_{AB}/256 + R_W$). Figure 28 shows a simplified diagram of the equivalent RDAC circuit. The general equation determining R_{WB} is

$$R_{WB}(D) = \frac{D}{256} R_{AB} + R_W \qquad (1)$$

where:

D is the decimal equivalent of the 8-bit binary code.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on-resistance of the internal switch.

Table 8. R_{WB} vs. Codes; R_{AB} = 10 kΩ and the A Terminal Is Opened

D (Dec)	R_{WB} (Ω)	Output State
255	9,961	Full Scale (R_{AB} – 1 LSB + R_W)
128	5,060	Midscale
1	99	1 LSB
0	60	Zero Scale (Wiper Contact Resistance)

Since a finite wiper resistance of 60 Ω is present in the zero-scale condition, care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a complementary resistance R_{WA} (AD5172 only). When these terminals are used, the B terminal can be opened or shorted to W. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} R_{AB} + R_W \quad \text{(AD5172 only)} \quad (2)$$

Table 9. R_{WA} vs. Codes; R_{AB} =10 kΩ and B Terminal Is Opened

D (Dec)	R_{WA} (Ω)	Output State
255	99	Full Scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero Scale

The typical distribution of the resistance tolerance from device to device is process lot dependent, and it is possible to have ±30% tolerance.

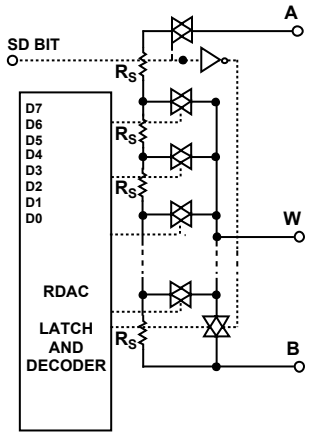

Figure 28. Equivalent RDAC Circuit (A terminal for AD5172 only)

Potentiometer Mode Operation (AD5172 only)

If all three terminals are used, the operation is called the potentiometer mode. The most common configuration is the voltage divider operation (Figure 29).

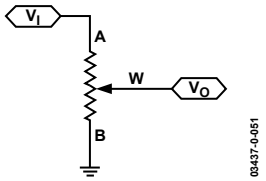

Figure 29. Potentiometer Mode Configuration

The transfer function can be found as

$$V_W(D) = \frac{\frac{D}{256} R_{AB} + R_W}{R_{AB} + 2R_W} V_A \quad \text{(AD5172 only)} \quad (3)$$

If we ignore the effect of the wiper resistance, the transfer function is simply

$$V_W(D) = \frac{D}{256} V_A \quad \text{(AD5172 only)} \quad (4)$$

Unlike in rheostat mode operation where the absolute tolerance is high, potentiometer mode operation yields an almost ratio-metric function of D/256 with a relatively small error contributed by the R_W terms, and therefore the tolerance effect is almost cancelled. Although the thin film step resistor R_S and CMOS switches resistance R_W have very different temperature coefficients, the ratio-metric adjustment also reduces the overall temperature coefficient effect to 5 ppm/°C, except at low value codes where R_W dominates.

Potentiometer mode operations include others such as op amp input, feedback resistor networks, and other voltage scaling applications. A, W, and B terminals can in fact be input or output terminals provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed V_{DD} to GND.

ESD PROTECTION

Digital inputs SDA and SCL are protected with a series input resistor and parallel Zener ESD structures (Figure30).

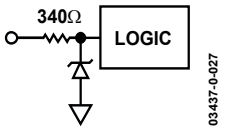

Figure30. ESD Protection of Digital Pins

TERMINAL VOLTAGE OPERATING RANGE

There are also ESD protection diodes between V_{DD} and the RDAC terminals. The V_{DD} of AD5172/73 therefore defines their voltage boundary conditions, see Figure31. Supply signals

present on terminals A, B, and W that exceed V_{DD} will be clamped by the internal forward-biased diodes and should be avoided.

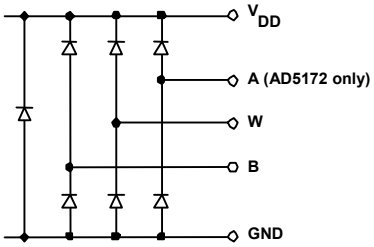

Figure31. Maximum Terminal Voltages Set by V_{DD}

POWER-UP/POWER-DOWN SEQUENCES

Similarly, because of the ESD protection diodes, it is important to power V_{DD} first before applying any voltages to terminals A, B, and W. Otherwise, the diode will be forward-biased such that V_{DD} will be powered unintentionally and may affect the rest of the users' circuits. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}. Similarly, V_{DD} should be powered down last.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the one-time programming and normal operating voltages are applied to the same V_{DD} terminal of the AD5172/73. The AD5172/73 employs fuse link technology that requires 6V to blow the internal fuses to achieve a given setting. On the other hand, it operates at 2.7V-5.5V once the programming is completed. Such dual voltage requirement requires isolation between the supplies. The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 6 V and be able to handle 400 ms and 100 mA of transient current for one-time programming. Once programming completes, the 6 V, supply must be removed to allow normal operation at 2.7 V to 5.5 V. Figure 32 shows the simplest implementation using a jumper. This approach saves one voltage supply but draws additional current and requires manual configuration.

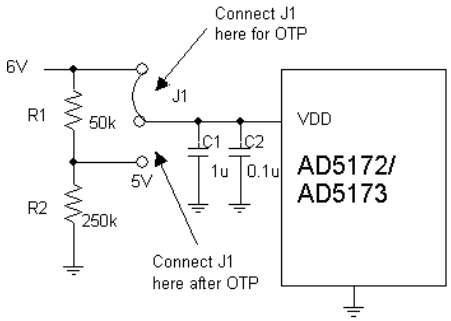

Figure 32. Power Supply Requirement

An alternate approach in 3.5V to 5.5V systems adds a signal diode between the system supply and the OTP supply for isolation as shown in Figure 33.

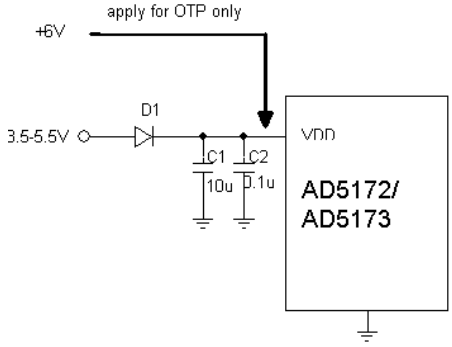

Figure 33. Isolate 6 V OTP supply from 3.5V-5.5V normal operating supply. The 6V supply must be removed once OTP is completed

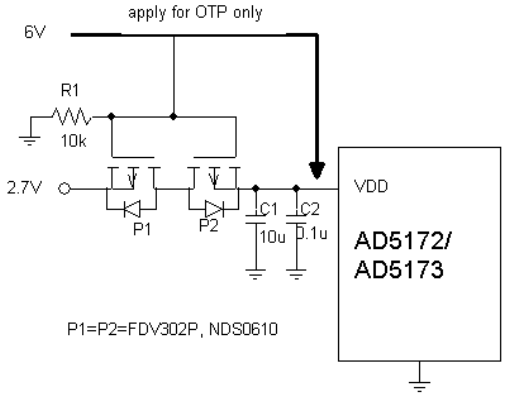

Figure 34. Isolate 6 V OTP Supply from 2.7V normal operating supply. The 6V supply must be removed once OTP is completed

For users who operate their systems at 2.7V, it is recommended to use the bi-directional low-threshold P-Ch MOSFETs for the supplies isolation. As shown in Figure 34, assumes the 2.7V system voltage is applied first but not the 6V, the gates of P1 and P2 are pulled to ground thus turns on P1 and subsequently P2. As a result, V_{DD} of AD5172/73 becomes 2.7V minus few tenths of mV drop across P1 and P2. When the AD5172/73 setting is found, the factory tester applies the 6V to V_{DD} and also the gates of P1 and P2 to turn them off. While the OTP command is executed at this time to program AD5172/73, the 2.7V source is therefore protected. Once the OTP is completed, the tester withdraws the 6V and AD5172/73's setting is permanently fixed.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 35). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

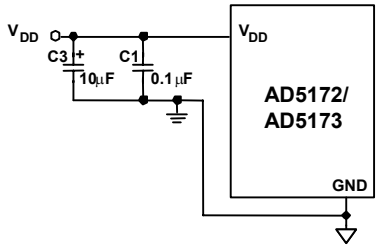

Figure 35. Power Supply Bypassing

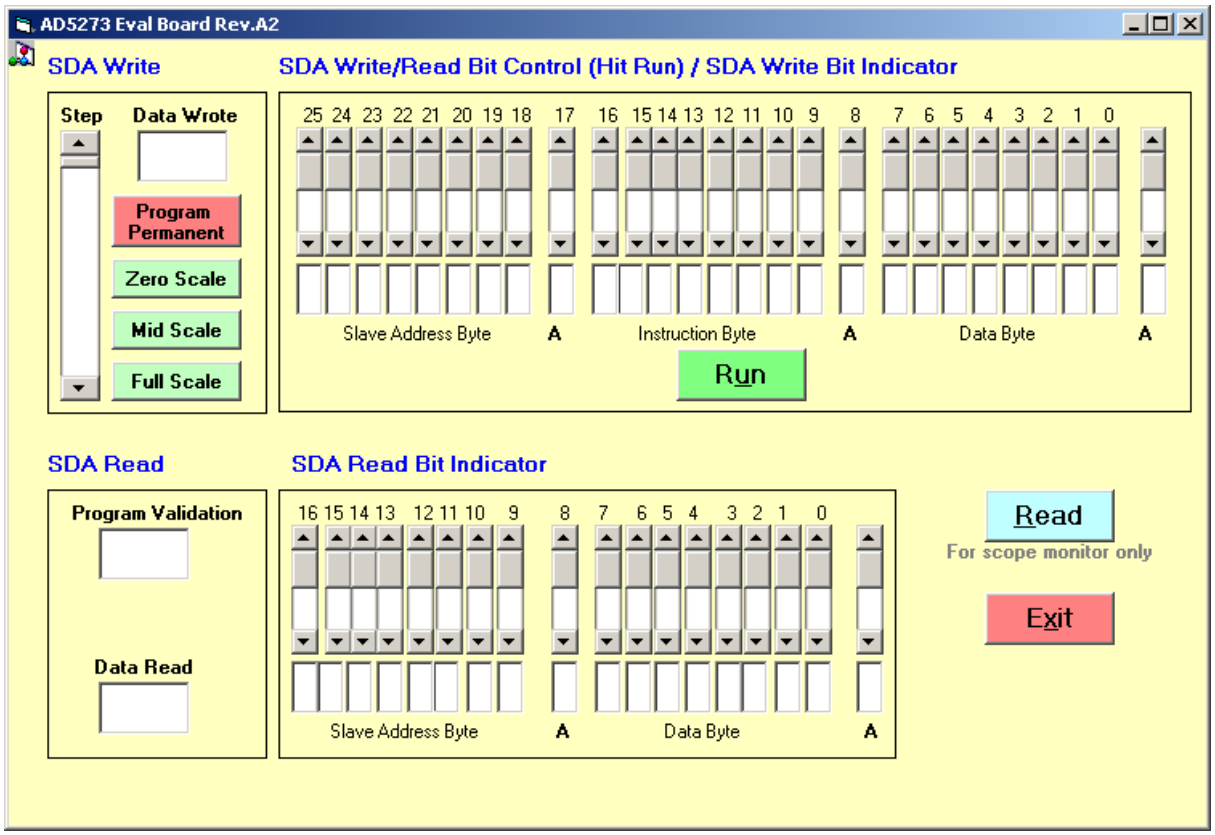

FIGURE 36. AD5172/73 COMPUTER SOFTWARE INTERFACE

CONTROLLING THE AD5172/73

There are two ways of controlling the AD5172/73. Users can either program the devices with computer software or external I²C controllers.

Software Programming

Due to the advantage of the one-time programmable feature, users may consider programming the device in the factory before shipping to end users. ADI offers a device programming software, which can be implemented in the factory on PCs that run Windows 95 to XP platforms. As a result, external controllers are not required, which significantly reduces development time. The program is an executable file that does not require any programming languages or user programming skills. It is easy to set up and use. ***Figure 36*** shows the software interface. The software can be downloaded from www.analog.com.

Write

The AD5172/73 start at midscale after power-up prior to the OPT programming. To increment or decrement the resistance, the user may simply move the scrollbar on the left. To write any specific values, the user should use the bit pattern control in the upper screen and press the Run button. The format of writing data to the device is shown in **Error! Reference source not found.**. Once the desirable setting is found, the user may press the Program Permanent button to blow the internal fuse links for permanent setting. The user may also set the programming bit pattern in the upper screen and press the Run button to achieve the same result.

Read

To read the validation bits and data out from the device, the user may simply press the Read button. The user may also set the bit pattern in the upper screen and press the Run button. The format of reading data out from the device is shown in **Error! Reference source not found.**.

To apply the device programming software in the factory, users need to modify a parallel port cable and configure Pins 2, 3, 15, and 25 for SDA_write, SCL, SDA_read, and DGND, respectively for the control signals (Figure 37). Users should also layout the PCB of the AD5172/73 with SCL and SDA pads, as shown in Figure 38, such that pogo pins can be inserted for the factory programming.

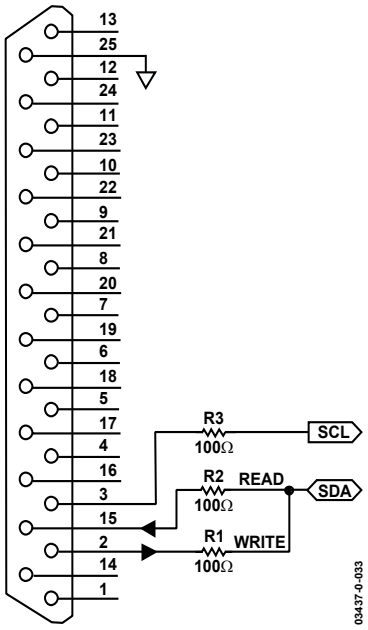

Figure 37. Parallel Port Connection. Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND.

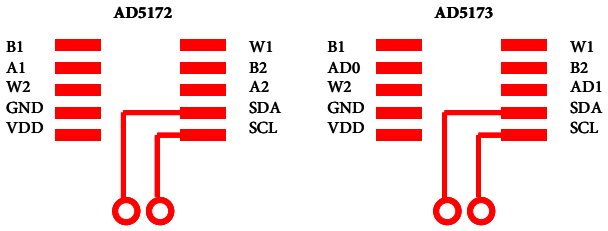

Figure 38. Recommended AD5172/73 PCB Layout. The SCL and SDA pads allow pogo pins to be inserted so that signals can be communicated through the parallel port for programming (Figure 37).

I²C INTERFACE

Table 10. Write Mode

AD5172

S	0	1	0	1	1	1	1	$\overline{W}$	A	A0	SD	T	0	OW	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

AD5173

S	0	1	0	1	1	AD1	AD0	$\overline{W}$	A	A0	SD	T	0	OW	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Table 11. Read Mode

AD5172

S	0	1	0	1	1	1	1	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

AD5173

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

S = Start Condition

P = Stop Condition

A = Acknowledge

X = Don't Care

$\overline{W}$ = Write

R = Read

A0 = RDAC sub address select bit

SD = Shutdown connects wiper to B terminal and open circuits A terminal. It does not change contents of wiper register.

T = OTP Programming Bit. Logic 1 programs wiper permanently.

OW = Overwrite fuse setting and program digital pot to different setting. Note that upon power up, digital pot will preset to either midscale or fuse setting depending on whether or not the fuse link has been blown.

D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits

E1, E0 = OTP Validation Bits

0 , 0 = Ready to program

0 , 1 = Test fuse not blown successfully(check setup)

1 , 0 = Fatal error. Retry.

1 , 1 =Programmed Successfully. No further adjustments possible.

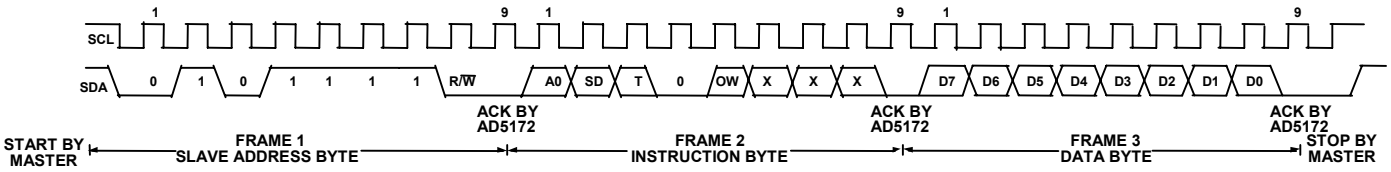

Figure 39. Writing to the RDAC Register – AD5172

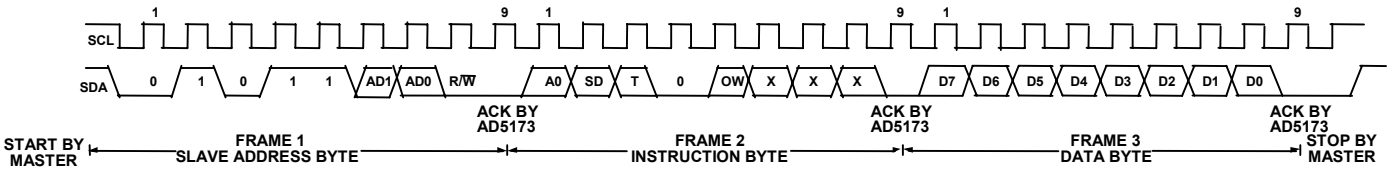

Figure 40. Writing to the RDAC Register – AD5173

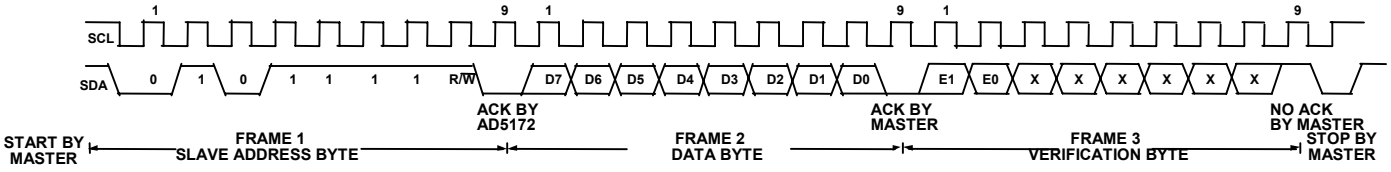

Figure 41. Reading Data from a Previously Selected RDAC Register in Write Mode – AD5172

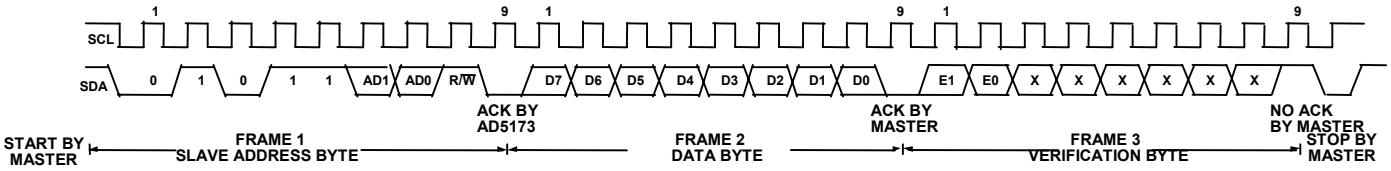

Figure 42 Reading Data from a Previously Selected RDAC Register in Write Mode – AD5173

I²C COMPATIBLE 2-WIRE SERIAL BUS

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 399 and 40). The following byte is the slave address byte, which consists of the slave address followed by an R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device). The AD5172 has a fixed slave address byte whereas the AD5173 has two configurable address bits AD0 and AD1 (see Table 10).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. On the other hand, if the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. In the write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is the RDAC sub address select bit. A logic low will select channel-1 and a logic high will select channel-2.

   The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at terminal A while shorting the wiper to terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting will be applied to the RDAC. Also, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting will be applied to the RDAC.

   The third MSB, T, is the OTP(One Time Programmable) programming bit. A logic high blows the poly fuses and programs the resistor setting permanently.

   The fourth MSB must always be at a logic zero.

   The fifth MSB, OW, is an overwrite bit. When raised to a logic high, this bit allows the RDAC setting to be changed

even after the internal fuses have been blown. However, once the OW bit is returned to a logic zero, the position of the RDAC will return to the setting prior to overwrite. Because OW is not static, if the device is powered off and on, the RDAC will preset to midscale or to the setting at which the fuses were blown depending on whether or not the fuses have been permanently set already.

The remainder of the bits in the instruction byte are don't cares(see Table 10).

After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figures 39 and 40).

3. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses(a slight difference with the write mode, where there are eight data bits followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 41 and Figure 42).

   Note that the channel of interest is the one that is previously selected in the Write Mode. In the case where users need to read the RDAC values of both channels, they need to program the first channel in the Write Mode and then change to the Read Mode to read the first channel value. After that, they need to change back to the Write Mode with the second channel selected and read the second channel value in the Read Mode again. It is not necessary for users to issue the Frame 3 data byte in the write mode for subsequent readback operation. Users should refer to Figure 41 for the programming format.

   Following the data byte, the validation byte contains two validation bits, E0 and E1. These bits signify the status of the One Time Programming (see Table).

4. After all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master will pull the SDA line high during the tenth clock pulse to establish a STOP condition (see Figure 39) In read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse which goes high to establish a STOP condition (see Figure 41).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output will update on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

Table 12. Validation Status

E1	E0	Status
0	0	Ready for Programming
0	1	Test Fuse Not Blown Successfully (Check Setup)
1	0	Fatal Error. Some Fuses are not Blown. Retry Again
1	1	Successful. No Further Programming is Possible

Multiple Devices on One Bus(AD5173 only)

Figure 44 shows four AD5173 devices on the same serial bus. Each has a different slave address since the states of their AD0 and AD1 pins are different. This allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C compatible interface.

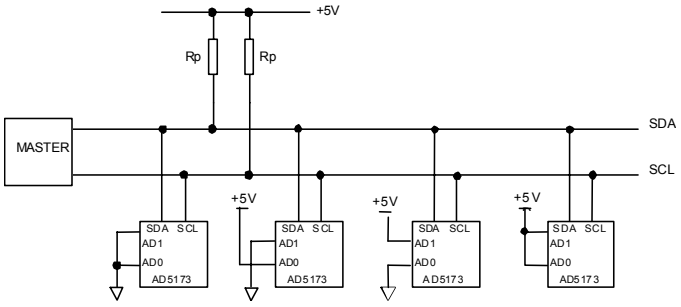

Figure 44. Multiple AD5173 Devices on One I²C Bus

TEST CIRCUITS

Figure 4 5 to Figure 53 illustrate the test circuits that define the test conditions used in the product specification tables.

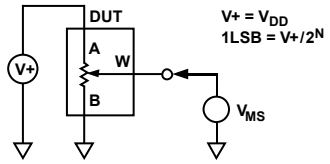

Figure 4 5. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

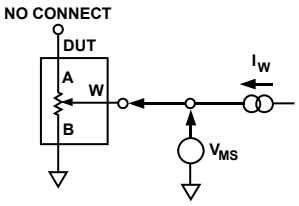

Figure 46. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

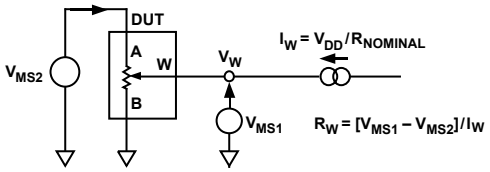

Figure 47. Test Circuit for Wiper Resistance

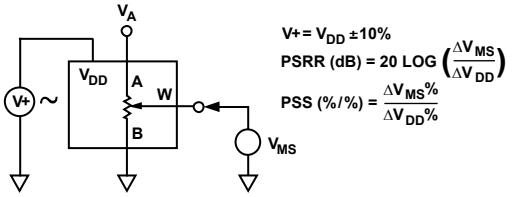

Figure 48. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

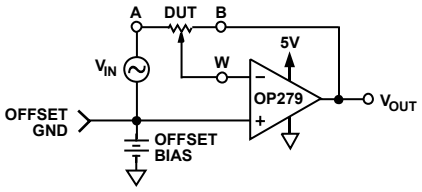

Figure 49. Test Circuit for Inverting Gain

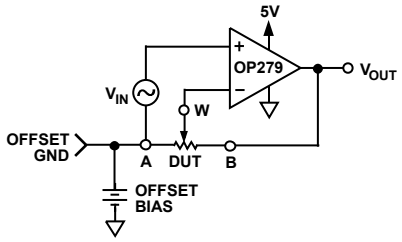

Figure 50. Test Circuit for Noninverting Gain

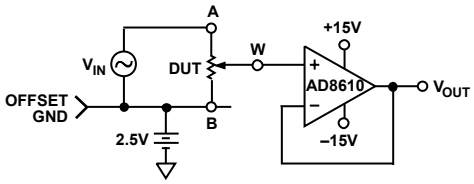

Figure 51. Test Circuit for Gain vs. Frequency

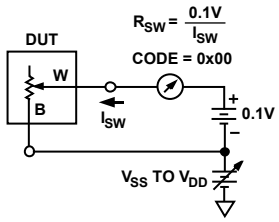

Figure 52. Test Circuit for Incremental ON Resistance

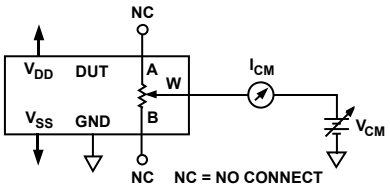

Figure 53. Test Circuit for Common-Mode Leakage current

OUTLINE DIMENSIONS

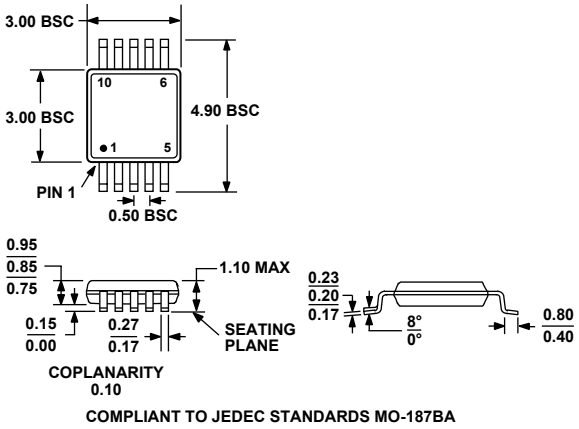

Figure 54. 10-Lead Mini Small Outline Package [MSOP] (RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5172BRM2.5-R2	2.5k	–40°C to +125°C	MSOP-10	RM-10	D0U
AD5172BRM2.5-RL7	2.5k	–40°C to +125°C	MSOP-10	RM-10	D0U
AD5172BRM10-R2	10k	–40°C to +125°C	MSOP-10	RM-10	D0V
AD5172BRM10-RL7	10k	–40°C to +125°C	MSOP-10	RM-10	D0V
AD5172BRM50-R2	50k	–40°C to +125°C	MSOP-10	RM-10	D10
AD5172BRM50-RL7	50k	–40°C to +125°C	MSOP-10	RM-10	D10
AD5172BRM100-R2	100k	–40°C to +125°C	MSOP-10	RM-10	D11
AD5172BRM100-RL7	100k	–40°C to +125°C	MSOP-10	RM-10	D11
AD5172EVAL	See Note 1		Evaluation Board		

Model	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5173BRM2.5-R2	2.5k	–40°C to +125°C	MSOP-10	RM-10	D1K
AD5173BRM2.5-RL7	2.5k	–40°C to +125°C	MSOP-10	RM-10	D1K
AD5173BRM10-R2	10k	–40°C to +125°C	MSOP-10	RM-10	D1L
AD5173BRM10-RL7	10k	–40°C to +125°C	MSOP-10	RM-10	D1L
AD5173BRM50-R2	50k	–40°C to +125°C	MSOP-10	RM-10	D1M
AD5173BRM50-RL7	50k	–40°C to +125°C	MSOP-10	RM-10	D1M
AD5173BRM100-R2	100k	–40°C to +125°C	MSOP-10	RM-10	D1N
AD5173BRM100-RL7	100k	–40°C to +125°C	MSOP-10	RM-10	D1N
AD5173EVAL	See Note 1		Evaluation Board		

[1]The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

NOTES