Energy Metering IC with pulse output

Preliminary Technical Data — AD7755*

FEATURES

High Accuracy, supports 50/60 Hz IEC 521/1036
Less than 0.3% error over a dynamic range of 500 to 1
The AD7755 supplies *average real power* on the frequency outputs F1 and F2
The high frequency output CF is intended for calibration and supplies *instantaneous real power*
The Logic output REVP can be used to indicate a potential mis-wiring or negative power
Direct drive for electromechanical counters and two phase stepper motors (F1 and F2)
A PGA in the current channel allows the use of small values of *shunt* and *burden* resistance
Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time
User selectable timed reset of AD7755 on power up/down
On-Chip reference 2.5V±8% (55 ppm/°C typical) with external overdrive capability
Single 5V Supply, Low power (15mW typical)
Low Cost CMOS Process

GENERAL DESCRIPTION

The AD7755 is a high accuracy electrical energy measurement IC which is intended for use with two-wire distribution systems. The part specifications surpass the accuracy requirements as quoted in the IEC1036 standard.

The only analog circuitry used in the AD7755 is in the ADCs and reference circuit. All other signal processing (e.g., multiplication and filtering) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

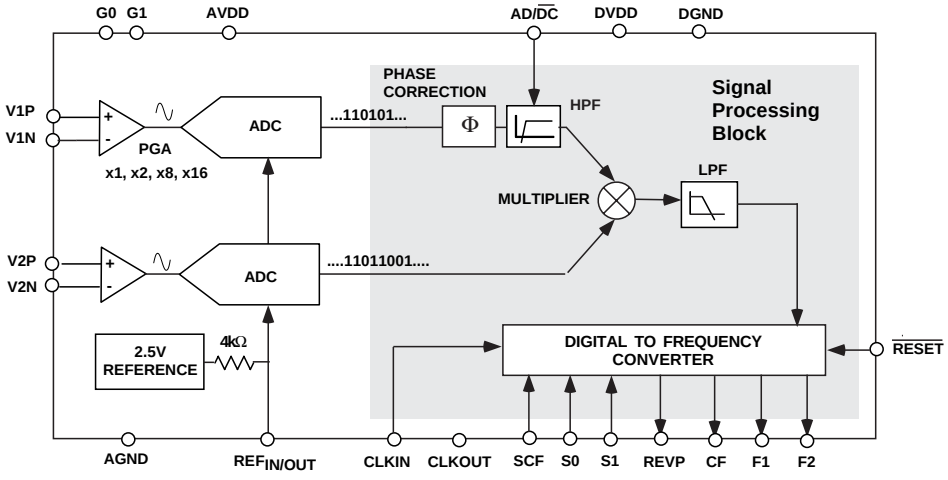
The AD7755 supplies Average Real Power information on the low frequency outputs F1 and F2. These logic outputs may be used to directly drive an electromechanical counter or interface to an MCU. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes.

An automatic timed (controlled by an external RC) reset pin on the AD7755 ensures correct operation on initial power up and at power down. The reset functions by holding the AD7755 in a reset state until the power supply has settled.

Internal phase matching circuitry ensures that the voltage and current channels are matched whether the HPF in channel 1 is on or off.

The AD7755 is fabricated on 0.6μm CMOS technology; a process that combines low power and low cost. The AD7755 is available in 24 Lead DIP and SSOP packages.

FUNCTIONAL BLOCK DIAGRAM



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*Patents Pending.

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AD7755–SPECIFICATIONS[1,4]

(AV_{DD} = DV_{DD} = 5V ± 5%, AGND = DGND = 0V, On-Chip Reference, CLKIN = 3.58MHz, TMIN to TMAX = -40°C to +85°C)

Parameter	B Version -40°C to +85°C	Units	Test Conditions/Comments
ACCURACY			
Measurement Error[1] on Channel 1 and 2			One Channel with Full Scale Signal (±500mV).
Gain = 1	0.2	%Reading typ	Over a dynamic range 500 to 1
Gain = 2	0.2	%Reading typ	Over a dynamic range 500 to 1
Gain = 8	0.3	%Reading typ	Over a dynamic range 500 to 1
Gain = 16	0.3	%Reading typ	Over a dynamic range 500 to 1
Phase Error[1] Between Channels			Line Frequency = 45Hz to 65Hz
V1 Phase Lead 37° (PF = 0.8 Capacitive)	±0.05	Degrees(°) max	AC/$\overline{DC}$ = 0 and AC/$\overline{DC}$ = 1
V1 Phase Lag 60° (PF = 0.5 Inductive)	±0.05	Degrees(°) max	AC/$\overline{DC}$ = 0 and AC/$\overline{DC}$ = 1
ac Power Supply Rejection[1]			AC/$\overline{DC}$ = 1 , S0=S1=1, G0=G1=0
Output Frequency Variation (CF)	0.01	%Reading typ	V1A=V1B=±100mV rms, V2P = ±100mV rms, Ripple on AV_{DD} of 250mV rms / 50Hz
dc Power Supply Rejection[1]			AC/$\overline{DC}$ = 1 , S0=S1=1, G0=G1=0
Output Frequency Variation (CF)	0.01	%Reading typ	V1A=V1B=±100mV, V2P = ±100mV rms, AV_{DD} = AV_{DD} ±250mV
ANALOG INPUTS			*See Analog Inputs Section*
Maximum Signal Levels	±1	V max	V1P, V1N, V2N and V2P to AGND
Input Impedance (dc)	400	kΩ min	CLKIN = 3.58 MHz
Bandwidth	3.5	kHz typ	CLKIN/1024, CLKIN = 3.58 MHz
ADC Offset Error[1]	±10	mV max	See Terminology
Gain Error[1]	±4	% Ideal typ	External 2.5V reference, Gain=1, V1=V2=500mV dc
Gain Error Match[1]	±0.3	% Ideal typ	External 2.5V reference
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.7	V max	2.5 V +8%
	2.3	V min	2.5V -8%
Input Impedance	4	kΩ min	
Input Capacitance	10	10	pF max
ON-CHIP REFERENCE			Nominal 2.5V
Reference Error	±200	mV max	
Temperature Coefficient	55	ppm/°C typ	
CLKIN			Note all specifications for CLKIN of 3.58MHz
Input Clock Frequency	4	MHz max	
	1	MHz min	
LOGIC INPUTS			
SCF, S0, S1, AC/$\overline{DC}$, $\overline{RESET}$, G0 and G1			
Input High Voltage, V_{INH}	2.4	V min	DV_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	DV_{DD} = 5 V ± 5%
Input Current, I_{IN}	±3	μA max	Typically 10nA, V_{IN} = 0V to DV_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS[3]			
F1and F2			
Output High Voltage, V_{OH}			I_{SOURCE} =10mA
	4.5	V min	DV_{DD} = 5V ±5%
Output Low Voltage, V_{OL}			I_{SINK} = 10mA
	0.5	V max	DV_{DD} = 5V ± 5%
CF and REVP			
Output High Voltage, V_{OH}			I_{SOURCE} =10mA
	4	V min	DV_{DD} = 5V ±5%
Output Low Voltage, V_{OL}			I_{SINK} =10mA
	1	V max	DV_{DD} = 5V ± 5%

Parameter	B Version -40°C to +85°C	Units	Test Conditions/Comments
POWER SUPPLY			For specified Performance
AV_{DD}	4.75	V min	5V - 5%
	5.25	V max	5V +5%
DV_{DD}	4.75	V min	5V - 5%
	5.25	V max	5V +5%
AI_{DD}	3	mA max	Typically 1.5 mA
DI_{DD}	2	mA max	Typically 1.5 mA

NOTES:
[1]See Terminology Section for explaination of Specifications
[2]Fault Detection Section of data sheet for explanation of fault detection functionality
[3] See Plots in Typical Performance Graphs
[4] Specifications subject to change without notice

AD7755 TIMING CHARACTERISTICS[1,2]

(AV_{DD} = DV_{DD} = 5V ± 5%, AGND = DGND = 0V, On-Chip Reference, CLKIN = 3.58MHz, TMIN to TMAX = -40°C to +85°C)

Parameter	B Versions	Units	Test Conditions/Comments
t_1[3]	275	ms	F1 and F2 pulse width (logic low)
t_2	See Table 1	s	Output pulse period. See Table 1 to determine the output frequency
t_3	$\frac{1}{2}t_2$	s	Time between F1 falling edge and F2 falling edge
t_4[3]	90	ms	CF pulse width (logic high)
t_5	See Table 1	s	CF pulse period, See Table 1 to determine the output frequency
t_6	CLKIN/4	s	Minimum time Between F1 and F2 Pulse

NOTES
[1] Sample tested during initial release and after any redesign or process change that may affect this parameter.
[2] See Figure 7.
[3] The Pulse widths of F1, F2 and CF are not fixed for higher output frequencies. See Frequency Outputs

ORDERING GIUDE

Model	Package Option*
AD7755BN	N-24
AD7755BRS	RS-24

* N = Plastic DIP; RS = Shrink Small Outline Package

Terminology

MEASUREMENT ERROR
The error associated with the power measurement made by the AD7755 is defined by the following formula:

$$\text{Error} = \frac{\text{Measured Power - Ideal Power}}{\text{Ideal Power}} \times 100\%$$

PHASE ERROR BETWEEN CHANNELS
The HPF (High Pass Filter) in the channel 1 has a phase lead response. To offset this phase response and equalize the phase response between channels a phase correction network is also placed in channel 1. The phase correction network matches the phase to within ±0.05° over a range of 45Hz to 65Hz.

POWER SUPPLY REJECTION
AD7755 measurement error as a percentage of reading when the power supplies are varied.
For the ac PSR measurement a reading at nominal supplies (5V) is taken. Then a 200mV rms/50Hz signal is introduced onto the supplies and a second reading obtain under with the same input signal levels. Any error introduced is expressed as a percentage of reading—see MEASUREMENT ERROR definition.
For the dc PSR measurement a reading at nominal supplies (5V) is taken. Then the supplies are varied ±5% and a second reading obtain under with the same input signal levels. Any error introduced is again expressed as a percentage of reading.

ADC OFFSET ERROR
This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND the ADCs still see an analog input signal of ±10mV. However when the HPF is switched on the offset is removed from the current channel and the power calculation is not affected by this offset.

GAIN ERROR
The gain error of the AD7755 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. It is measured with a gain of 1 in channel V1. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the AD7755 transfer function—see AD7755 Transfer Function

GAIN ERROR MATCH
The Gain Error Match is defined as the gain error (minus the offset) obtained when switching between a gain of 1 and a gain of 2, 8, or 16. It is expressed as a percentage of the output frequency obtained under a gain of 1.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} toAV_{DD} ..... –0.3 V to +0.3 V
Analog Input Voltage to AGND
V_{1A}, V_{1B}, V_{1N}, V_{2P} and V_{2N} ..... -6V to +6V
Reference Input Voltage to AGND .. –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND .... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND .. –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
24Pin Plastic DIP, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 105°C/W
Lead Temperature, (Soldering 10 sec) ..... +260°C
24Pin SSOP, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 112°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

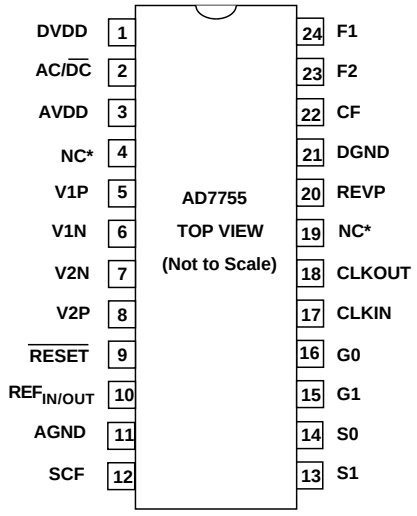
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7755 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	MNEMONIC	DESCRIPTION
1	DV_{DD}	Digital power supply. This pin provides the supply voltage for the digital circuitry in the AD7755. The supply voltage should be maintained at 5V ± 5% for specified operation. This pin should be decoupled to DGND with a 10μF capacitor in parallel with a ceramic 100nF capacitor.
2	AC/$\overline{DC}$	High pass filter select. This logic input is used to enable the HPF in Channel 1 (the current channel). A logic one on this pin enables the HPF. The associated phase response of this filter has been internally compensated over a frequency range of 45Hz to 65Hz. The HPF filter should be enabled in power metering applications.
3	AV_{DD}	Analog power supply. This pin provides the supply voltage for the analog circuitry in the AD7755. The supply should be maintained at 5V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. The typical performance graphs in this data sheet show power supply rejection performance. This pin should be decoupled to AGND with a 10μF capacitor in parallel with a ceramic 100nF capacitor.
5,6	V1P, V1N	Analog inputs for Channel 1. These inputs are fully differential voltage inputs with a maximum signal level of ±500mV with respect to pin V1N for specified operation. Channel 1 also has a PGA and the gain selections are outlined in table I.The maximum signal level at this pin is ±1V with respect to AGND. Both inputs have internal ESD protection circuitry and in addition an overvoltage of ±6V can be sustained on these inputs without risk of permanent damage.
7,8	V2N, V2P	Negative and positive inputs for Channel 2 (voltage channel). These inputs provide a fully differential input pair. The maximum differential input voltage is ±500mV for specified operation. The maximum signal level at these pins is ±1V with respect to AGND. Both inputs have internal ESD protection circuitry and an overvoltage of ±6V can also be sustained on these inputs without risk of permanent damage.
9	$\overline{RESET}$	Reset pin for the AD7755. A logic low on this pin will hold the ADCs and digital circuitry in a reset condition. This pin may be used to hold the AD7755 in reset until the power supplies have settled after power up—see Using the Reset Pin.
10	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5V ± 8% and a typical temperature coefficient of 55ppm/°C. An external reference source may also be connected at this pin. In either case this pin should be decoupled to AGND with a 1μF ceramic capacitor.
11	AGND	This provides the ground reference for the analog circuitry in the AD7755, i.e. ADCs and reference. This pin should be tied to the analog ground plane of the PCB. The analog ground plane is the ground reference for all analog circuitry, e.g. anti aliasing filters, current and voltage transducers, etc. For good noise suppression the analog ground plane should only connected to the digital ground plane at the DGND pin.
12	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table IV shows how the calibration frequencies are selected.
13,14	S1, S0	These logic inputs are used to select one of four possible frequencies for the digital to frequency conversion. This offers the designer greater flexibility when designing the energy meter. See AD7755 Transfer Function.

Pin No.	MNEMONIC	DESCRIPTION
15,16	G1, G0	These logic inputs are used to select one of four possible gains for the analog inputs V1A and V1B. The possible gains are 1, 2, 8 and 16. See Analog Input section.
17	CLKIN	An external clock can be provided at this logic input. Alternatively a crystal can be connected across CLKIN and CLKOUT to provide a clock source for the AD7755. The clock frequency for specified operation is 3.58MHz. Crystal load capacitors of 33pF ceramic should be used the with gate oscillator circuit.
18	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the AD7755. The CLKOUT pin can drive one CMOS load when an external clock is supplied at CLKIN.
20	REVP	This logic output will go logic high when negative power is detected, i.e. when the voltage and current signals at 180° out of phase. This output is not latched and will be reset when positive power is once again detected. The output will go high or low at the same time as a pulse output on F1 and F2.
21	DGND	This provides the ground reference for the digital circuitry in the AD7755, i.e. multiplier, filters and digital to frequency converter. This pin should be tied to the digital ground plane of the PCB. The digital ground plane is the ground reference for all digital circuitry, e.g. counters (mechanical and digital), MCUs and indicator LEDs. For good noise suppression the analog ground plane should only connected to the digital ground plane at the DGND pin.
22	CF	Calibration Frequency logic output. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes. Also see SCF pin description.
23, 24	F2, F1	Low frequency logic outputs. F1 and F2 supply *average real power* information. The logic outputs can be used to directly drive electromechanical counters and two phase stepper motors. See AD7755 Transfer Function.

PIN CONFIGURATION
DIP & SSOP PACKAGES



*NC = No Connection

ANALOG INPUTS

Channel V1 ***(Current Channel)***

The voltage output from the current transducer is connected to the AD7755 here. Channel V1 is a fully differential voltage input. V1P is the positive input with respect to V1N.
The maximum peak differential signal on Channel 1 should be less than ±500mV for specified operation. Note Channel 1 has a programmable gain amplifier (PGA) with user selectable gain of 1, 2, 8 or 16—see Table I. These gains facilitate easy transducer interfacing.

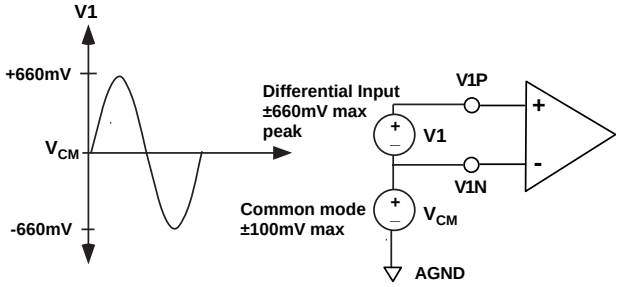


Figure 1. Maximum signal levels, Channel 1, Gain = 1

The diagram in figure 1 illustrates the maximum signal levels on V1P and V1N. The maximium differential voltage is ±500mV divided by the gain selection. The differential voltage signal on the inputs must be referenced to a common mode, e.g. AGND.

TABLE I

G1	G0	Gain	Maximum differential Signal
0	0	1	±500mV
0	1	2	±250mV
1	0	8	±62mV
1	1	16	±31mV

Channel V2 ***(Voltage Channel)***

The output of the line voltage transducer is connected to the AD7755 at this analog input. Channel V2 is a fully differential voltage input. The maximum peak differential signal on Channel 2 is ±500mV. Figure 2 illustrates the maximum signal levels which can be connected to the AD7755 Channel 2.

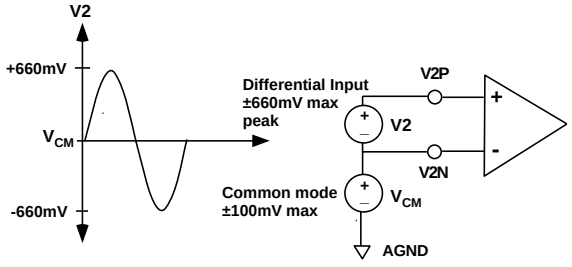


Figure 2. Maximum signal levels, Channel 2

Channel 2 must be driven from a common mode voltage, i.e. the differential voltage signal on the input must be referenced to a common mode(usually AGND). The analog inputs of the AD7755 can be driven with common mode voltages of up to 100mV with respect to AGND. However best results are achieved using a common mode equal to AGND.

Typical Connection Diagrams

Figure 3 below shows a typical connection diagram for Channel V1. A CT (current transformer) is the current transducer selected for this example. Notice the common mode volatge for channel 1 is AGND and is derived by center tapping the burden resistor to AGND. This provides the complemetary analog input signals for V1P and V1N. The CT turns ratio and burden resistor Rb are selected so as to give a peak differential voltage of ±500mV/Gain at maximum load.

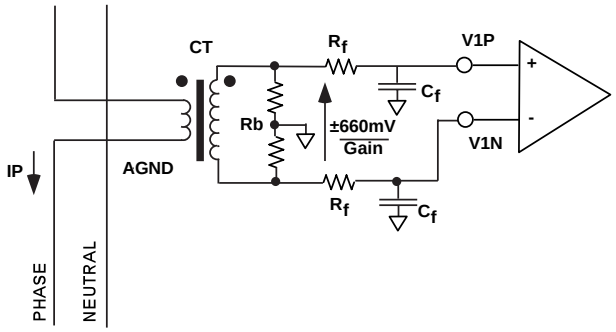


Figure 3. Typical connection for Channel 1

Figure 4. shows two typical connections for Channel V2. The first option uses a PT (potential transformer) to provide complete isolation from the mains voltage. In the second option the AD7755 is biased around the neutral wire and a resistor divider is used to provide a voltage signal which is proportional to the line voltage. Adjusting the ratio of Ra and Rb is also a convenient way of carrying out a gain calibration on the meter.

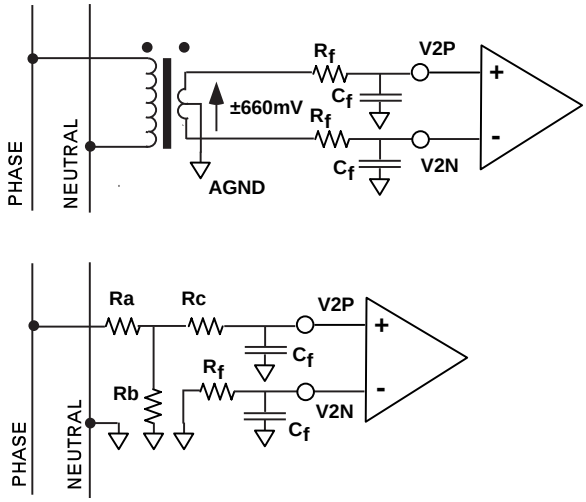


Figure 4. Typical connections for Channel 2

THEORY OF OPERATION

The two ADCs digitize the voltage signals from the current and voltage transducers. These ADCs are 16 bit second order sigma delta with an over sampling rate of 900kHz. This analog input structure greatly simplifies transducer interfacing by providing a wide dynamic range for direct connection to the transducer and also simplifying the antialiasing filter design. A programmable gain stage in the current channel further facilitates easy transducer interfacing. A high pass filter in the current channel removes any dc component from the current signal. This eliminates any inaccuracies in the real power calculation due to offsets in the voltage or current signals.

The real power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. In order to extract the real power component (i.e., the dc component) the instantaneous power signal is low pass filtered. Figure 5 illustrates the instantaneous real power signal and shows how the real power information can be extracted by low pass filtering the instantaneous power signal. This scheme calculates real power correctly for non sinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

The low frequency output of the AD7755 is generated by accumulating this real power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average real power. This average real power information can in turn be accumulated (e.g., by a counter) to generate real energy information. Because of its high output frequency and hence shorter integration time, the CF output is proportional to the instantaneous real power. This is useful for system calibration purposes which would take place under steady load conditions.

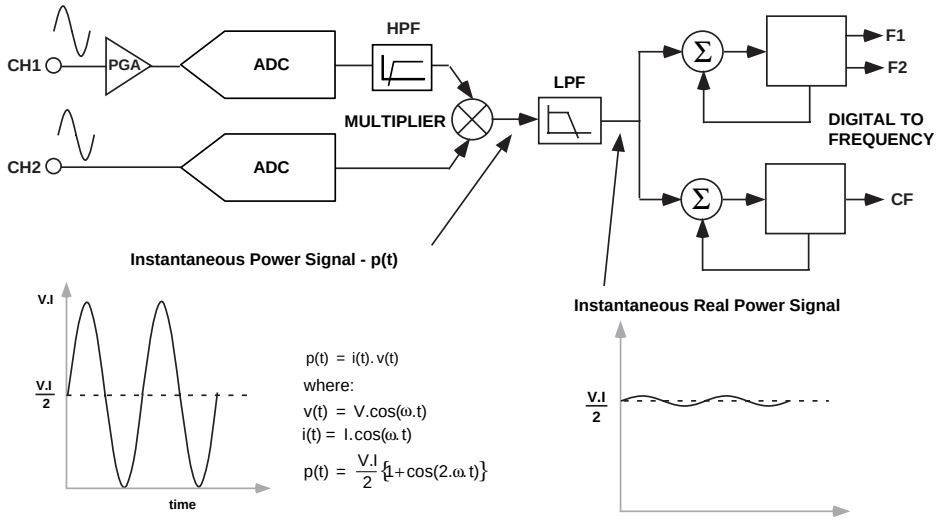


Figure 5. AD7755 Signal Processing Block Diagram

Offset Effects

Figure 6 shows the effect of offsets on the real power calculation. As can be seen from figure 2 an offset on Channel 1 and Channel 2 will contribute a dc component after multiplication. Since this dc component is extracted by the LPF to generate the real power information, the offsets will have contributed an error to the real power calculation. This problem is easily avoided by enabling the HPF (i.e., pin AC/$\overline{DC}$ is set logic high) in Channel 1. By removing the offset from at least 1 channel no error component can be generated at dc by the multiplication. Error terms at Cos(ω.t) are removed by the LPF.

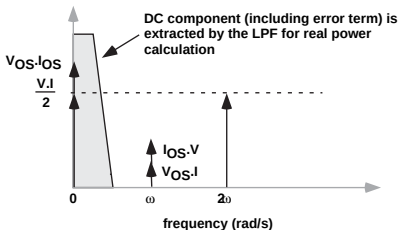


Figure 6. Effect of channel offsets on the real power calculation

Power Factor Considerations

The method used to extract the real power information from the instantaneous power signal (i.e., by low pass filtering) is still valid even when the voltage and current signals are not in phase. Figure 7 below displays the unity power factor condition and a dPF (Displacement Power Factor) = 0.5, i.e., current signal lagging the voltage by 60° . If we assume the voltage and current waveforms are sinusoidal then the real power component of the instantaneous power signal (i.e., the dc term) is given by (V.I/2).Cos(60°).

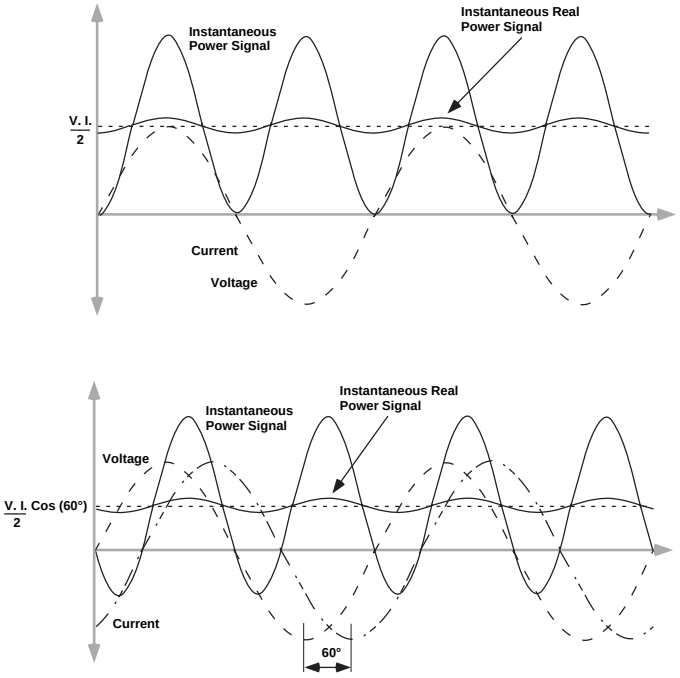


Figure 7. dc component of Instantaneous Power Signal conveys Real Power Information PF < 1

NONSINUSOIDAL VOLTAGE AND CURRENT

The real power calculation method also holds true for non sinusoidal current and voltage waveforms. All voltage and current waveforms in a practical applications will have some harmonic content. Using the Fourier Transform, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content.

$$v(t) = V_0 + \sqrt{2}.\sum_{h\neq 0}^{\infty} V_h.\sin(h\omega t + \alpha_h) \qquad (1)$$

Where: v(t) is the instantaneous voltage, V_o is the average value, V_h is the rms value of voltage harmonic h and α_h is the phase angle of the voltage harmonic.

$$i(t) = I_0 + \sqrt{2}.\sum_{h\neq 0}^{\infty} I_h.\sin(h\omega t + \beta_h) \qquad (2)$$

Where:i(t) is the instantaneous current, I_o is the dc component, I_h is the rms value of current harmonic h and β_h is the phase angle of the current harmonic.

Using equations 1 and 2 the real power P can be expressed in terms of its fundamental real power (P_1) and harmonic real power (P_H).

$$P = P_1 + P_H$$

where:

$$P_1 = V_1.I_1\cos\phi_1$$
$$\phi_1 = \alpha_1 - \beta_1 \qquad (3)$$

and

$$P_H = \sum_{h\neq 1} V_h.I_h\cos\phi_h$$
$$\phi_h = \alpha_h - \beta_h \qquad (4)$$

As can be seen from equation 4 above, a harmonic real power component is generated for every harmonic provided that harmonic is present in both the voltage and current waveforms. The Power Factor calculation has previously been shown to be accurate in the case of a pure sinusoid, therefore the harmonic real power must also correctly account for Power Factor since it is made up of a series of pure sinusoids.
Note the input Bandwidth of the analog inputs is 3.5kHz with a master clock frequency of 3.5795MHz.

Digital to Frequency Conversion.

As previously described the digital output of the Low Pass Filter after multiplication contains the real power information. However since this LPF is not an ideal "brick wall" filter implementation, the output signal also contains attenuated components at the line frequency and its harmonics ,i.e., Cos(h.ω.t) where h = 1,2,3,...etc. The dominating harmonic will be at twice the line frequency, i.e., Cos(2ω.t) and this is due the instantaneous power signal. Figure 8 shows the instantaneous real power signal which still contains a significant amount of instantaneous power information, i.e., Cos(2ω.t). This signal is then passed to the digital to frequency converter where it is integrated (accumulated) over time in order to produce an output frequency. This accumulation of the signal will suppress or average out any non dc components in the instantaneous real power signal. The average value of a sinusoidal signal is zero. Hence the frequency generated by the AD7755 is proportional to the average real power. Figure 8 below shows the digital to frequency conversion for steady load conditions, i.e., constant voltage and current.

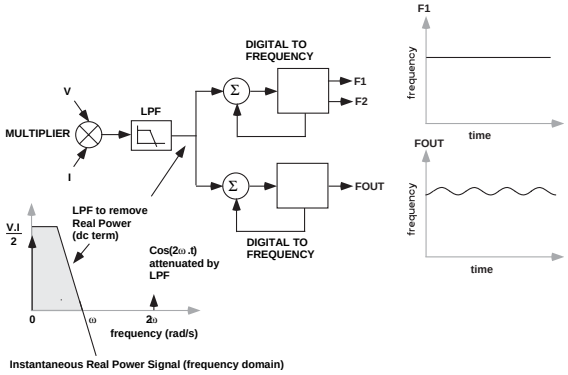


Figure 8. Real Power to Frequency Conversion

As can be seen in the diagram, the frequency output CF is seen to vary over time, even under steady load conditions. This frequency variation is primarily due to the Cos(2ω.t) component in the instantaneous real power signal. The output frequency on CF can be up to 2048 times higher than the frequency on F1 and F2. This higher output frequency is generated by accumulating the instantaneous real power signal over a much shorter time while converting it to a frequency. This shorter accumulation period means less averaging of the Cos(2ω.t) component. As a consequence some of this instantaneous power signal passes through the Digital to Frequency conversion. This will not be a problem in the application—see Meter Calibration. Because the outputs F1 and F2 operate at a much lower frequency, a lot more averaging of the instantaneous real power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple free frequency output.

Frequency Outputs

Figure 9 below shows the waveforms of the various frequency outputs. The outputs F1 and F2 are the low frequency outputs which can be used to directly drive a stepper motor or electromechanical impulse counter. The F1 and F2 outputs provide two alternating low going pulses. The pulse width *(t_1)* is set at 275ms and the time between the falling edges of F1 and F2 *(t_3)* is approximately half the period of F1 *(t_2)* . If however the period of F1 and F2 falls below 550ms (1.81Hz) the pulse width of F1 and F2 is set to half of their period.

The High frequency CF output is intended to be used for communications and calibration purposes. CF produces a 90ms wide active high pulse *(t_4)* at a frequency which is proportional to the product of Channel 1 and Channel 2 . The output frequencies are given in Table III. As in the case of F1 and F2, if the period of CF *(t_5)* falls below 180ms then the CF pulse width is set to half the period. For example if the CF frequency is 20Hz then the CF pulse width is 25ms.

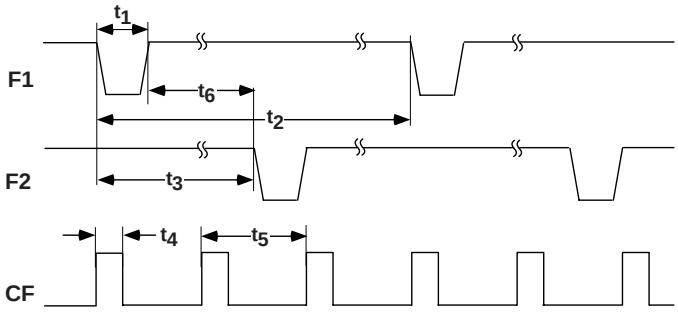


Figure 9. Timing Diagram for Frequency outputs

AD7751 TRANSFER FUNCTION

Frequency Outputs F1 and F2

The AD7751 calculates the product of two voltage signals (on Channel 1 and Channel 2) and then low pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low, e.g. 0.17Hz maximun for ac signals with S0 = S1 = 0 —see Table III. This means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency which is proportional to the averge real power. The averaging of the real power signal is implicit to the digital to frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation.

$$\text{Freq} = \frac{2.5 \times V1 \times V2 \times \text{Gain} \times F_{1-4}}{V_{REF}^2}$$

where,

Freq = Output frequency on F1 and F2 *(Hz)*

V1 = Differential RMS voltage signal on Channel 1 *(volts)*

V2 = Differential RMS voltage signal on Channel 2 *(volts)*

Gain = 1, 2, 8 or 16 depending on the PGA gain selection made using logic inputs G0 and G1

V_{REF} = The reference voltage (2.5V ± 8%) *(volts)*

F_{1-4} = One of four possible frequencies selected by using the logic inputs S0 and S1—see Table II

TABLE II

S1	S0	F_{1-4} (Hz)	XTAL/CLKIN*
0	0	0.85	3.579MHz / 2^{22}
0	1	1.7	3.579MHz / 2^{21}
1	0	3.41	3.579MHz / 2^{20}
1	1	6.83	3.579MHz / 2^{19}

*NOTE F1-4 are a binary fraction of the master clock and therefore will vary if the specified CLKIN frequency is altered.

Example 1

Thus if full scale differential dc voltages of +500mV and -500mV are applied to V1 and V2 respectively (500mV is the maximum differential voltage which can be connected to channel 1 and channel 2) the expected output frequency is calculated as follows.

Gain = 1, *G0 = G1 = 0*

F_{1-4} = 0.85Hz, *S0 = S1 = 0*

V1 = +500mV dc = 0.66 volts (RMS of dc = dc)

V2 = -500mV dc = 0.66 volts (RMS of dc = |dc|)

V_{REF} = 2.5V (nominal reference value).
NOTE: If the on chip reference is used actual output frequencies may vary from device to device due to reference tolerence of ±8%.

$$\text{Freq} = \frac{2.5 \times 0.5 \times 0.5 \times 1 \times 0.85}{2.5^2} = 0.34$$

Example 2

In this example ac voltages of ±500mV peak applied to V1 and V2 then the expected output frequency is calculated as follows.

Gain = 1, *G0 = G1 = 0*

F_{1-4} = 0.85Hz, *S0 = S1 = 0*

V1 = RMS of 660mV peak ac = $0.66 / \sqrt{2}$ volts

V2 = RMS of 660mV peak ac = $0.66 / \sqrt{2}$ volts

V_{REF} = 2.5V (nominal reference value).
NOTE: If the on chip reference is used actual output frequencies may vary from device to device due to reference tolerence of ±8%.

$$\text{Freq} = \frac{2.5 \times 0.5 \times 0.5 \times 1 \times 0.85}{\sqrt{2} \times \sqrt{2} \times 2.5^2} = 0.17$$

As can be seen from these two example calculations the maximum output frequency for ac inputs is alway half of that for dc input signals. Table II shows a complete listing of all maximum output frequencies.

TABLE III

S1	S0	Max Frequency for dc inputs (Hz)	Max Frequency for ac inputs (Hz)
0	0	0.34	0.17
0	1	0.68	0.34
1	0	1.36	0.68
1	1	2.72	1.36

Frequency Output CF

The pulse output CF (Calibration Frequency) is intended for use during calibration. The output pulse rate on CF can be up to 128 times the pulse rate on F1 and F2. The lower the F1-4 frequency selected the higher the CF scaling. Table IV shows how the two frequencies are related depending on the states of the logic inputs S0, S1 and SFC. Because of its relatively high pulse rate, the frequency at this logic output is proportional to the instantaneous real power. As is the case with F1 and F2 the frequency is derived from the output of the low pass filter after multiplication. However because the output frequency is high, this real power information is accumulated over a much shorter time. Hence less averaging is carried out in the digital to frequency conversion. With much less averaging of the real power signal, the CF output is much more responsive to power

fluctuations—see Signal Processing Block in figure 5.

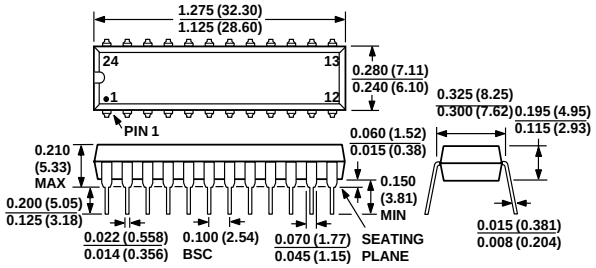
TABLE IV

SCF	S1	S0	F_{1-4} (Hz)	CF max for ac signals (Hz)
1	0	0	0.85	128 x Freq = 10.88
0	0	0	0.85	64 x Freq = 5.44
1	0	1	1.7	64 x Freq = 10.88
0	0	1	1.7	32 x Freq = 5.44
1	1	0	3.41	32 x Freq = 10.88
0	1	0	3.41	16 x Freq = 5.44
1	1	1	6.83	16 x Freq = 10.88
0	**1**	**1**	**6.83**	**2048 x Freq = 5.57kHz**

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead Plastic DIP (N-24)



24-Shrink Small Outline Package (RS-24)