Features

- 8-bit Multiplexed Addresses/Outputs
- Fast Read Access Time – 70 ns
- Dual Voltage Range Operation
  – Low-voltage Power Supply Range, 3.0V to 3.6V, or
  – Standard 5V ± 10% Supply Range
- Pin Compatible with Standard AT27C520
- Low-power CMOS Operation
  – 20 µA max. Standby for ALE = V_{IH} and V_{CC} = 3.6V
  – 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Packages
  – 20-lead TSSOP
  – 20-lead SOIC
- High-reliability CMOS Technology
  – 2,000V ESD Protection
  – 200 mA Latch-up Immunity
- Rapid™ Programming Algorithm – 50 µs/Byte (Typical)
- CMOS- and TTL-compatible Inputs and Outputs
  – JEDEC Standard for LVTTL
- Integrated Product Identification Code
- Commercial and Industrial Temperature Range

512K (64K x 8) Multiplexed Addresses/ Outputs Low-voltage OTP EPROM

AT27LV520

Description

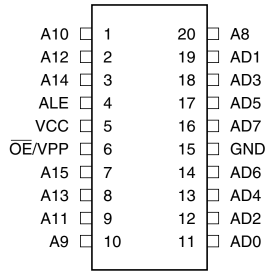
The AT27LV520 is a low-power, high-performance, 524,288-bit one-time programmable read-only memory (OTP EPROM) organized 64K by eight bits. It incorporates latches for the eight lower order address bits to multiplex with the eight data bits. This minimizes system chip count, reduces cost, and simplifies the design of multiplexed bus systems. It requires only one power supply in the range of 3.0V to 3.6V for normal read mode operation, making it ideal for fast, portable systems using battery power. Any byte can be accessed in less than 70 ns.

The AT27LV520 is available in 173 mil, 20-lead TSSOP and 300 mil, 20-lead SOIC, one-time programmable (OTP) plastic packages. *(continued)*

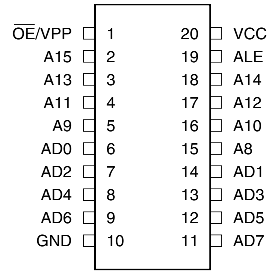
Pin Configurations

Pin Name	Function
A8 - A15	Addresses
AD0 - AD7	Addresses/Outputs
$\overline{OE}$ /VPP	Output Enable/Program Supply
ALE	Address Latch Enable

TSSOP Top View



SOIC Top View



Rev. 0911D–05/00

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3.3V supply. At V_{CC} = 3.0V, any byte can be accessed in less than 70 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3.3V, the AT27LV520 consumes less than one fifth the power of a standard 5V EPROM. Standby mode is achieved by asserting ALE high. Standby mode supply current is typically less than 1 µA at 3.3V.

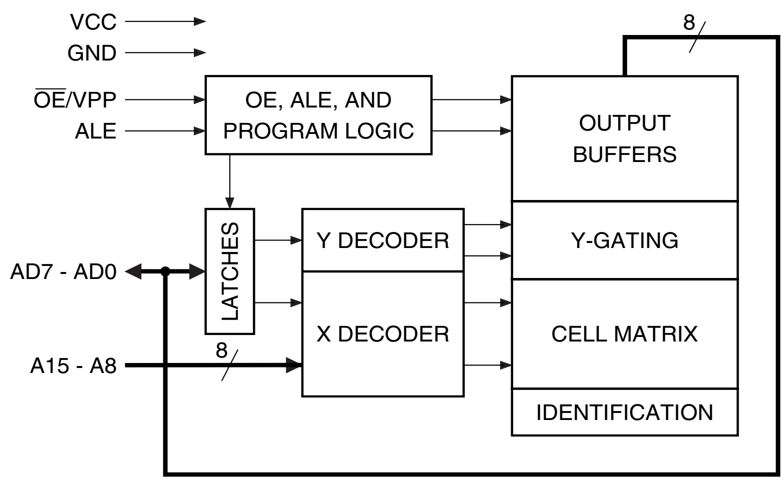
The AT27LV520 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are plugable in both 3-volt and 5-volt hosts.

Atmel's AT27LV520 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programing time is typically only 50 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV520 programs exactly the same way as a standard 5V AT27C520 and uses the same programming equipment.

System Considerations

Switching under active conditions may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode/Pin	ALE	$\overline{OE}/V_{PP}$	A8 - A15	AD0 - AD7
Read(2)	V_{IL}	V_{IL}	Ai	D_{OUT}
Output Disable(2)	V_{IL}/V_{IH}	V_{IH}	X(1)	High Z/A0 - A7
Standby	V_{IH}	V_{IH}	Ai	A0 - A7
Address Latch Enable(2)	V_{IH}	V_{IH}	X	A0 - A7
Rapid Program(3)	V_{IH}	V_{PP}	Ai	D_{IN}
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H(5) A8 = V_{IH} or V_{IL} A10 - A15 = V_{IL}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require 3.0V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All A8 - A15 inputs are held low (V_{IL}), except A9 which is set to V_H and A8 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27LV520-70	AT27LV520-90
Operating Temp. (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - +85°C	-40°C - +85°C
V_{CC} Supply		3.0V to 3.6V	3.0V to 3.6V
		5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 3.0V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{SB} (1)	V_{CC} Standby Current	ALE = V_{CC} ± 0.3V; Ai, ADi = GND/V_{CC} ± 0.3V		20	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, ALE = V_{IL}		8	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{SB} (1)	V_{CC} Standby Current	ALE = V_{CC} ± 0.3V; Ai, ADi = GND/V_{CC} ± 0.3V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, ALE = V_{IL}		20	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		

Note: 1. V_{CC} standby current will be slightly higher with ALE, Ai, and ADi at TTL levels.

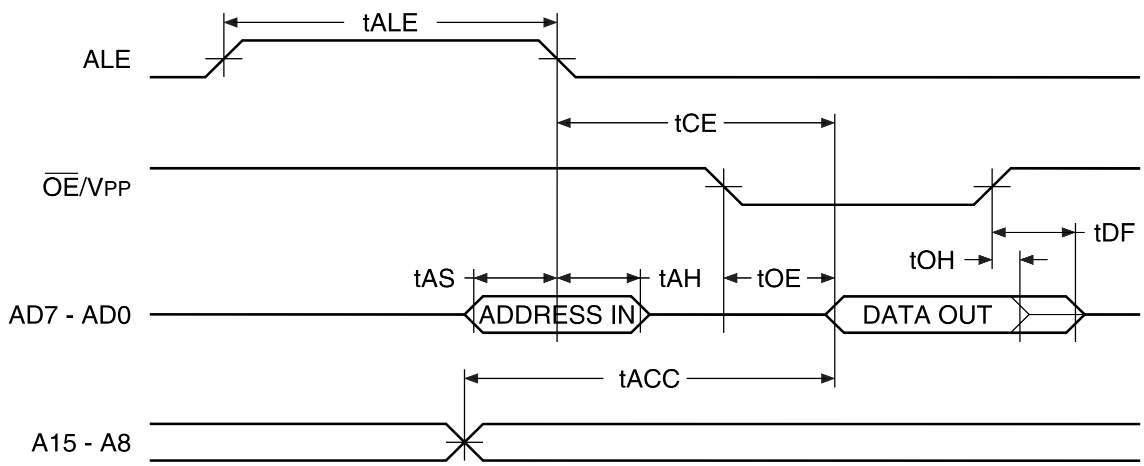
AC Characteristics for Read Operation

V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V

Symbol	Parameter	Condition	AT27LV520-70		AT27LV520-90		Units
			Min	Max	Min	Max	
t_{ACC} (3)	Address to Output Delay	ALE = $\overline{OE}/V_{PP}$ = V_{IL}		70		90	ns
t_{CE}	Address Latch Enable Low to Output Delay	Address Valid		55		70	ns
t_{AS}	Address Setup Time	$\overline{OE}/V_{PP}$ = V_{IH}	12		15		ns
t_{AH}	Address Hold Time	$\overline{OE}/V_{PP}$ = V_{IH}	12		15		ns
t_{ALE}	Address Latch Enable Width	$\overline{OE}/V_{PP}$ = V_{IH}	40		45		ns
t_{OE} (3)	$\overline{OE}/V_{PP}$ to Output Delay	ALE = V_{IL}		30		35	ns
t_{DF} (4)(5)	$\overline{OE}/V_{PP}$ High to Output Float	ALE = V_{IL}		25		25	ns
t_{OH}	Output Hold from Address or $\overline{OE}/V_{PP}$, whichever occurred first	ALE = V_{IL}	7		0		ns

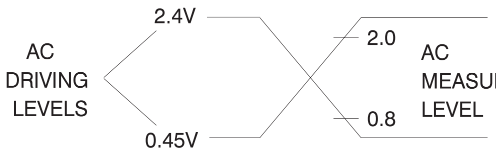
Note: 3, 4, 5 — see AC Waveforms for Read Operation

AC Waveforms for Read Operation(1)



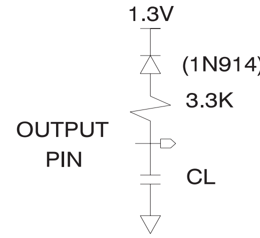
Notes:
1. Timing measurement reference levels for all speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE} - t_{OE} after the address is valid without impact on t_{CE}.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



Note: C_L = 100 pF including jig capacitance.

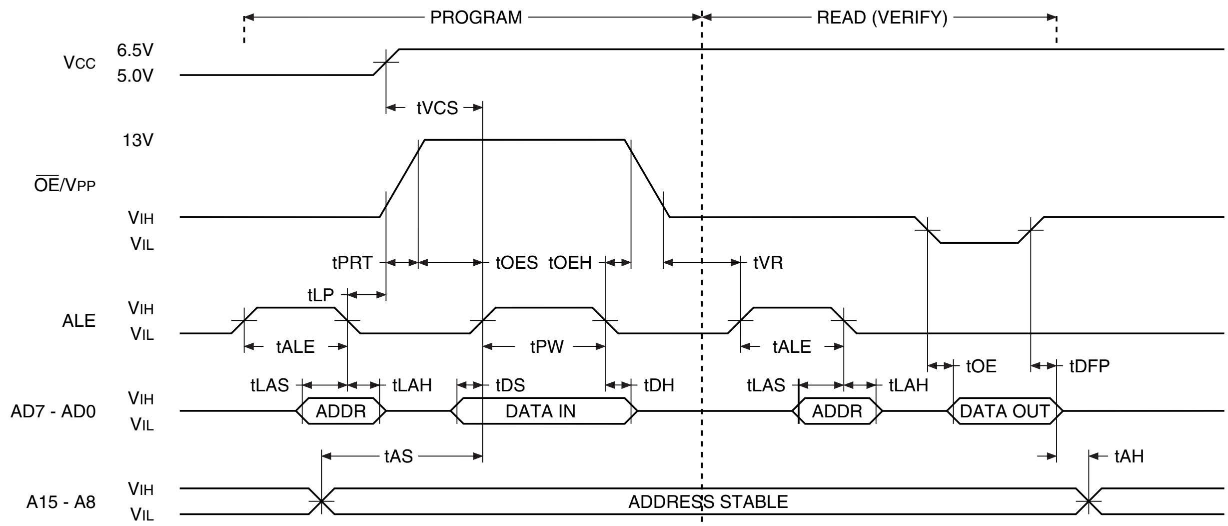
Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

DC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC} + 1.0$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	ALE = V_{IH}		25	mA

AC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter[1]	Test Conditions	Limits		Units
			Min	Max	
t_{ALE}	Address Latch Enable Width	Input Rise and Fall Times: (10% to 90%) 20 ns Input Pulse Levels: 0.45V to 2.4V Input Timing Reference Level: 0.8V to 2.0V Output Timing Reference Level: 0.8V to 2.0V	500		ns
t_{LAS}	Latched Address Setup Time		100		ns
t_{LAH}	Latched Address Hold Time		100		ns
t_{LP}	ALE Low to $\overline{OE}/V_{PP}$ High Voltage Delay		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{DH}	Data Hold Time		2		µs
t_{PW}	ALE Program Pulse Width[2]		47.5	52.5	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{OE}	Data Valid from $\overline{OE}/V_{PP}$			150	ns
t_{DFP}	$\overline{OE}/V_{PP}$ High to Output Float Delay[3]		0	130	ns
t_{AS}	Address Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Program Pulse width tolerance is 50 µsec ± 5%.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.

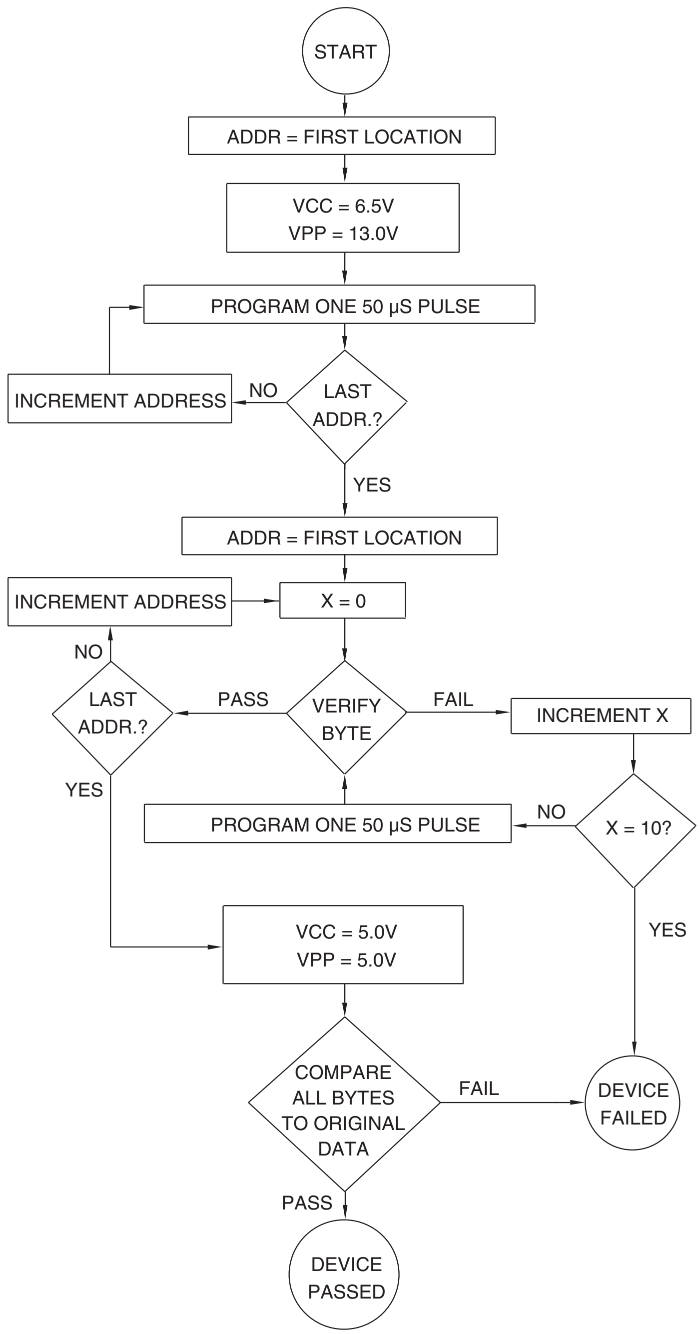
Atmel's 27LV520 Integrated Product Identification Code

Codes	Pins									Hex Data
	A8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	1	1	1	0	1	9D

Note: 1. The AT27LV520 has the same product identification code as the AT27C520. Both are programming compatible.

Rapid™ Programming Algorithm

A 50 µs ALE pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 50 µs ALE pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IH} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



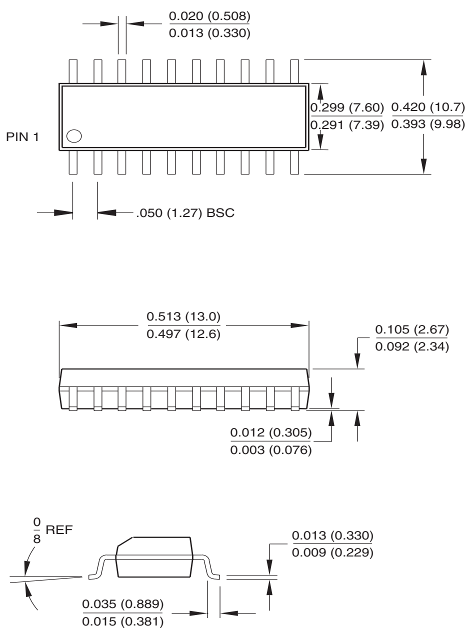
Ordering Information

t_{ACC} (ns)	I_{CC} (mA) Active	Ordering Code	Package	Operation Range
90	8	AT27LV520-90SC AT27LV520-90XC	20S 20X	Commercial (0°C to 70°C)
		AT27LV520-90SI AT27LV520-90XI	20S 20X	Industrial (-40°C to +85°C)
70	8	AT27LV520-70SC AT27LV520-70XC	20S 20X	Commercial (0°C to 70°C)
		AT27LV520-70SI AT27LV520-70XI	20S 20X	Industrial (-40°C to +85°C)

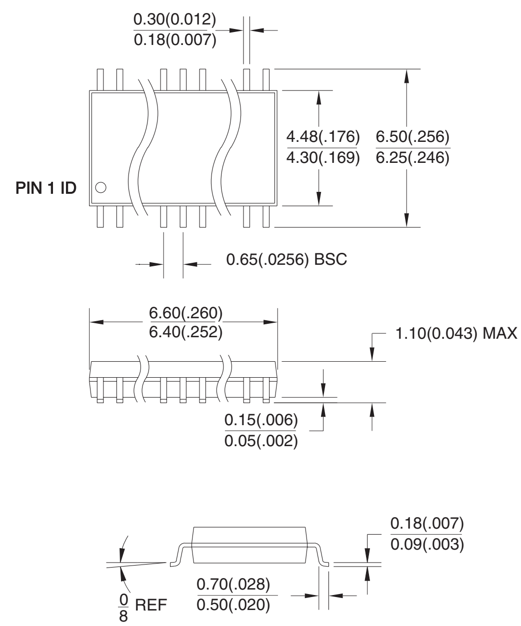
Package Type	
20S	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
20X	20-lead, 0.173" Wide, Thin Shrink Small Outline (TSSOP)

Packaging Information

20S, 20-lead, 0.300" Wide,
Plastic Gull Wing Small Outline
Dimensions in Inches and (Millimeters)



20X, 20-lead, 0.173" Wide,
Thin Super Small Outline Package (TSSOP)
Dimensions in (Millimeters) and Inches



Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

0911D–05/00/xM