

PowerMOS transistor
Logic level TOPFET

BUK107-50DL

DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving

- lamps
- small motors
- solenoids

FEATURES

- Vertical power DMOS output stage
- Overload protected up to 85°C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	0.7	A
P_D	Total power dissipation	1.8	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	200	mΩ

FUNCTIONAL BLOCK DIAGRAM

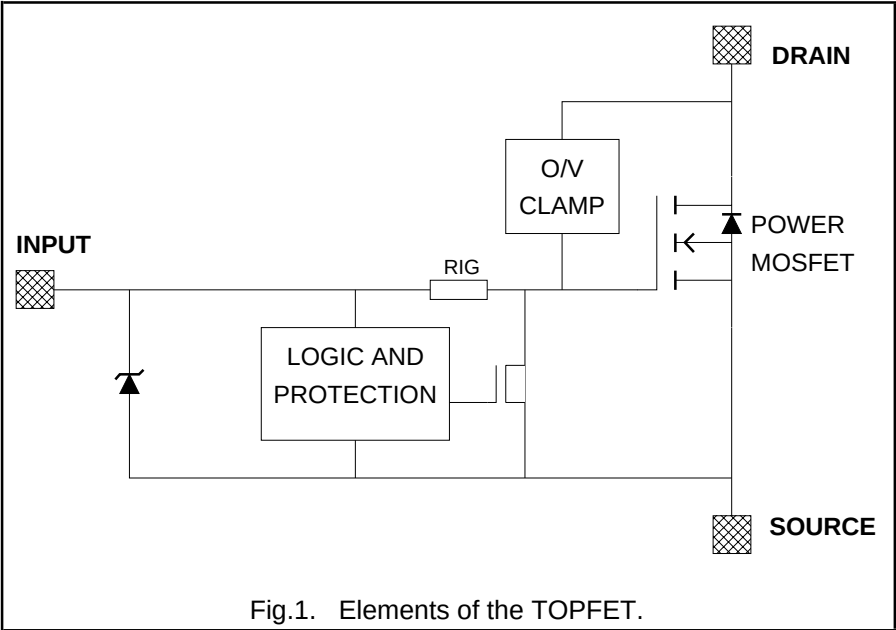
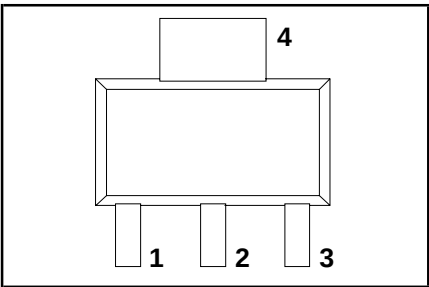


Fig.1. Elements of the TOPFET.

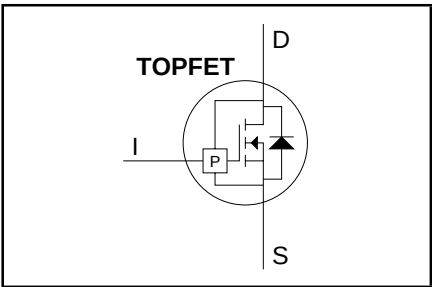
PINNING - SOT223

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



PowerMOS transistor

Logic level TOPFET

BUK107-50DL

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage ¹	-	-	50	V
I_D	Continuous drain current ²	-	-	self limiting	A
I_I	Continuous input current	clamping	-	3	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
P_D	Total power dissipation	$T_{amb} = 25$ °C	-	1.8	W
T_{stg}	Storage temperature	-	-55	150	°C
T_J	Continuous junction temperature	normal operation ³	-	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 k Ω	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$T_b \leq 25$ °C; $I_{DM} < I_{D(lim)}$; inductive load	-	100	mJ
E_{DRM}	Repetitive clamping energy	$T_b \leq 75$ °C; $I_{DM} = 50$ mA; f = 250 Hz	-	4	mJ

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads. Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDP}	Protected drain source supply voltage	$V_{IS} = 5$ V	-	35	V
		$V_{IS} = 4$ V	-	16	V

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{D(lim)}$	Overload protection Drain current limiting	$V_{IS} = 5$ V	0.7	1.1	1.5	A
$T_{J(TO)}$	Overtemperature protection Threshold junction temperature	only in drain current limiting $V_{IS} = 5$ V	100	130	160	°C

¹ Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

² Refer to OVERLOAD PROTECTION CHARACTERISTICS.

³ Not in an overload condition with drain current limiting.

PowerMOS transistor

Logic level TOPFET

BUK107-50DL

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance Junction to solder point		-	12	18	K/W
$R_{th\ j-b}$	Junction to board ¹	Mounted on any PCB	-	40	-	K/W
$R_{th\ j-a}$	Junction to ambient	Mounted on PCB of fig. 19	-	-	70	K/W

STATIC CHARACTERISTICS

 $T_b = 25\ ^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0\ \text{V}$; $I_D = 10\ \text{mA}$	50	55	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0\ \text{V}$; $I_{DM} = 200\ \text{mA}$; $t_p \leq 300\ \mu\text{s}$; $\delta \leq 0.01$	-	56	70	V
I_{DSS}	Off-state drain current	$V_{DS} = 45\ \text{V}$; $V_{IS} = 0\ \text{V}$	-	0.5	2	μA
I_{DSS}	Off-state drain current	$V_{DS} = 50\ \text{V}$; $V_{IS} = 0\ \text{V}$	-	1	20	μA
I_{DSS}	Off-state drain current	$V_{DS} = 40\ \text{V}$; $V_{IS} = 0\ \text{V}$; $T_j = 100\ ^\circ\text{C}$	-	10	100	μA
$R_{DS(ON)}$	Drain-source on-state resistance ²	$V_{IS} = 5\ \text{V}$; $I_{DM} = 100\ \text{mA}$; $t_p \leq 300\ \mu\text{s}$; $\delta \leq 0.01$	-	150	200	m Ω

INPUT CHARACTERISTICS

 $T_b = 25\ ^\circ\text{C}$ unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	$V_{DS} = 5\ \text{V}$; $I_D = 1\ \text{mA}$	1.7	2.2	2.7	V
I_{IS}	Input supply current	normal operation; $V_{IS} = 5\ \text{V}$	-	330	450	μA
		$V_{IS} = 4\ \text{V}$	-	170	270	μA
I_{ISL}	Input supply current	protection latched; $V_{IS} = 5\ \text{V}$	-	500	650	μA
		$V_{IS} = 3.5\ \text{V}$	-	250	400	μA
V_{ISR}	Protection latch reset voltage ³		1	2.2	3.5	V
$V_{(CL)IS}$	Input clamping voltage	$I_l = 1.5\ \text{mA}$	6	7.5	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	33	-	k Ω

SWITCHING CHARACTERISTICS

 $T_{amb} = 25\ ^\circ\text{C}$; resistive load $R_L = 50\ \Omega$; adjust V_{DD} to obtain $I_D = 250\ \text{mA}$; refer to test circuit and waveforms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	$V_{IS} = 0\ \text{V}$ to $V_{IS} = 5\ \text{V}$	-	8	-	μs
t_r	Rise time		-	30	-	μs
$t_{d\ off}$	Turn-off delay time	$V_{IS} = 5\ \text{V}$ to $V_{IS} = 0\ \text{V}$	-	3	-	μs
t_f	Fall time		-	6	-	μs

¹ Temperature measured 1.3 mm from tab.² Continuous input voltage. The specified pulse width is for the drain current.³ The input voltage below which the overload protection circuits will be reset.

PowerMOS transistor

Logic level TOPFET

BUK107-50DL

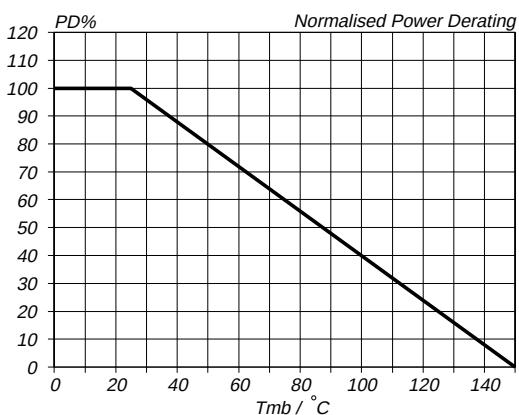


Fig.2. Normalised limiting power dissipation.
 $P_D\% = 100 \cdot P_D / P_D(25^\circ\text{C}) = f(T_{mb})$

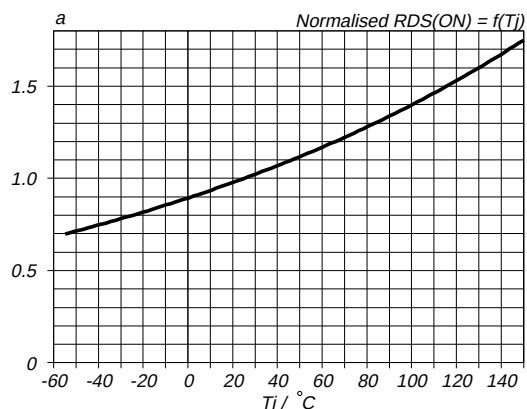


Fig.5. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)} / R_{DS(ON)25^\circ\text{C}} = f(T_j)$; $I_D = 100\text{ mA}$; $V_{IS} = 5\text{ V}$

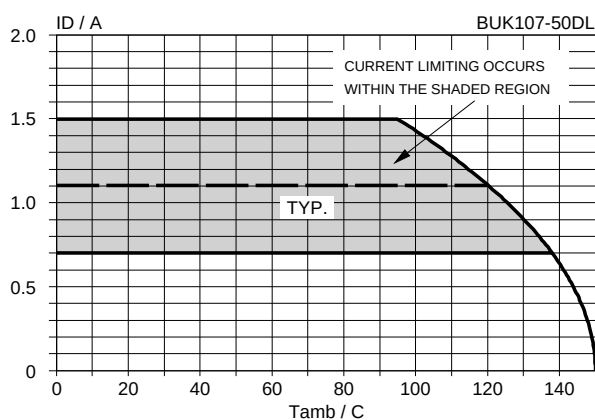


Fig.3. Continuous drain current.
 $I_D = f(T_{amb})$; condition: $V_{IS} = 5\text{ V}$

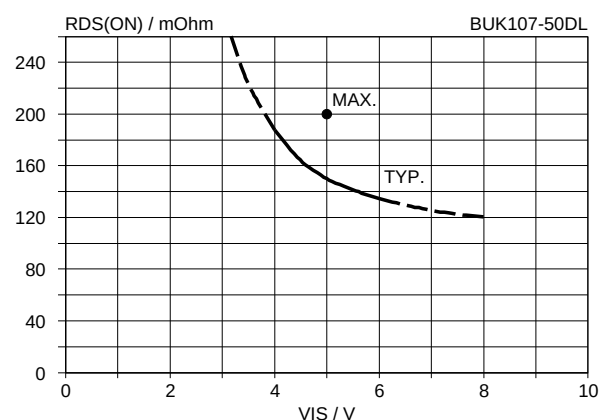


Fig.6. Typical on-state resistance, $T_j = 25^\circ\text{C}$.
 $R_{DS(ON)} = f(V_{IS})$; conditions: $I_D = 100\text{ mA}$, $t_p = 300\text{ }\mu\text{s}$

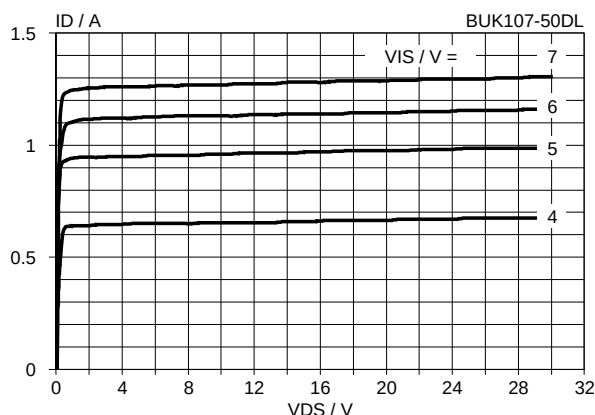


Fig.4. Typical on-state characteristics, $T_j = 25^\circ\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{IS} ; $t_p = 300\text{ }\mu\text{s}$

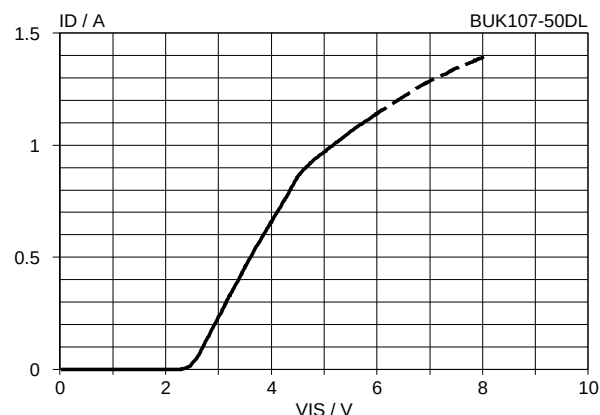
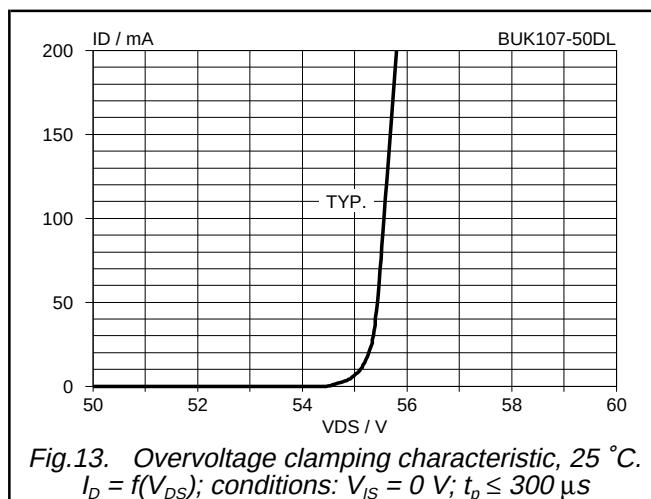
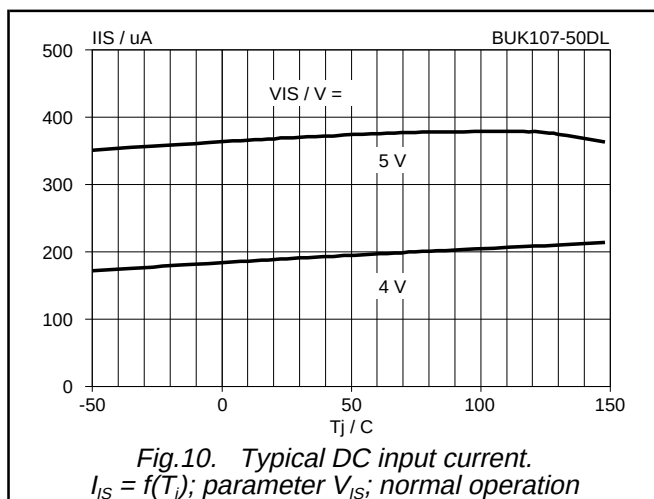
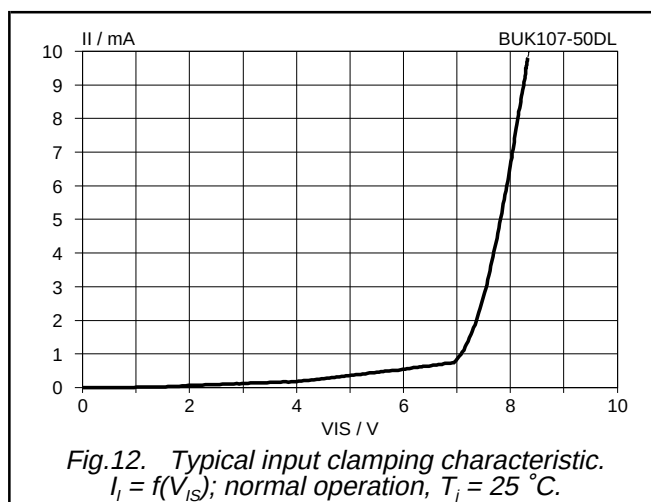
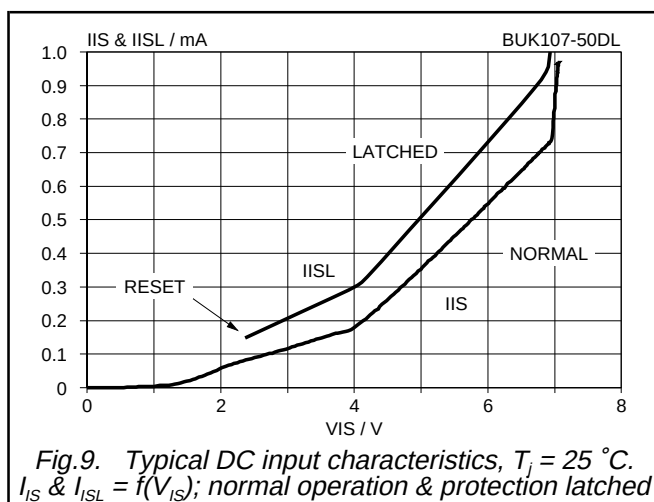
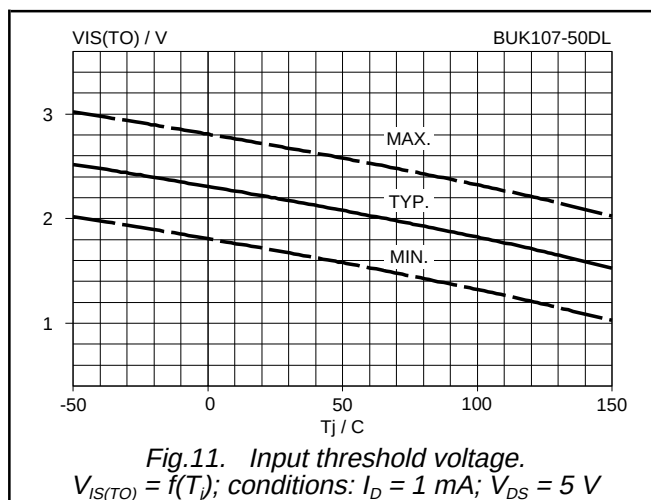
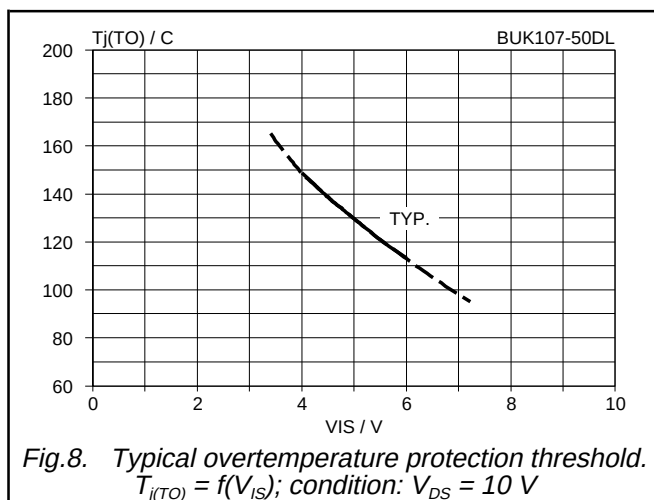


Fig.7. Typical transfer characteristics, $T_j = 25^\circ\text{C}$.
 $I_D = f(V_{IS})$; conditions: $V_{DS} = 10\text{ V}$, $t_p = 300\text{ }\mu\text{s}$

PowerMOS transistor

Logic level TOPFET

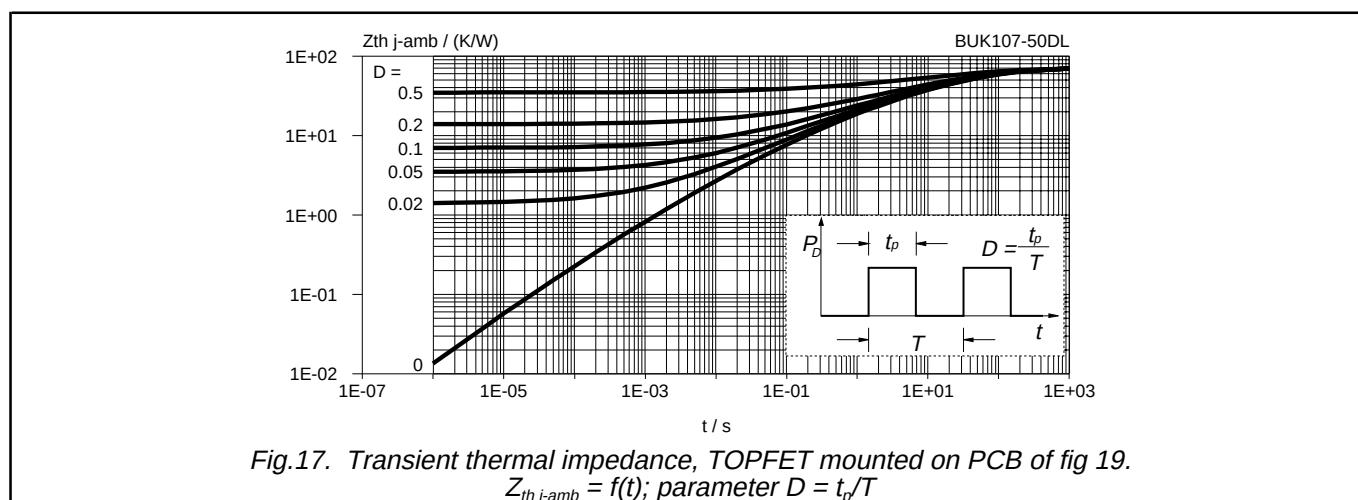
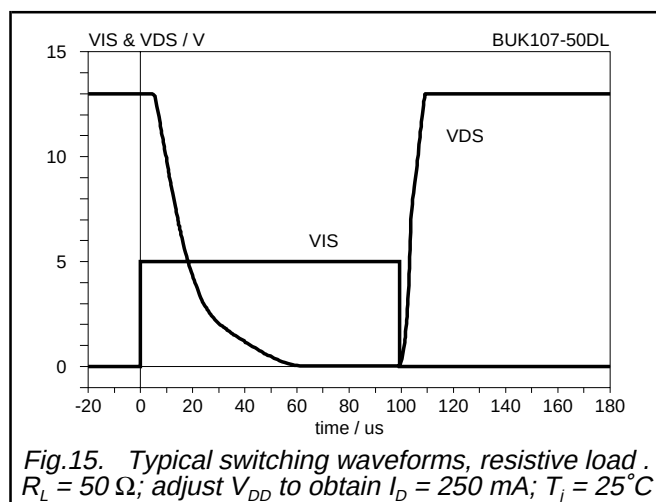
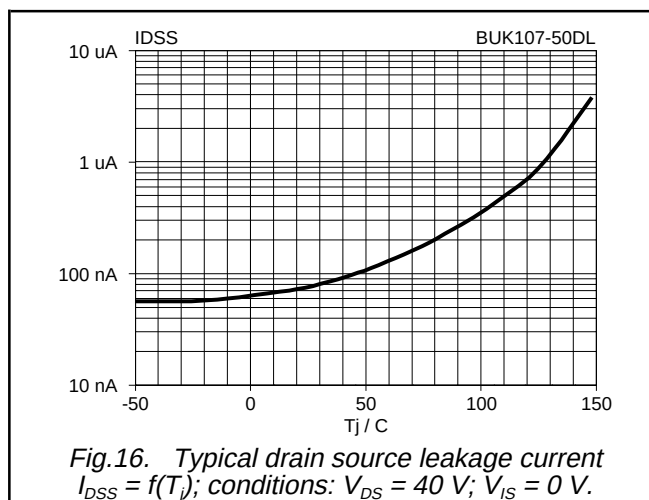
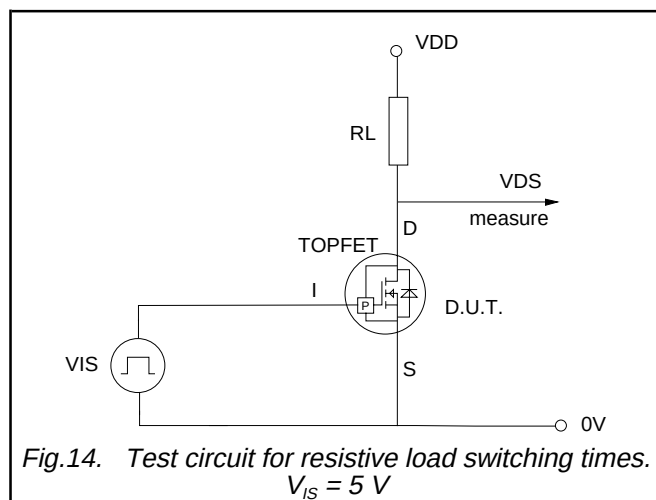
BUK107-50DL



PowerMOS transistor

Logic level TOPFET

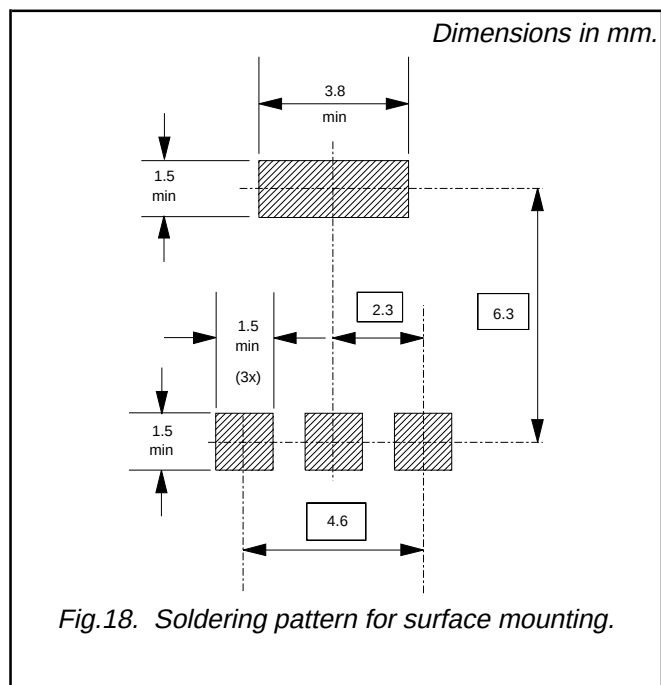
BUK107-50DL



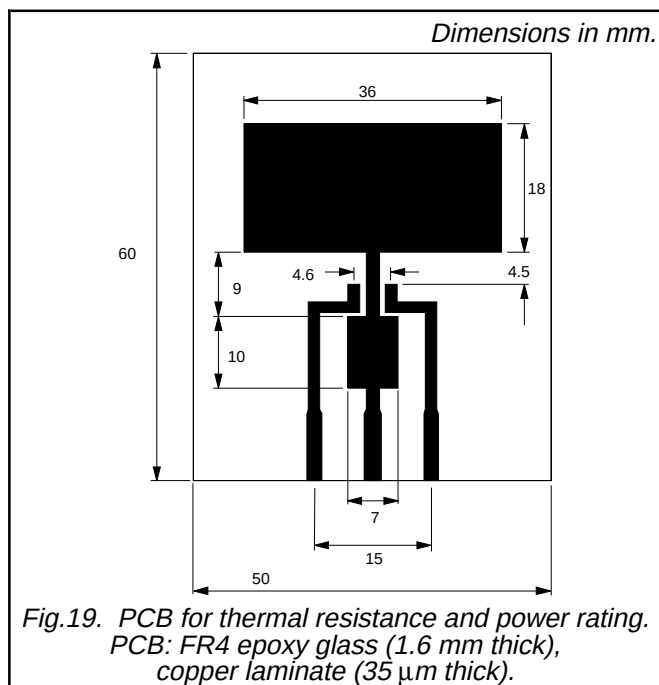
PowerMOS transistor Logic level TOPFET

BUK107-50DL

MOUNTING INSTRUCTIONS



PRINTED CIRCUIT BOARD



PowerMOS transistor Logic level TOPFET

BUK107-50DL

MECHANICAL DATA

Dimensions in mm

Net Mass: 0.11 g

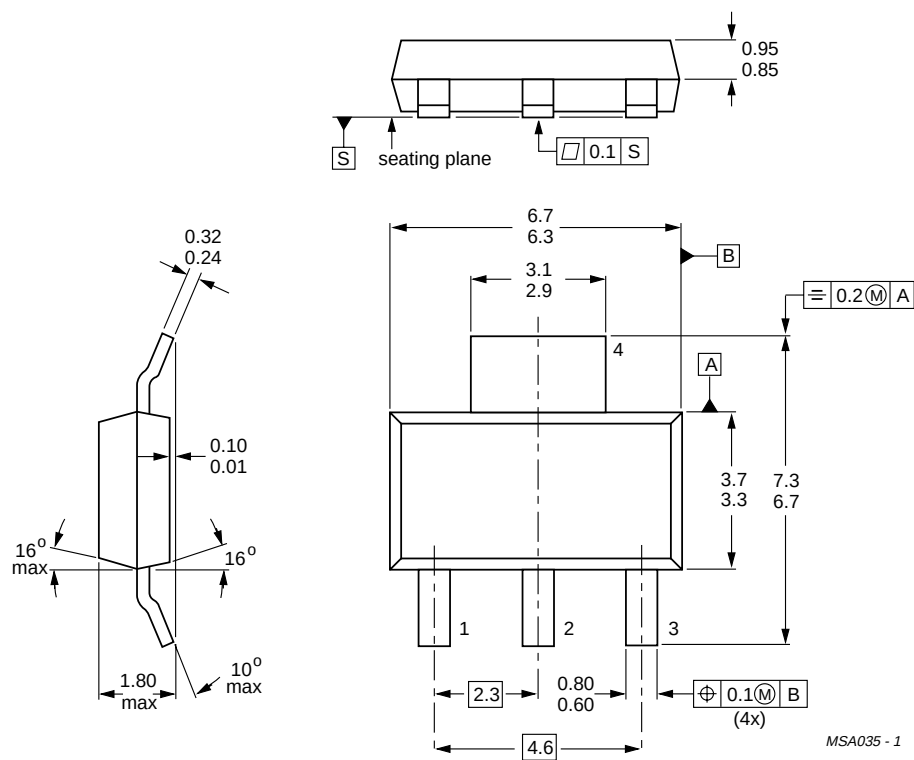


Fig.20. SOT223 surface mounting package¹.

¹ For further information, refer to surface mounting instructions for SOT223 envelope. Epoxy meets UL94 V0 at 1/8".

PowerMOS transistor
Logic level TOPFET

BUK107-50DL

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 1997	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.