# CS403

# 5.0 V, 750 mA Linear Regulator with $\overline{\text{RESET}}$

The CS403 is a linear regulator specially designed as a post regulator. The CS403 provides low noise, low drift, and high accuracy to improve the performance of a switching power supply. It is ideal for applications requiring a highly efficient and accurate linear regulator. The active $\overline{\text{RESET}}$ makes the device particularly well suited to supply microprocessor based systems. The PNP–NPN output stage assures a low dropout voltage without requiring excessive supply current. Its features include low dropout (1.0 V typically) and low supply drain (4.0 mA typical with $I_{OUT}$ = 500 mA).

The CS403 design optimizes supply rejection by switching the internal reference from the supply input to the regulator output as soon as the nominal output voltage is reached.

### Features

- 5.0 V ± 3.0% Output Voltage
- Low Drift
- High Efficiency
- Short Circuit Protection
- Active Delayed Reset
- Noise Immunity on Reset
- 750 mA Output Current

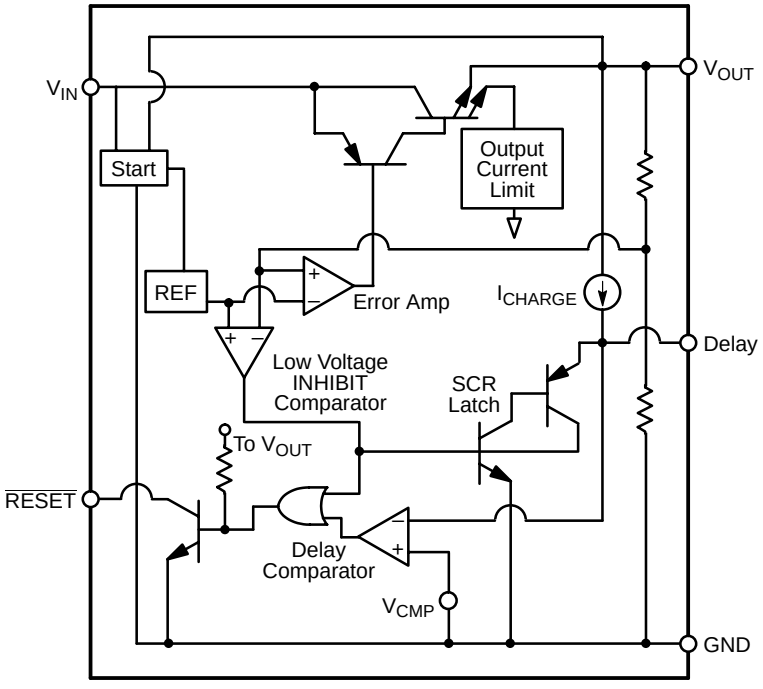


**Figure 1. Block Diagram**

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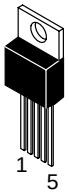
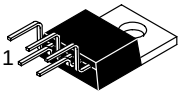
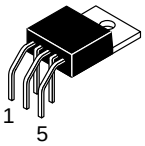



**TO–220**
**FIVE LEAD**
**T SUFFIX**
**CASE 314D**

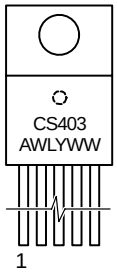



**TO–220**
**FIVE LEAD**
**TVA SUFFIX**
**CASE 314K**




**TO–220**
**FIVE LEAD**
**THA SUFFIX**
**CASE 314A**

**PIN CONNECTIONS AND MARKING DIAGRAM**




Tab = GND
Pin 1. $V_{IN}$
2. $\overline{\text{RESET}}$
3. GND
4. Delay
5. $V_{OUT}$

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| CS403GT5 | TO–220* STRAIGHT | 50 Units/Rail |
| CS403GTVA5 | TO–220* VERTICAL | 50 Units/Rail |
| CS403GTHA5 | TO–220* HORIZONTAL | 50 Units/Rail |

*Five lead.

## ABSOLUTE MAXIMUM RATINGS*

| Rating | | Value | Unit |
|---|---|---|---|
| Forward Input Voltage | | 18 | V |
| Operating Junction Temperature, $T_J$ | | –40 to 150 | °C |
| Storage Temperature Range, $T_S$ | | –55 to +150 | °C |
| Lead Temperature Soldering: | Wave Solder: (through hole styles only) (Note 1.) | 260 peak | °C |

1. 10 second maximum.

*The maximum package power dissipation must be observed.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, –40°C ≤ $T_C$ ≤ 125°C, –40°C ≤ $T_J$ ≤ 150°C, 7.0 V ≤ $V_{IN}$ ≤ 10 V, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage, $V_{OUT}$ | $V_{IN}$ = 8.5 V, $I_{OUT}$ = 250 mA, $T_J$= 25°C<br>100 mA ≤ $I_{OUT}$ ≤ 750 mA | 4.95<br>4.85 | 5.00<br>5.00 | 5.05<br>5.15 | V<br>V |
| Operating Input Voltage | 100 to 750 mA | –0.75 | – | 18.0 | V |
| Load Regulation | 100 mA ≤ $I_{OUT}$ ≤ 750 mA, $V_{IN}$ = 8.5 V | – | 30 | 100 | mV |
| Dropout Voltage | $I_{OUT}$ = 750 mA | – | 1.4 | 1.8 | V |
| Quiescent Current | $I_{OUT}$ = 0 mA<br>$I_{OUT}$ = 750 mA | –<br>– | 3.0<br>5.0 | 4.0<br>25 | mA<br>mA |
| PSRR | $I_{OUT}$ – 250 mA, f = 120 Hz<br>$C_{OUT}$ = 10 μF, $V_{IN}$ = 8.5 V + $V_{pp}$ | – | 70 | – | dB |
| Output Short Circuit Current | – | – | 1.0 | – | A |
| Reset Output Voltage | $I_R$ = 1.6 mA, 1.0 ≤ $V_{OUT}$ ≤ 4.75 V | – | 0.08 | 0.40 | V |
| Reset Output Leakage Current | $V_{OUT}$ in regulation | – | 0 | 50 | μA |
| Delay Time for Reset Output | $C_d$ = 100 nF | 10 | 20 | 30 | ms |
| Reset Threshold, $V_{RTH}$ | $V_{OUT}$ Increasing | – | – | $V_{OUT}$ – 0.04 | V |
| Reset Threshold, $V_{RTL}$ | $V_{OUT}$ Decreasing | 4.75 | – | – | V |
| Threshold Hysteresis | – | 10 | 50 | – | mV |
| Delay, $V_{DTC}$ | Charge | 3.7 | 4.0 | 4.4 | V |
| Delay, $V_{DTD}$ | Discharge | 3.1 | 3.5 | 3.9 | V |
| Delay Hysteresis, $V_{DH}$ | – | 200 | 500 | 1000 | mV |
| Reset Delay Capacitor Charging Current, $I_{CH}$ | – | 10 | 20 | 40 | μA |
| Reset Delay Capacitor Discharge Voltage, $V_{DIS}$ | – | – | 0.6 | 1.2 | V |

## PACKAGE PIN DESCRIPTION

| PACKAGE LEAD #<br>5 Lead TO–220 | LEAD SYMBOL | FUNCTION |
|---|---|---|
| 1 | $V_{IN}$ | Input voltage. |
| 2 | $\overline{\text{RESET}}$ | CMOS compatible output lead. $\overline{\text{RESET}}$ goes low whenever $V_{OUT}$ falls out of regulation. |
| 3 | GND | Ground connection. |
| 4 | Delay | Timing capacitor for $\overline{\text{RESET}}$ function. |
| 5 | $V_{OUT}$ | Regulated output voltage, 5.0 V (typ). |

## TYPICAL PERFORMANCE CHARACTERISTICS

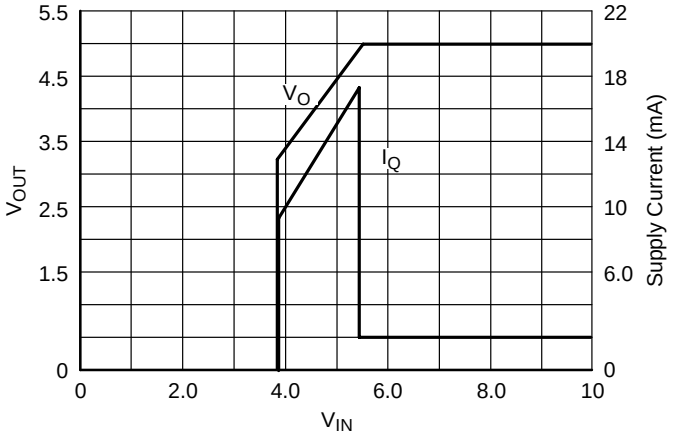



**Figure 2. Output Voltage vs. $V_{IN}$, $I_Q$**

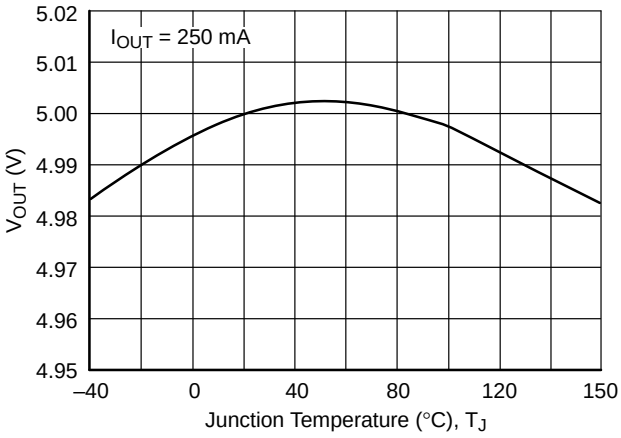



**Figure 3. Output Voltage vs. Junction Temperature**

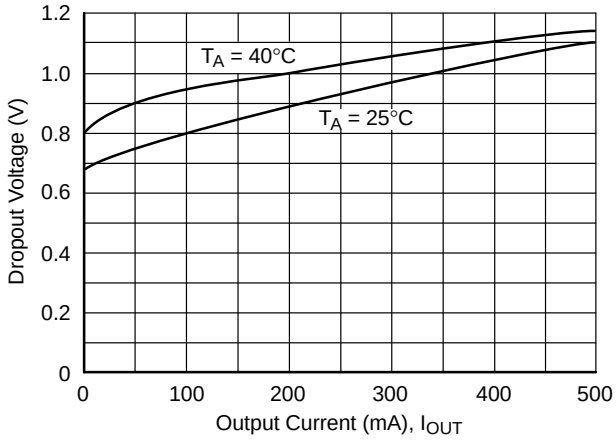
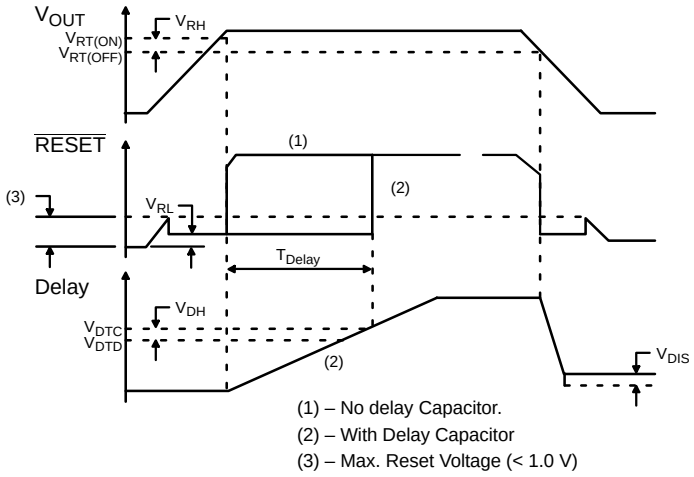



**Figure 4. Dropout Voltage vs. Output Current Over Temperature**

## RESET CIRCUIT




(1) – No delay Capacitor.
(2) – With Delay Capacitor
(3) – Max. Reset Voltage (< 1.0 V)

**Figure 5. Reset Circuit Waveform**

## CIRCUIT DESCRIPTION

The CS403 $\overline{\text{RESET}}$ function is very precise, has hysteresis on both the $\overline{\text{RESET}}$ and Delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1.0 V.

The $\overline{\text{RESET}}$ circuit output is an open collector type with ON and OFF parameters as specified. The $\overline{\text{RESET}}$ output NPN transistor is controlled by the two circuits described (see Figure 1).

### Low Voltage Inhibit Circuit

This circuit monitors output voltage, and when output voltage is below the specified minimum, causes the $\overline{\text{RESET}}$ output transistor to be in the ON (saturation) state. When the output voltage is above the specified level, this circuit permits the $\overline{\text{RESET}}$ output transistor to go into the OFF state if allowed by the reset Delay circuit.

### Reset Delay Circuit

This circuit provides a programmable (external capacitor) delay on the $\overline{\text{RESET}}$ output lead. The Delay lead provides source current to the external delay capacitor only when the Low Voltage Inhibit circuit indicates that output voltage is above $V_{RT(ON)}$. Otherwise, the Delay lead sinks current to ground (used to discharge the Delay capacitor). The discharge current is latched ON when the output voltage is below $V_{RT(OFF)}$, or when the voltage on the Delay capacitor is above $V_{DIS}$. In other words, the Delay capacitor is fully discharged any time the output voltage falls out of regulation, even for a short period of time. This feature ensures a controlled $\overline{\text{RESET}}$ pulse is generated following detection of an error condition. The circuit allows the $\overline{\text{RESET}}$ output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than $V_{DIS}$.

$$t_d = C_d \times V_{DTC}/I_{CH} = C_{Delay} \times 2.10^5 \text{ (typical)}.$$

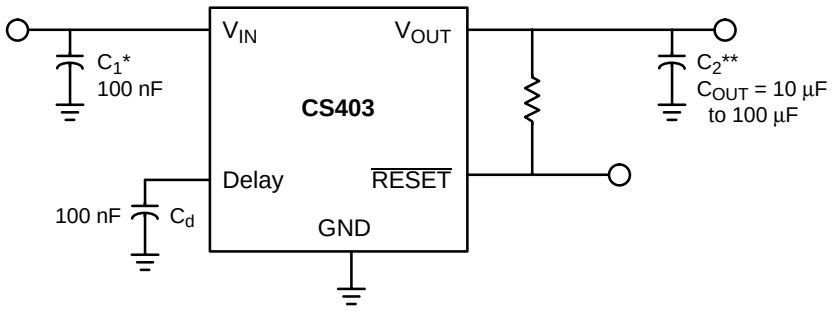
where:

$t_d$ = Time delay.

$C_d$ = Value of external charging capacitor (see Figure 6).

$V_{DTC}$ = Delay Threshold charge.

$I_{ch}$ = Reset delay capacitor charging current.




$C_1$* is required if the regulator is far from the power source filter.
$C_2$** is required for stability.

**Figure 6. Test Circuit**

## APPLICATION NOTES

### Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start–up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (–25°C to –40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor $C_{OUT}$ shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for $C_{OUT}$ for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

**Step 1:** Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the

higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

**Step 2:** With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

**Step 3:** Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

**Step 4:** Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

**Step 5:** If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

**Step 6:** Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

**Step 7:** Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ± 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

### Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 7) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current, for the application, and

$I_Q$ is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

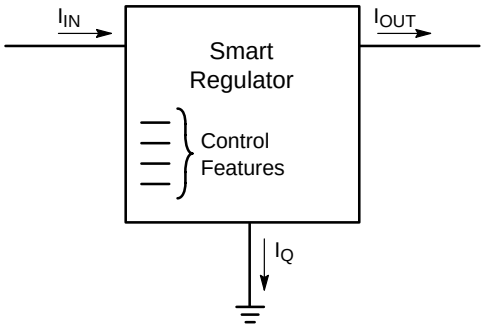



**Figure 7. Single Output Regulator With Key Performance Parameters Labeled**

### Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

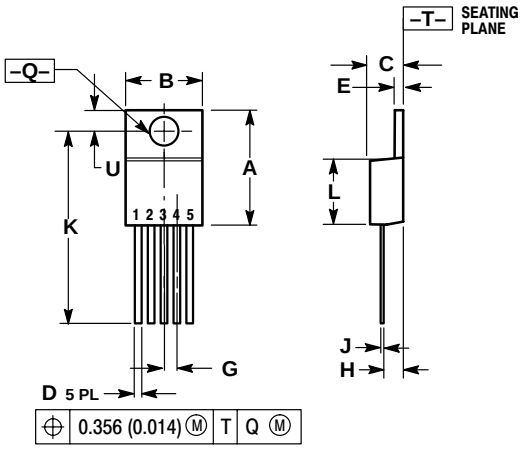
$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## PACKAGE DIMENSIONS

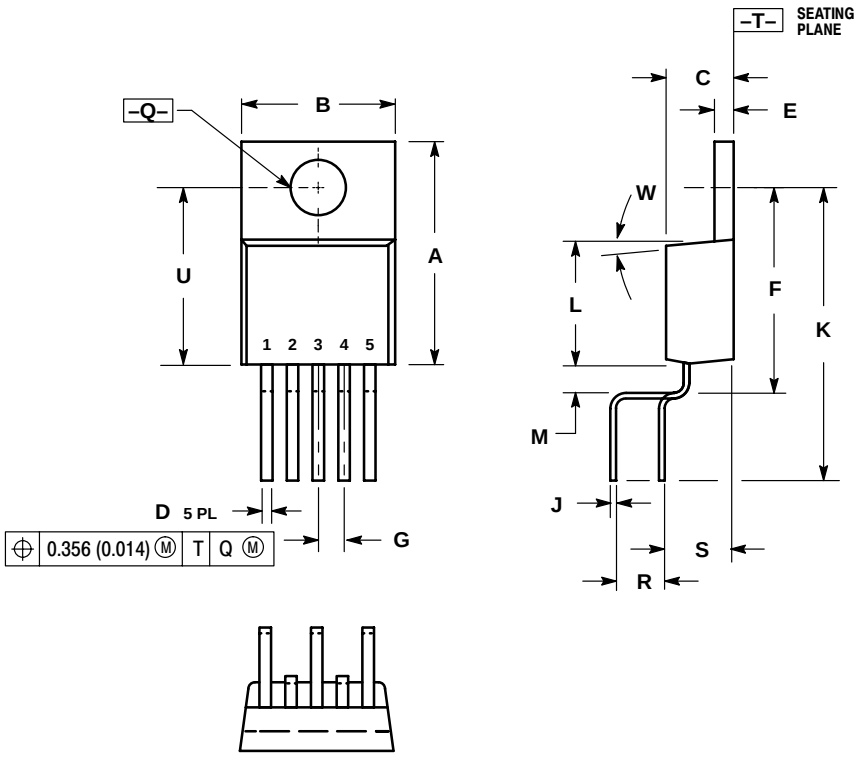
**TO–220**
**FIVE LEAD**
**T SUFFIX**
CASE 314D–04
ISSUE E




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.572 | 0.613 | 14.529 | 15.570 |
| B | 0.390 | 0.415 | 9.906 | 10.541 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.025 | 0.038 | 0.635 | 0.965 |
| E | 0.048 | 0.055 | 1.219 | 1.397 |
| G | 0.067 BSC | | 1.702 BSC | |
| H | 0.087 | 0.112 | 2.210 | 2.845 |
| J | 0.015 | 0.025 | 0.381 | 0.635 |
| K | 0.990 | 1.045 | 25.146 | 26.543 |
| L | 0.320 | 0.365 | 8.128 | 9.271 |
| Q | 0.140 | 0.153 | 3.556 | 3.886 |
| U | 0.105 | 0.117 | 2.667 | 2.972 |

**TO–220**
**FIVE LEAD**
**TVA SUFFIX**
CASE 314K–01
ISSUE O

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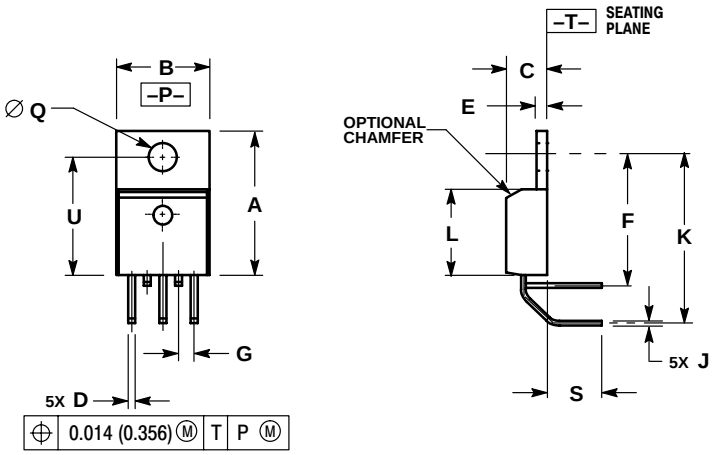
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.560 | 0.590 | 14.22 | 14.99 |
| B | 0.385 | 0.415 | 9.78 | 10.54 |
| C | 0.160 | 0.190 | 4.06 | 4.83 |
| D | 0.027 | 0.037 | 0.69 | 0.94 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| F | 0.530 | 0.545 | 13.46 | 13.84 |
| G | 0.067 BSC | | 1.70 BSC | |
| J | 0.014 | 0.022 | 0.36 | 0.56 |
| K | 0.785 | 0.800 | 19.94 | 20.32 |
| L | 0.321 | 0.337 | 8.15 | 8.56 |
| M | 0.063 | 0.078 | 1.60 | 1.98 |
| Q | 0.146 | 0.156 | 3.71 | 3.96 |
| R | 0.271 | 0.321 | 6.88 | 8.15 |
| S | 0.146 | 0.196 | 3.71 | 4.98 |
| U | 0.460 | 0.475 | 11.68 | 12.07 |
| W | 5 ° | | 5 ° | |

**TO–220**
**FIVE LEAD**
**THA SUFFIX**
CASE 314A–03
ISSUE E

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| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.572 | 0.613 | 14.529 | 15.570 |
| B | 0.390 | 0.415 | 9.906 | 10.541 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.025 | 0.038 | 0.635 | 0.965 |
| E | 0.048 | 0.055 | 1.219 | 1.397 |
| F | 0.570 | 0.585 | 14.478 | 14.859 |
| G | 0.067 BSC | | 1.702 BSC | |
| J | 0.015 | 0.025 | 0.381 | 0.635 |
| K | 0.730 | 0.745 | 18.542 | 18.923 |
| L | 0.320 | 0.365 | 8.128 | 9.271 |
| Q | 0.140 | 0.153 | 3.556 | 3.886 |
| S | 0.210 | 0.260 | 5.334 | 6.604 |
| U | 0.468 | 0.505 | 11.888 | 12.827 |

**PACKAGE THERMAL DATA**

| Parameter | | TO–220 | Unit |
|---|---|---|---|
| $R_{\Theta JC}$ | Typical | 4.1 | °C/W |
| $R_{\Theta JA}$ | Typical | 50 | °C/W |

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